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INSTRUCTION MANUAL

5100

DIGITAL MULTIMETER

DANA®

[redacted]

PUBLICATION NO. 980503

5100
DIGITAL MULTIMETER

DANA LABORATORIES, INC.
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DANA®

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Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltages hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC Mains through an autotransformer (such as a Variac or equivalent) ensure that the instrument common connector is connected to the ground (earth) connection of the power mains.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adapter.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument.

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation section.
2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.
3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

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SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION.

1.1.1 The Model 5100 Digital Multimeter/Counter (figure 1.1) is a five digit "Delayed Dual Slope" instrument with a sixth decade for a full scale reading of 199999. Measurement capability is shown in table 1.1. The basic instrument is equipped for dc voltage measurements on five ranges, ac voltage measurements on four ranges and resistance measurements on six ranges. The basic instrument is also capable of measuring frequency on two ranges: 2 MHz full scale and 20 MHz full scale.

1.2 OPTIONS.

1.2.1 The instrument is normally equipped with the Averaging AC Converter (option 14). A true rms converter (option 10) is available for measuring complex waveforms. If neither AC converter is desired option 16 may be specified when ordering. Option 16 eliminates AC measurement capability completely. Use of the option 85 current shunt set provides the capability for measuring current in six ranges. The Read and Hold probe, option 81, provides remote control of the measurement and display cycle at the measurement probe. The Data Output Card, option 51, provides serial or parallel BCD output data at the rear panel of the instrument for connection to other instruments or systems.

1.2.2 Range can be selected manually or automatically (autorange). In Autorange the proper range for a particular measurement is selected automatically (full scale is defined as "200 000" on any range). The instrument "upranges" at 200,000 counts and "downranges" at 10,000 counts. Polarity selection is also automatic and is displayed on the front panel.

1.2.3 Two operating modes are provided when the option 81 Read and Hold probe is used with the Model 5100. When the probe is connected in the Sample mode, pressing the button on the probe causes the instrument to sample at the rate of 2-1/2 measurements per second and to "hold" the measurement when the button is released. When the probe is connected in the "Hold" mode, the instrument samples until the button on the probe is depressed; the instrument holds and displays the result of the last measurement.

Table 1.1 - Measurement Capability

Range	Function			
	DCV	Ohms	Frequency	ACV
.2V	▨			
2V	▨			▨
20V	▨			▨
200V	▨			▨
1000V	▨			▨
.2 KΩ		▨		
2 KΩ		▨		
20 KΩ		▨		
200 KΩ		▨		
2 MΩ		▨		
20 MΩ		▨		
2 MHz			▨	
20 MHz			▨	

The rear panel of the instrument has provided a connection to the "HOLD" line which, when activated by the controller, causes the instrument to hold its most recent measurement.

Rack mounting is provided by the Rack Mount Adapter Kit, option 60.

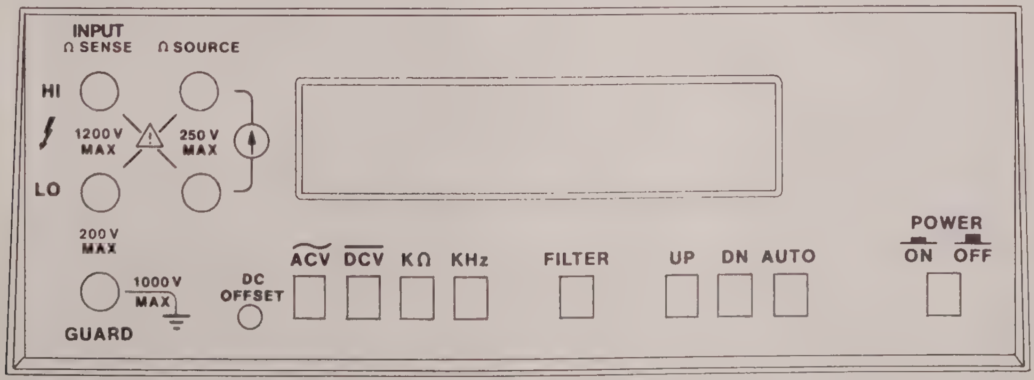


Figure 1.1 - Model 5100

1.3 ELECTRICAL DESCRIPTION.

1.3.1 The Dana Model 5100 Digital Voltmeter consists of three parts: the Signal Conditioning section, the Digital section, and the Analog-to-Digital (A/D) converter.

1.3.2 The signal conditioning section modifies the input signal before reaching the A/D converter. For dc measurements, the input signal is scaled, if required, to a 2 volt (200,000 count) signal and filtered if required. For ac or resistance measurements, the input signal is scaled, if necessary, and converted to a proportional dc value. The dc value is filtered, if necessary, and routed to the A/D converter.

1.3.3 The A/D converter changes a dc signal input into a representative digital signal. The method used to perform this task is called Delayed Dual Slope integration.

1.3.4 The digital section measures the output of the A/D converter to produce a numeric value on the instrument display that represents the value of the input signal. The digital section also provides range control, decimal placement, and BCD output.

1.4 SPECIFICATIONS.

1.4.1 Specifications are provided in table 1.2.

Table 1.2 - Specifications

GENERAL	
Maximum Counts:	200,000
Display:	5 full decades plus overrange digit (.43 inch (1.1cm) high LEDs), polarity announciator and automatic decimal point
Read Rate:	2.5 readings per second
Ranging:	Manual and automatic. Up ranges automatically at 200,000 counts and down ranges at 10,000 counts
Overrange Indication:	"200000" flashing on display
Maximum Common Mode Voltage:	1000V between guard and earth ground 200V between "—" input and guard
Power Requirement:	100, 120, 220, 240V±10%; 50-400Hz; 22 watts nominal
Weight:	3Kg (6.6 lbs.)
Dimensions:	Height x Width x Depth 73 x 200 x 250 mm 2.87 x 7.87 x 9.84 inches
Warm up Time:	30 minutes to full accuracy
Operating Temperature:	0°C to +50°C at 70% RH
Storage Temperature:	−40°C to +75°C at 80% RH
Warranty:	12 months – repair or replace malfunctions due to faulty workmanship or component failure

DC VOLTS		
Ranges:	±.200000V, ±2.00000V, ±20.0000V, ±200.000V, ±1000.00V	
Maximum Resolution:	1µV on 0.2V range	
Maximum Input Voltage:	1200V peak	
Accuracy:	24 hours, 23°C±1°C	
	0.2V, 1200V:	±(0.003% Rdg. + 4 Counts)
After Zero Adjustment	2V, 20V, 200V:	±(0.0025% Rdg. + 2 Counts)
	90 days, 23°C±5°C	
	0.2V:	±(0.006% Rdg. + 8 Counts)
	2V, 20V, 200V:	±(0.004% Rdg. + 2 Counts)
	1200V:	±(0.008% Rdg. + 4 Counts)
	1 year, 23°C±5°C	
	0.2V:	±(0.009% Rdg. + 8 Counts)
	2V, 20V, 200V:	±(0.008% Rdg. + 2 Counts)
	1200V:	±(0.02% Rdg. + 4 Counts)
Temperature Coefficient:	0°C-50°C	
	0.2V:	±(0.0005% Rdg. + 1 Count)/°C
	2V, 20V, 200V:	±(0.0005% Rdg. + .4 Count)/°C
	1200V:	±(0.0015% Rdg. + .4 Count)/°C
Input Impedance:	0.2V, 2V, 20V, 200V:	100,000MΩ
	1200V:	10MΩ
Normal (Series) Mode Noise Rejection:	Unfiltered:	>20dB at 45Hz >60dB at 50 & 60Hz
	Filtered:	>75dB at 45Hz >120dB at 50 & 60Hz
Common Mode Noise Rejection: (with 1KΩ unbalanced in either lead)	Unfiltered:	>140dB at DC >120dB at 50 & 60Hz
	Filtered:	>140dB at DC >180dB at 50 & 60Hz
Selectable Filter:	3-pole active filter	
Settling Time: (to within 0.01% of range)	Unfiltered:	30ms
	Filtered:	500ms

FREQUENCY		
Ranges:	2MHz, 20MHz Full Scale	
Maximum Resolution:	10Hz	
Accuracy:	90 days, 23°C±5°C±(0.006% Rdg. + 4 Counts) 1 year, 23°C±5°C±(0.01% Rdg. + 4 Counts)	
Input Characteristics:		
Sinewave Sensitivity:	350mV rms to 20MHz	
Input Impedance:	510KΩ//100pF	
Maximum Input Voltage:	350V rms (±500V peak)	
Measurement Time:	2MHz range:	.1s
	20MHz range:	.1s with divide by 10 prescaler

OHMS

Ranges:	.200000KΩ, 2.00000KΩ, 20.0000KΩ, 200.000KΩ, 2000.00KΩ, 20000.0KΩ	
Maximum Resolution:	1mΩ on 0.2KΩ range	
Maximum Input Voltage:	250V rms continuous (±350V peak) on all ranges	
Measurement Scheme:	True 4-wire	
Accuracy:	90 days, 23°C ±5°C	
(1Ω Max Resistance in – Sense Lead)	0.2KΩ, 2,000KΩ:	±(0.007% Rdg. + 6 Counts)
	2KΩ-200KΩ:	±(0.006% Rdg. + 6 Counts)
	20,000KΩ:	±(0.02% Rdg. + 6 Counts)
	1 year, 23°C ±5°C	
	0.2KΩ, 2,000KΩ:	±(0.013% Rdg. + 6 Counts)
	2KΩ-200KΩ:	±(0.01% Rdg. + 6 Counts)
	20,000KΩ:	±(0.03% Rdg. + 6 Counts)
Temperature Coefficient:	0°C-50°C	
	0.2KΩ, 2,000KΩ:	±(0.0012% Rdg. + .6 Counts)/°C
	2KΩ-200KΩ:	±(0.001% Rdg. + .6 Counts)/°C
	20,000KΩ:	±(0.003% Rdg. + .6 Counts)/°C
Maximum Open Circuit Voltage:	5V	
Current Through Unknown:	0.2KΩ:	1mA
	2KΩ:	1mA
	20KΩ:	100μA
	200KΩ:	10μA
	2,000KΩ:	1μA
	20,000KΩ:	100nA
Normal (Series) Mode Noise Rejection:	Same as DC Volts	
Common Mode Noise Rejection:	Same as DC Volts	
Settling Time: (to within 0.01% of range)	Unfiltered:	
	0.2KΩ-200KΩ:	30ms
	2,000KΩ:	50ms
	20,000KΩ:	200ms
	Filtered:	Add 5 x R seconds to unfiltered settling time where R is range selected in MΩ

AC VOLTS

Averaging AC Calibrated rms

Ranges:	2.00000V, 20.0000V, 200.000V, 1000.00V rms	
Maximum Resolution:	10μV on 2V range	
Maximum Input Voltage:	1000V rms, 1500V peak, decreasing to 20V rms at 1MHz. 2×10^7VHz product maximum on any range	
Accuracy:	1 year, 23°C ±5°C (.1% to 100% of range)	
	2V-200V:	
	30-50Hz	±(1.1% Rdg. + 60 Counts)
	50-100Hz	±(0.35% Rdg. + 20 Counts)
(No Adjustments)	100-10KHz	±(0.2% Rdg. + 10 Counts)
	10K-20KHz	±(0.35% Rdg. + 20 Counts)
	20K-100KHz	±(1.1% Rdg. + 60 Counts)
	1000V (0-500V):	
	30-100Hz	±(0.35% Rdg. + 40 Counts)
	100-10KHz	±(0.25% Rdg. + 40 Counts)
	10K-20KHz	±(0.35% Rdg. + 40 Counts)
	1000V (500-1000V):	
	30-100Hz	±(0.6% Rdg. + 40 Counts)
	100-10KHz	±(0.4% Rdg. + 40 Counts)

AC VOLTS (Cont)

Accuracy (Cont):	10K-20KHz	±(60% Rdg. + 40 Counts)
	90 days, 23°C ±5°C(.1% to 100% of range) All frequencies and ranges: substract ±0.1% Rdg. from the 1 year specification	
Temperature Coefficient:	±(0.008% Rdg. + 2 Counts)/°C	
Input Impedance:	2MΩ || 100pF	
Common Mode Noise Rejection: (with 1KΩ unbalance in either lead)	80dB, DC to 60Hz	
Filter:	The selectable active filter is automatically engaged whenever the AC function is selected	
Settling Time:	1 second maximum	

True RMS (Option 10)

Ranges:	2.00000V, 20.0000V, 200.000V, 1000.00V rms	
Maximum Resolution:	10μV on 2V range	
Maximum Input Voltage:	1000V rms, 1500V peak, decreasing to 20V rms at 1MHz. 2×10^7VHz product maximum on any range	
Accuracy:	1 year, 23°C ±5°C (1% to 100% of range)	
	2V:	
	30-100Hz	±(0.45% Rdg. + 700 Counts)
	100-5KHz	±(0.25% Rdg. + 700 Counts)
(No Adjustments)	5K-50KHz	±(0.45% Rdg. + 700 Counts)
	50K-100KHz	±(0.65% Rdg. + 900 Counts)
	100K-200KHz	±(5.15% Rdg. + 800 Counts)
	200K-300KHz	±(10.15% Rdg. + 1300 Counts)
	20V-1000V:	
	30-100Hz	±(0.45% Rdg. + 700 Counts)
	100-20KHz	±(0.25% Rdg. + 500 Counts)
	20K-50KHz	±(0.35% Rdg. + 700 Counts)
	50K-100KHz	±(0.45% Rdg. + 700 Counts)
	100K-200KHz	±(5.15% Rdg. + 800 Counts)
	200K-300KHz	±(10.15% Rdg. + 1300 Counts)
	90 days, 23°C ±5°C (1% to 100% of range) All frequencies and ranges: substract ±(0.15% Rdg. + 300 Counts) from the 1 year specification	
Temperature Coefficient:	Total drift as tested between 25°C and 50°C: <400 digits on all ranges	
Input Impedance:	1MΩ || 100pF	
Crest Factor:	5 : 1 maximum at full scale	
	$5 \times \sqrt{\frac{\text{full scale of range}}{\text{reading}}}$	for other voltages
Common Mode Noise Rejection: (with 1KΩ unbalance in either lead)	80dB, DC-60Hz	
Filter:	The selectable active filter is automatically engaged whenever the AC function is selected	
Settling Time:	1 second maximum	

Table 1.2 - Specifications continued

DATA OUTPUT (Option 51)	
Information:	Numeric BCD output in both parallel and byte serial mode, range, function, DATA VALID lines, and HOLD line.
Logic Type:	Standard TTL levels, 8-4-2-1 BCD
Input Command:	Single read/hold line
Isolation:	1000V peak between Data Output and Analog Commons
Auxiliary Output Voltage:	+5V DC ±10%, 50mA
Data Output Connector:	PCB edge connector (Amp #583718-9) supplied with option

READ/HOLD PROBE (Option 81)	
Input Resistance:	10^9 Ohms shunted by instrument
Input Capacitance:	200 pF
Maximum Input Voltage:	500V DC or AC peak

CURRENT (Option 85)	
Ranges:	20µA (DC only), 200µA, 2mA, 20mA, 200mA, 2A
Maximum Resolution:	100pA on 20µA range
Accuracy:	
DC Current:	0.01% plus DC Volts accuracy (0.07% on 2A range)
AC Current:	2m-2A ranges 50Hz–10KHz 0.15% plus ACV accuracy 200µA range 50Hz-1KHz 0.65% plus ACV accuracy 2000mA range 50Hz–10KHz .2% Reading
Overload:	1 watt or 250V peak whichever occurs first

2.1 GENERAL.

2.1.1 This section covers the visual inspection, installation and storage of the Model 5100.

2.2 UNPACKING AND INSPECTION.

2.2.1 The instrument is enclosed between two molded, plastic-foam forms and packaged in a double-walled cardboard carton for shipment. The plastic forms hold the instrument securely in the carton and absorb any reasonable external shock normally encountered in transit.

2.2.2 Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the instrument from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3 POWER CONNECTIONS.

2.3.1 Power is supplied to the instrument through a standard 6-foot long detachable power cord. The ground pin (round) on the power plug is electrically connected to the power transformer primary winding shield. It is important that this pin be connected to a good quality earth ground.

2.3.2 The cord connects to the instrument at power input jack J201 on the rear panel.

2.3.3 The power fuse holder is located next to the power input jack and requires a .25 ampere fuse.

2.3.4 The instrument is designed to operate at one of four selectable line voltages; 100, 120, 220 or 240V AC.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

2.3.5 Selection of the line voltage is accomplished by removing the instrument from its case and positioning a printed circuit jumper so that the desired line voltage appears in the aperture in the right hand side of the case. Figure 2.1 illustrates the location of the PCB jumper and figure 2.2 illustrates the aperture with the jumper in place for 120 volt operation.

2.4 STORAGE REQUIREMENTS.

2.4.1 The instrument can be stored at temperatures ranging from –40°C to +75°C at 80% relative humidity without damaging the PCBs or components. The instrument must be brought up to operating range (0°C to 50°C) before power is applied.

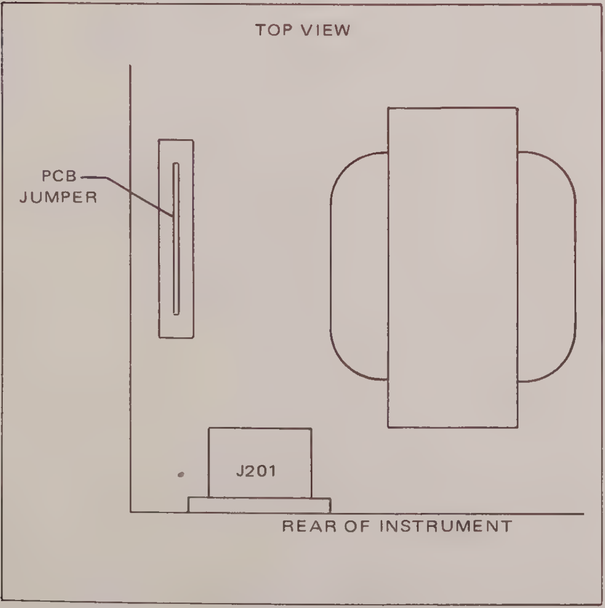


Figure 2.1 - Line Selector PCB Jumper Location

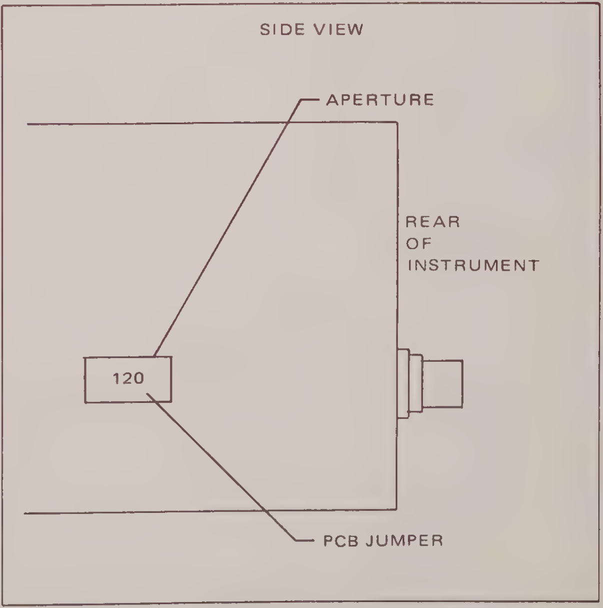


Figure 2.2 - Line Voltage Indicator Aperture

2.5 RESHIPMENT PACKAGING REQUIREMENTS.

2.5.1 The shipping carton with its molded plastic foam forms and plastic dust cover is specifically designed to provide the required support necessary for safe shipment. Whenever possible, these should be used for reshipment.

2.5.2 If the original packing materials are not available, proceed as follows:

a. Wrap instrument in plastic or heavy paper.

b. Place packing material around all sides of instrument and pack in cardboard box.

c. Place instrument and inner container in a sturdy cardboard or wooden box. Mark box with appropriate precautionary labels.

2.6 INPUT CONNECTORS.

2.6.1 The signal input connectors are located on the front panel and consists of five universal binding posts. The posts are spaced 3/4 inch center to center and accept spade lugs, banana plugs and American Wire Gage (AWG) sizes up to number 12.

2.6.2 The power cable connector J201 is located on the rear panel.

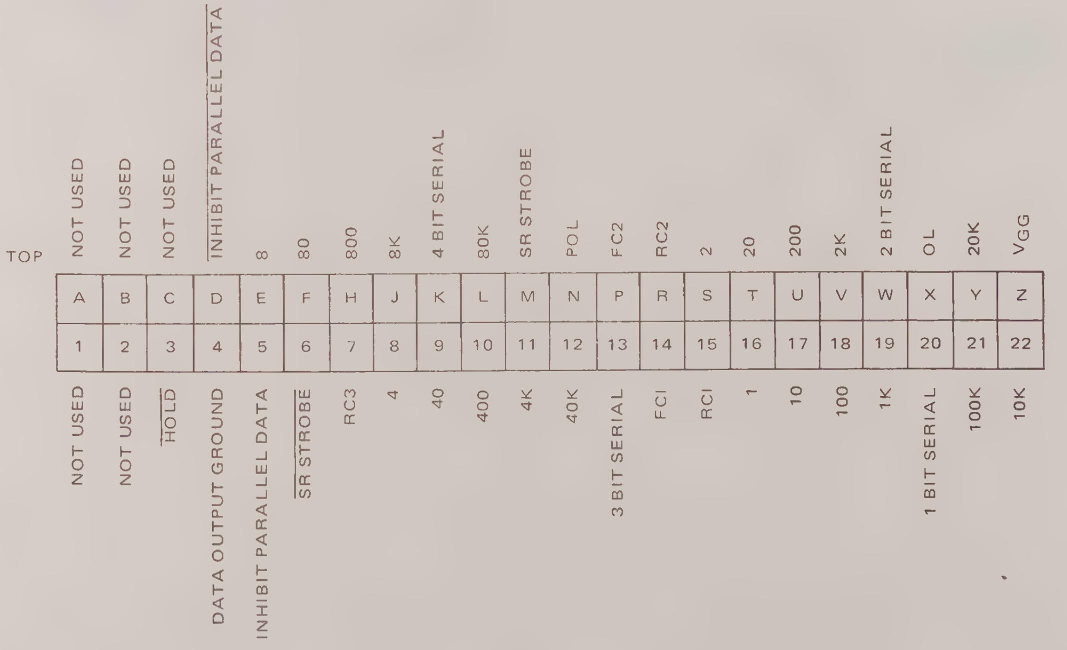
2.6.3 The three prong connector, J202, for the sample/hold accessory is located on the rear panel.

2.6.4 The BCD output connector, J203, (Option 51) is illustrated in figure 2.3. This connector is a printed circuit board edge pin connector. The mating connector for the BCD output is an AMP No. 583718-9 and is included in the Data Output Shipping Kit part number 403920.

The pin assignments are shown in figure 2.3.

2.7 RACK MOUNTING.

2.7.1 The Model 5100 may be left or right-hand mounted in a standard 19 inch, 3-1/2 high instrument rack. Option 60 rack mounting accessory (page 6-24) may be used for this purpose.



TOP			
NOT USED	A	1	NOT USED
NOT USED	B	2	NOT USED
NOT USED	C	3	$\overline{\text{HOLD}}$
$\overline{\text{INHIBIT PARALLEL DATA}}$	D	4	DATA OUTPUT GROUND
8	E	5	INHIBIT PARALLEL DATA
80	F	6	$\overline{\text{SR STROBE}}$
800	H	7	RC3
8K	J	8	4
4 BIT SERIAL	K	9	40
80K	L	10	400
SR STROBE	M	11	4K
POL	N	12	40K
FC2	P	13	3 BIT SERIAL
RC2	R	14	FC1
2	S	15	RC1
20	T	16	1
200	U	17	10
2K	V	18	100
2 BIT SERIAL	W	19	1K
OL	X	20	1 BIT SERIAL
20K	Y	21	100K
V_{GG}	Z	22	10K

Figure 2.3 - BCD Output Connector Pin Assignments

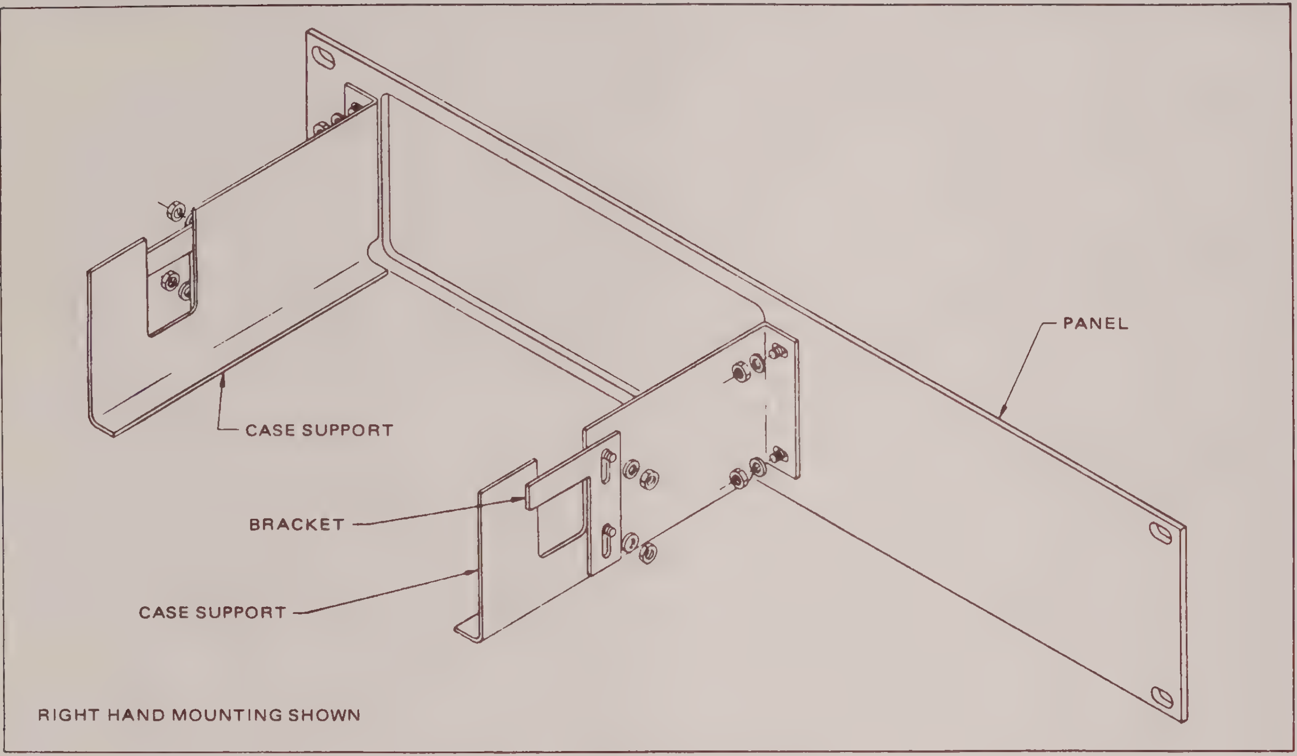


Figure 2.4 - Rack Mount Installation

2.7.2 The option is shown in figure 2.4 and assembled as described below:

a. With the bail of the instrument in a vertical position above the instrument, slide the case supports up against the side of the instrument.

b. Move the bail to the back of the instrument and mount "L" shaped brackets and secure with lock washer and nuts.

c. Move the bail and set the instrument up on the rear panel.

d. Place the cut-out of panel over the front of the instrument. Be sure the offset is on the correct side for your installation. Secure panel with lock washers and nuts.

e. To clear the power plug be sure the bail is up or down flush with the top or bottom of instrument before installation into rack.

3.1 GENERAL.

3.1.1 This section presents instructions for operating the Model 5100 Digital Multimeter. These instructions consist of preliminary checks and power up procedures followed by a description of the instruments controls and indicators. This is followed by a description of the operation for each function and instructions for connection of the instrument to the device under test.

3.2 OPERATION.

3.2.1 Before operating the instrument, it is strongly recommended that the operator read this entire section in order to avoid damage to the unit. After reading the operating instructions, refer to the Installation Section, paragraph 2.3.4, and check the position of the line voltage selector.

CAUTION

This instrument may be damaged if operated on a line voltage other than that called for by the line voltage selection jumper.

3.2.2 After ensuring that the line voltage selector is in the proper position and replacing the cover on the instrument, connect the power cord to the power outlet and turn it on by depressing the POWER switch so that it is in the ON position as shown on the front panel. Allow the instrument to warm up for approximately one minute. When the instrument is turned on, the display should light. The instrument is now ready for operation. Refer to the following paragraphs for details of control operation and measurement connections.

3.3 CONTROLS AND INDICATORS.

3.3.1 Function Select.

3.3.1.1 Four buttons select the functions: ACV, DCV, KΩ and kHz. The buttons are interlocked allowing only one button to be pressed at a time.

3.3.2 Filter.

3.3.2.1 The filter button is a push on, push off switch that selects an active filter. The filter provides normal mode noise attenuation as shown.

@ 10 Hz – 20 dB
@ 50 Hz – 60 dB

3.3.3 Range Select.

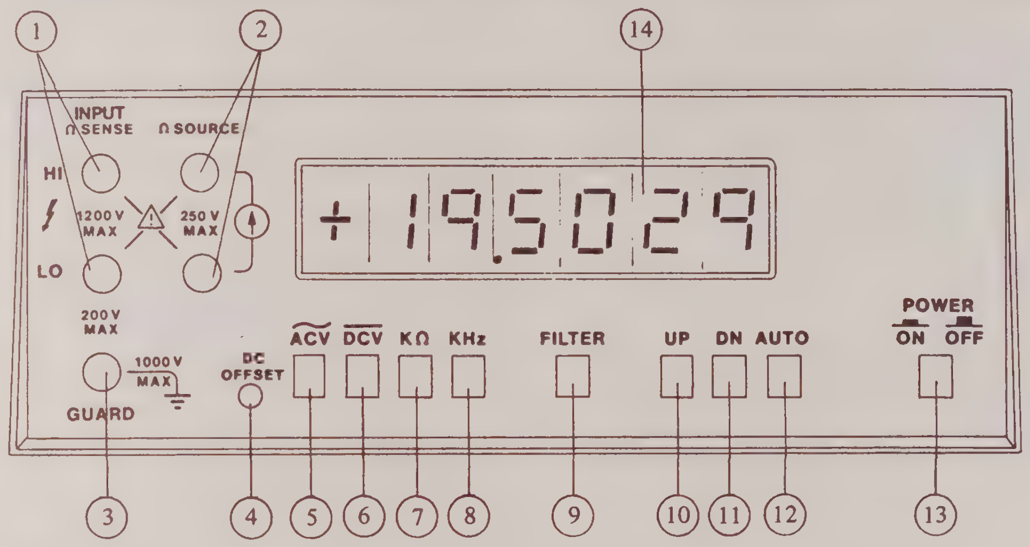
3.3.3.1 Three buttons are used to control ranging: AUTO, UP, and DN.

a. AUTO is a push on, push off switch. When pushed in, the instrument automatically selects the range most compatible with the input signal, the instrument up ranges at 200,000 counts or full scale and down ranges at 5% of range.

b. UP button is a momentary switch. UP range occurs one range at a time with each measurement cycle with each depression of the button when DMM is in non-auto range position.

c. DN button is a momentary switch. DN range occurs one range at a time with each depression. It will also down range in the auto range mode, if one needs to, for input signals between 10% and 1% of range.

Table 3.1 - Front Panel Identification


1
2
14
INPUT
Ω SENSE
Ω SOURCE
HI
1200 V MAX
250 V MAX
LO
+19.5029
200 V MAX
1000 V MAX
GUARD
DC OFFSET
ACV
DCV
KΩ
KHz
FILTER
UP
DN
AUTO
POWER
ON
OFF
3
4
5
6
7
8
9
10
11
12
13

① Voltage Input, Ohms Sense Terminals, J101 (Hi) and J102 (Lo), and Frequency Input

② Ohms Current, J103 (Source), J104 (Sink)

③ Guard Terminal, J105

④ DC offset. Allows user to zero front panel display

⑤ AC Volts Function Select Switch, push on

⑥ DC Volts Function Select Switch, push on

⑦ KOHMS Function Select Switch, push on

⑧ KHz Function Select Switch, push on

⑨ FILTER Select Switch, push on, push off

⑩ UP. Causes instrument to up range. Momentary on

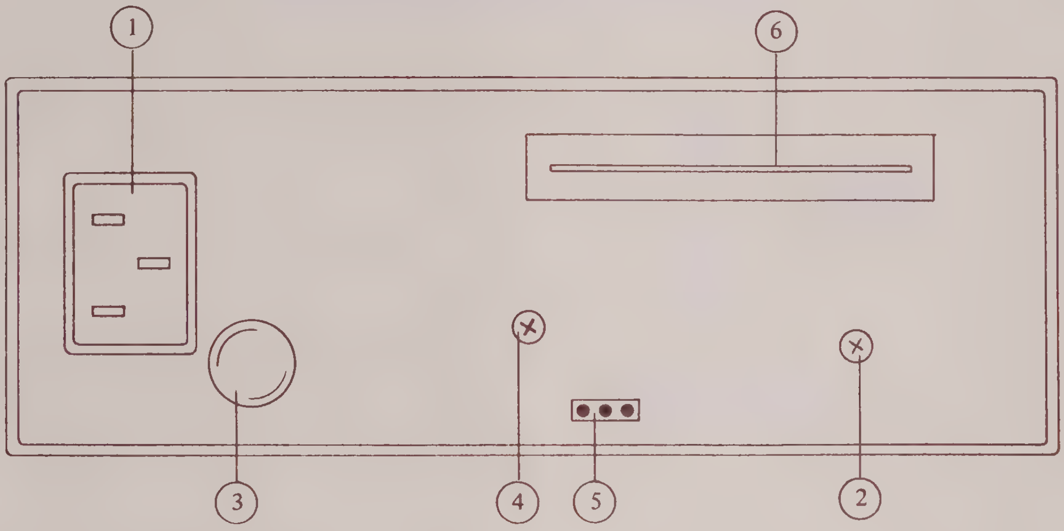
⑪ DOWN. Causes instrument to down range. Momentary on

⑫ AUTO. Selects range most compatible with input signal. Push on, push off

⑬ POWER Switch. Push on, push off

⑭ DISPLAY. Consists of 6 decade readouts “0 – 9” (MSD = 0, 1, or 2) and a ± readout LED

Table 3.2 - Rear Panel Identification



① Power Receptacle J201 receives power cable

② Disassembly Screw. Removal of this screw allows removal of case

③ Power Fuse Holder, F201

④ Disassembly Screw. Removal of this screw allows removal of case

⑤ Connector J202, Sample/Hold accessory, Option 81

⑥ BCD Output, J203, Option 51

3.3.4 Power.

3.3.4.1 The power switch is a push on, push off switch. When on, power is applied to all circuits.

3.4 DISPLAY.

3.4.1 The Display consists of six numeric LEDs, .43 inches high, and a polarity LED.

3.5 MEASUREMENT CONNECTIONS.

CAUTION

Before taking any ACV measurements, refer to chart showing the maximum input voltages, figure 3.1.

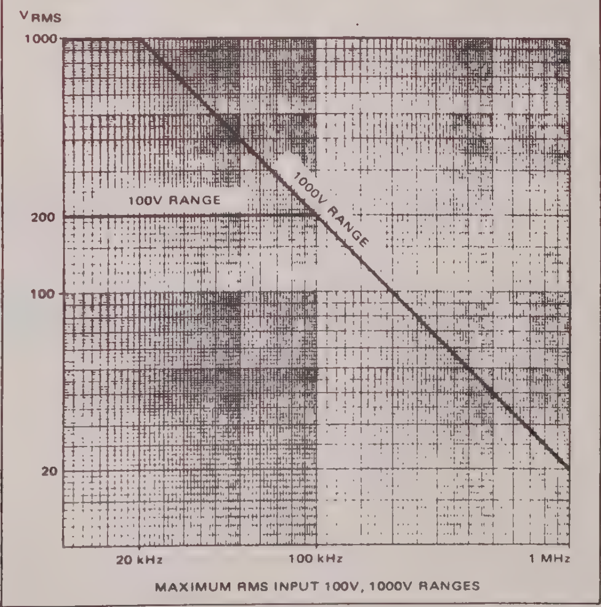


Figure 3.1 - Maximum RMS Input Voltage

3.5.1 For basic ac or dc voltage measurements, the measurement connection recommended to minimize the effects of noise requires a two-conductor shielded cable connected as shown in figure 3.2.

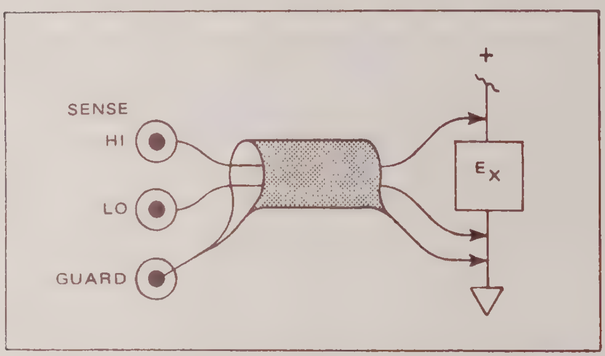


Figure 3.2 - Basic Voltage Measurement Connections

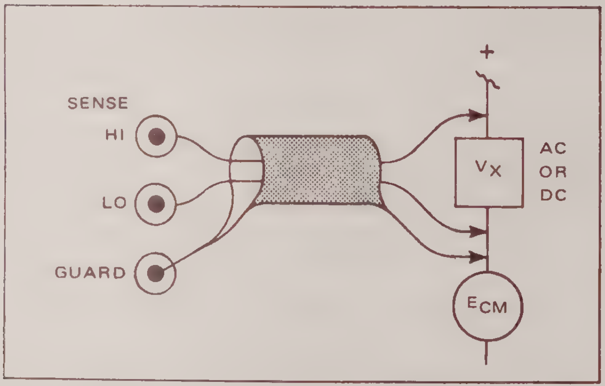


Figure 3.3 - Connections where CM Present

3.5.2 For all voltage measurements, the GUARD lead and LO lead are connected to the measurement point nearest ground potential. Somewhat less shielding is achieved by placing a jumper between LO and GUARD. This arrangement is adequate for measuring all but low voltage (mV) levels and/or in high-noise environments. When making measurements of low voltage levels in noisy environments or where common mode signals are present it is recommended that the two-wire-shielded type of input cable be used. This input configuration is shown in figure 3.3.

The option 80 input cable is especially useful in low signal high noise applications.

3.5.3 When making "floating" voltage measurements (both measurement points above ground potential), do not connect GUARD to measurement ground without making sure that the voltage between GUARD and LO does not exceed 200 volts.

3.5.4 Ohms Measurement.

3.5.4.1 Ohms measurement consists of the application of a fixed value of current through the unknown resistor, supplied through the HI and LO Ω current terminals. The resulting voltage drop is measured by the DMM through the HI and LO SENSE terminals. The current is set for each range at a level that produces a full scale reading when the unknown resistor is the same as the range selected (i.e., a 1 Kohm resistor measured on the 2 Kohm range produces a half scale reading of 1.00000).

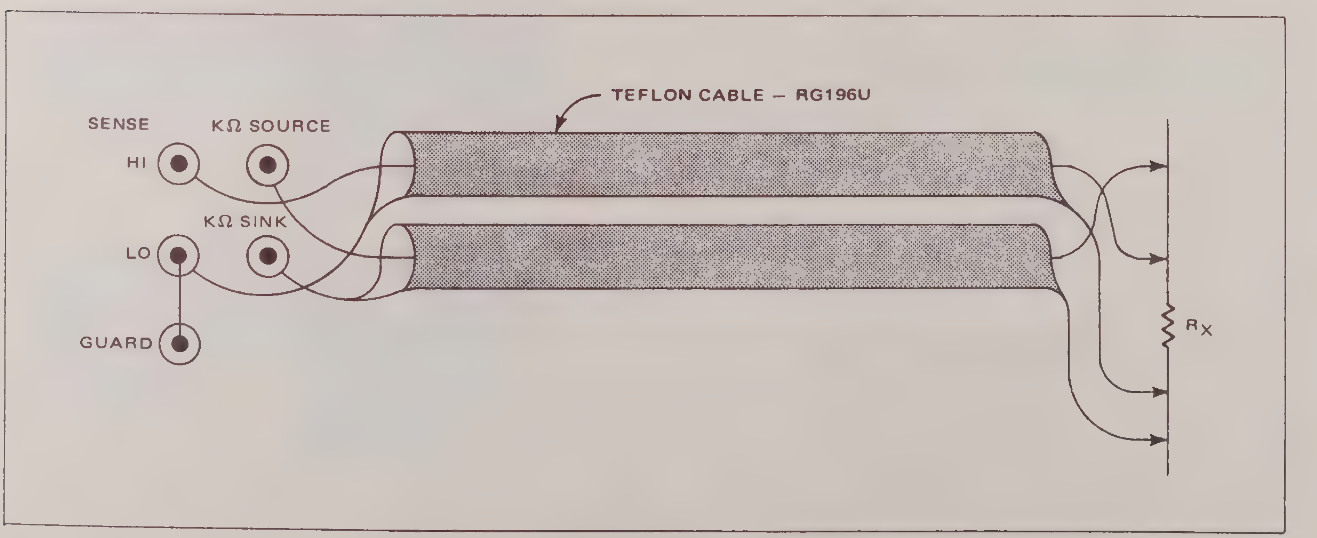


Figure 3.4 - Ohms Measurement Connection

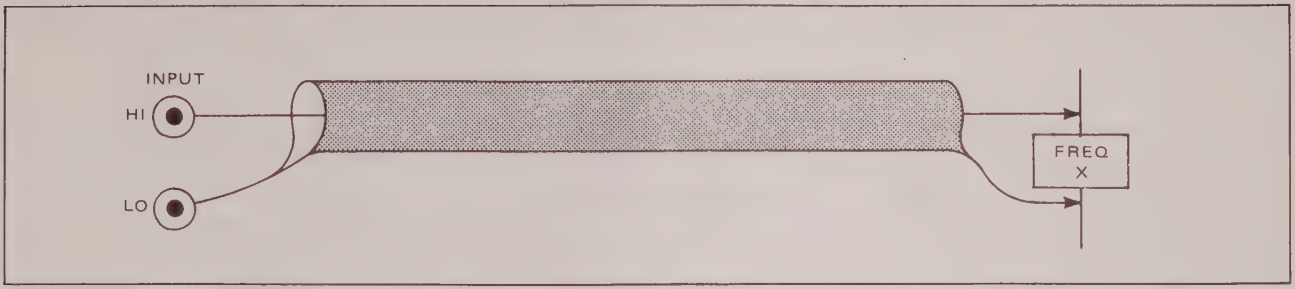


Figure 3.5 - Frequency Measurement Connections

3.5.4.2 Connecting the instrument to a resistor for ohms measurement consists of connecting both the KΩ current source and HI SENSE terminals to one side of the resistor and both the KΩ current sink and LO SENSE terminals to the other side of the resistor. An example is shown in figure 3.4.

3.5.5 Frequency kHz.

3.5.5.1 To measure frequency with the Model 5100 connect the input signal as shown in figure 3.5.

3.5.5.2 The option 80 input cable may also be used for frequency measurement in a noisy environment.

3.5.6 Current Measurement.

3.5.6.1 The Model 5100 may be used to measure AC or DC current if used with option 85 current shunts. In operation the shunt for the desired current range is plugged into the HI and LO input terminals. The test lead set or input cable is then plugged into the shunt and connected to the measurement circuit.

3.5.7 High Voltage Measurement (5 KV DC).

3.5.7.1 The DCV range of the Model 5100 may be extended to 5000 volts through use of the option 82 High Voltage probe accessory on the 1000 DCV range.

WARNING

When using option 82 high voltage probe keep your fingers behind the circular shield to avoid electrical shock or personal injury.

3.5.7.2 To use the option 82 probe simply plug it into the HI-LO input terminals. The DMM must be on the 1000 range (DMM input resistance equals 10 MΩ). Connect the alligator clip to the negative or ground side of the measurement source and touch the probe tip to the circuit point to be measured.

3.5.8 High Voltage Measurement (50 KV DC).

3.5.8.1 For measuring high voltages in the 0-50 KV range in circuits such as cathode ray tube power supplies, the option 83 high voltage probe accessory is available. This accessory extends the operating range of the instrument to 50 KV DC. In operation the probe is plugged into the HI-LO INPUT terminals. The DMM must be on the 1000 range (DMM input resistance equals 10 MΩ). The alligator-clip lead is connected to the negative or ground side of the measurement circuit and the probe tip is touched to the high voltage point to be measured.

WARNING

When using option 83 high voltage probe keep your fingers behind the corona ring to avoid electrical shock or personal injury.

3.5.9 R.F. Voltage Measurements.

3.5.9.1 To measure voltage in the radio-frequency (RF) range two optional probes are available. Option 84 extends the measurement capability to 200 MHz while the option 90 probe extends the range to 520 MHz. In operation the probe cable is plugged into the HI-LO INPUT connectors of the instrument. The probe ground (or low side) alligator clip is connected to one side of the device under measurement and the probe tip is touched to the other measurement point. The instrument then measures the RF voltage and presents the voltage reading on the display. The reading is the DC voltage equivalent of the AC RF voltage or .707 times the RF (sine wave) voltage value.

3.5.10 READ/HOLD Accessory Probe.

3.5.10.1 The option 81 Read/Hold probe is designed to enable an operator to make measurements in awkward positions, places where he may be concerned about slipping off the measurement test point or in situations where the probe and the meter cannot be viewed at the same time.

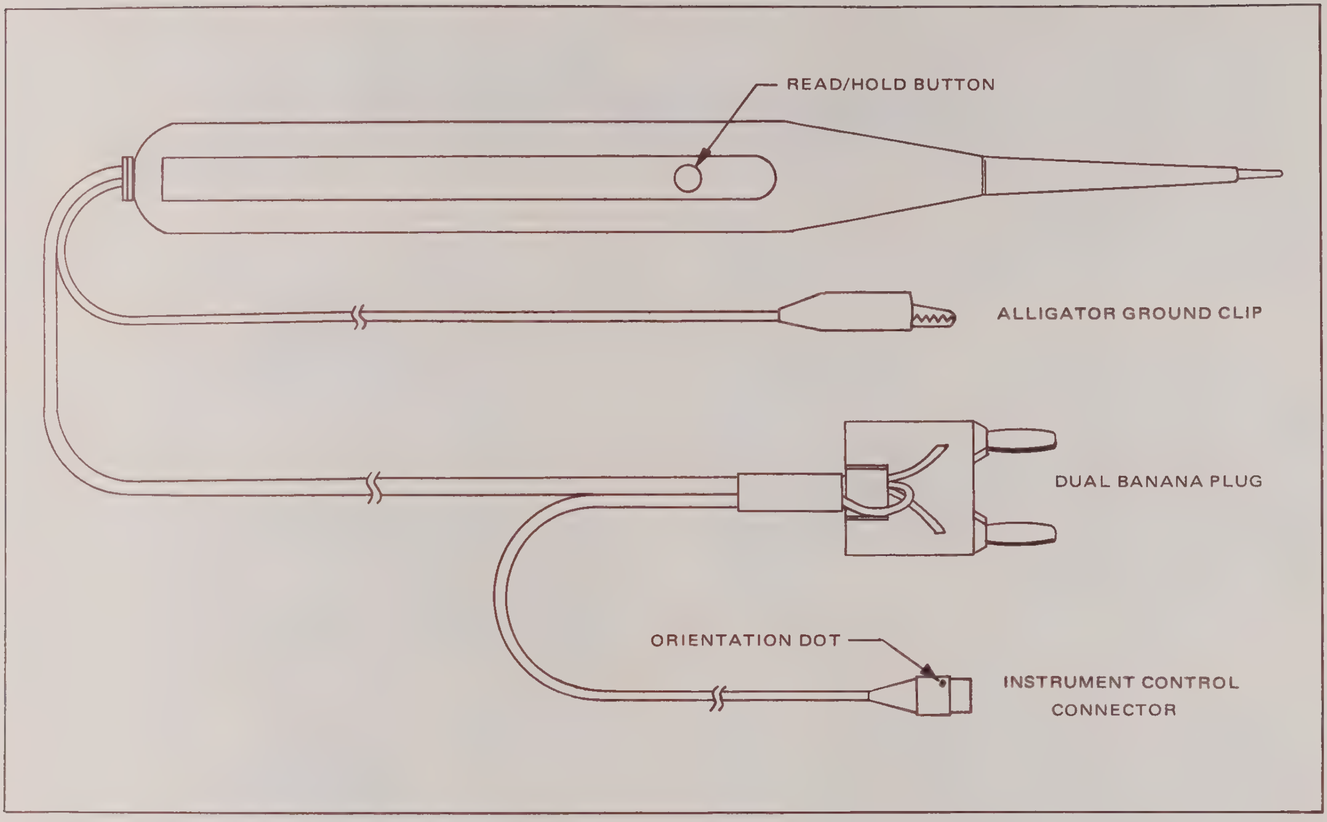


Figure 3.6 - Read/Hold Probe

3.5.10.2 The probe (figure 3.6) consists of a probe assembly, a six-foot cable, a dual banana plug, alligator ground clip and an instrument control plug. The probe assembly contains a pushbutton switch that controls the read or hold circuits in the instrument.

3.5.10.3 Attach the probe to the instrument by plugging the dual banana plug to the binding posts as shown in figure 3.7 so that the GND side of the plug goes to the LO binding post. The plug connects to the left hand terminals on the Model 5100 or to the right hand terminals on the Model 4600.

3.5.10.4 Connect the instrument control connector to the rear panel of the instrument as shown in figure 3.8.

3.5.10.5 Note that there is a tiny white dot on one side of the instrument control connector. When the connector is inserted in the instrument so that the dot is on top the instrument and probe are in the push-to-read mode; conversely when the connector is connected with the dot on the bottom the instrument is in the push-to-hold mode.

3.5.10.6 In the push-to-read mode the instrument will take measurements so long as the probe pushbutton is held down and stops when the button is released. Thus you can use the probe to reach into an inconvenient location with the probe tip, push and hold the button for a short period, release the button and remove the probe from the circuit. The DVM will hold the reading thereby eliminating the need to hold the probe on the test point while watching the instrument display.

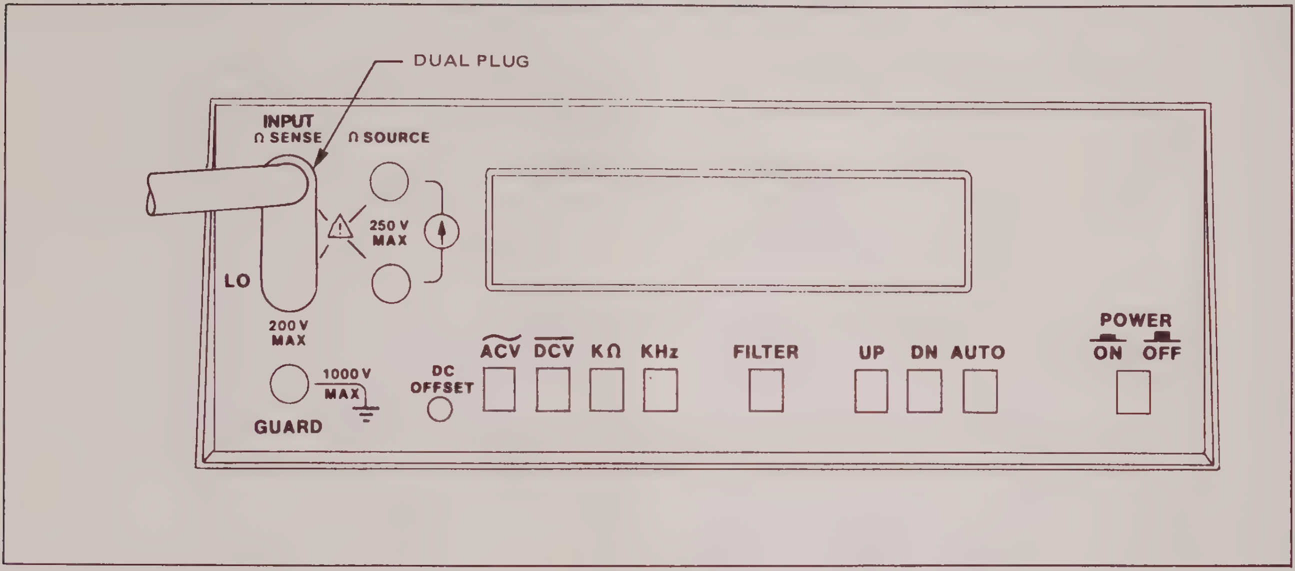

DUAL PLUG
INPUT
Ω SENSE
Ω SOURCE
250 V
MAX
LO
200 V
MAX
1000 V
MAX
GUARD
DC
OFFSET
ACV
DCV
KΩ
KHz
FILTER
UP
DN
AUTO
POWER
ON
OFF

Figure 3.7 - Connection of Read/Hold Probe to Instrument

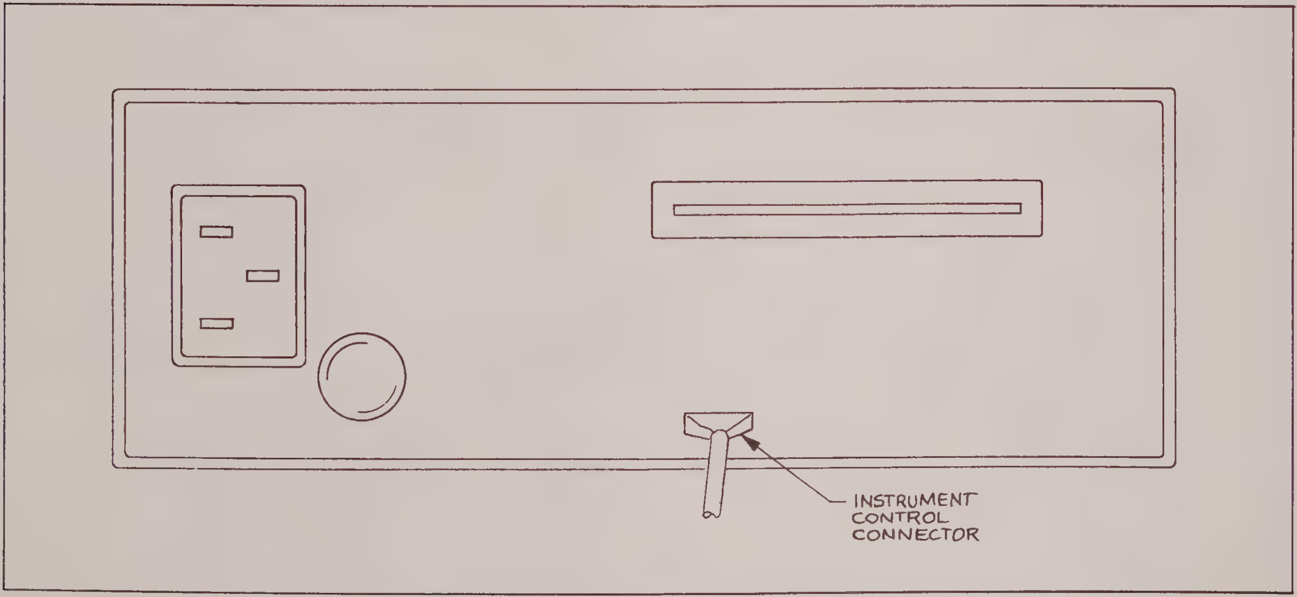

INSTRUMENT
CONTROL
CONNECTOR

Figure 3.8 - Connection of Control Connector to Rear Panel

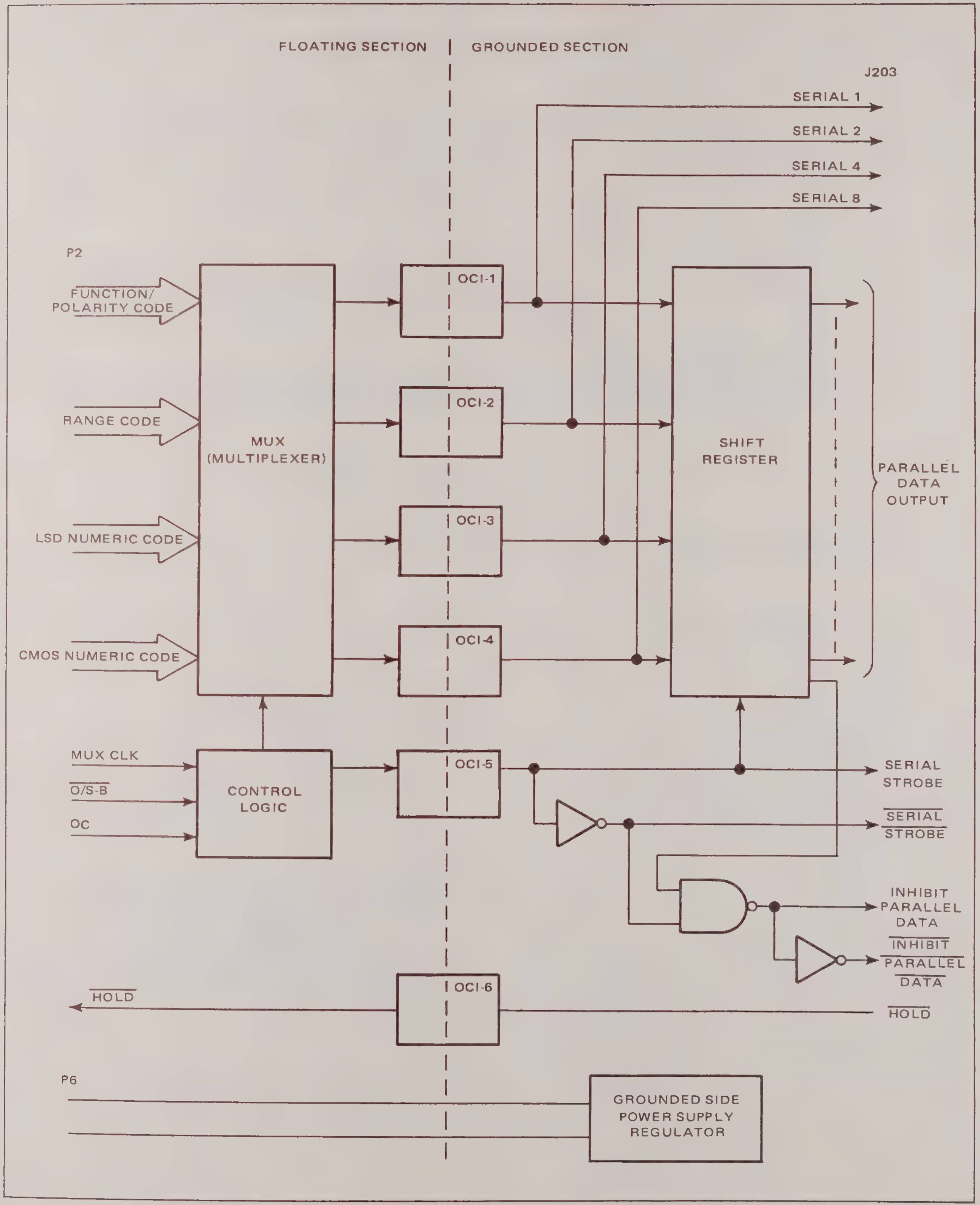

FLOATING SECTION
GROUNDED SECTION
J203
SERIAL 1
SERIAL 2
SERIAL 4
SERIAL 8
P2
FUNCTION/
POLARITY CODE
RANGE CODE
LSD NUMERIC CODE
CMOS NUMERIC CODE
MUX
(MULTIPLEXER)
OCI-1
OCI-2
OCI-3
OCI-4
OCI-5
OCI-6
SHIFT
REGISTER
PARALLEL
DATA
OUTPUT
MUX CLK
O/S-B
OC
CONTROL
LOGIC
SERIAL
STROBE
SERIAL
STROBE
INHIBIT
PARALLEL
DATA
INHIBIT
PARALLEL
DATA
HOLD
HOLD
P6
GROUNDED SIDE
POWER SUPPLY
REGULATOR

Figure 3.9 - BCD Data Output

3.6 BCD OUTPUT.

3.6.1 The Model 5100 Option 51, (Isolated BCD) Data Output provides the function, range, polarity, and numeric readout data in BCD form, both serially and in parallel, from a single connector on the instrument rear panel. The output data is completely isolated from the measurement portion of the 5100, thereby preserving the common mode noise characteristics of the instrument.

3.6.2 Mechanical Description.

3.6.2.1 All components for the option are on a single printed circuit board that is mounted above the DMM main PCB by four screws attached to the wrap-around chassis. An aluminum shield, secured to the PCB assembly, prevents digital noise, generated on the option PCB, from affecting the measurement circuitry on the main PCB assembly.

3.6.2.2 One end of the option PCB forms an edge connector that extends out the back of the DMM through a slot provided for this purpose. This connector is the option output and is designated J202.

3.6.3 Electrical Description.

3.6.3.1 The option, shown in simplified block diagram form in figure 3.9, consists of a floating section, a grounded section, and six optical couplers.

3.6.3.2 The floating section codes and multiplexes the binary data from the measurement portion of the DMM and transmits the data through optical couplers 1 through 5. The sixth optical coupler is used for Hold (see paragraph 3.9.8.1). The floating section consists of:

FUNCTION/POLARITY CODE
Range Code
Numeric Code (LSD and CMOS)
Multiplexer (MUX)
CONTROL LOGIC

3.6.3.3 The multiplexer consists of two dual 4-line to 1-line data selector/multiplexers, U5 and U6 (74LS153). The multiplexer receives inputs from the Main logic and Interconnection PC boards counter and control logic section in BCD form for function, polarity, range, and numeric (LSD and CMOS) value. The multiplexer has a 4-bit byte output which drives the four optical couplers. The output byte corresponds to one of the three possible input bytes, selected by the control logic.

3.6.3.4 The Control Logic, shown in simplified form in figure 3.10, consists of a synchronizer (U3), clock gate (U2), counter (U4), and decode selector (U2). The control logic generates the operational logic for the multiplexer outputs that drive the optical couplers and also provides timing information for the shift registers on the grounded (output) side. The circuitry operates by a predetermined series of steps shown in figure 3.11. The operation starts when the

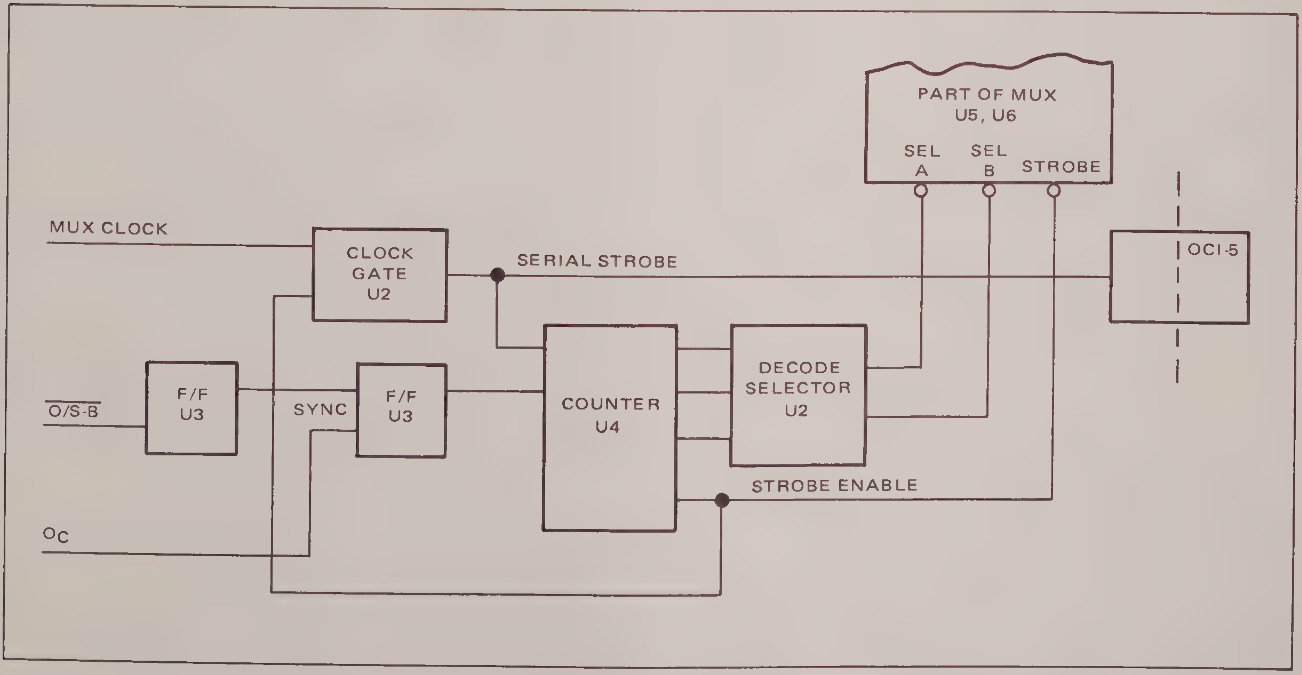


Figure 3.10 - Control Logic

One-Shot B $\overline{Q}$ output ($\overline{O/S\text{-}B}$) goes high, causing the output of the synchronizer to go high at U3-5. When the output of the CMOS (3814) multiplexer drive, O_C, is coincident, the counter, U4, is reset at U4-11; which enables the clock gate at U2-2. This allows the MUX clock (approximately 500 Hz) to advance the counter, and through inverter U1-12, drive the Serial Strobe optical coupler, OCI-5, to clock the output serial shift registers, U9, U10, U11, and U12.

3.6.3.5 The gated MUX clock advances the counter through eight steps. The eighth MUX clock pulse causes the output at U4-11 to go high, which disables the MUX clock gate and ARMS the Synchronizer F/F clear inputs at U3 pin 1 and 13 for the next digitize sequence. The counter outputs are decoded by U2 to drive the (U5, U6) Multiplexers $\overline{\text{select A}}$, $\overline{\text{select B}}$, and $\overline{\text{strobe}}$ inputs; which provide the serial outputs that drive the Optical coupled isolators (OCI-1 through OCI-4).

3.6.3.6 The grounded portion of the option converts the data from the optical isolators to provide the output data in serial or parallel form for a recorder, printer, or other digitally operated device at the output connector, J203. The grounded portion consists of a shift register, control circuitry, Hold circuit, and a power supply regulator.

3.6.3.7 The shift register consists of four 8-bit, parallel-out, serial shift registers, each of which is driven by one of the four data optical couplers (OCI-1 thru 4). The outputs of the optical couplers are also used as the serial outputs, being binarily weighted (1-2-4-8). The Serial Strobe

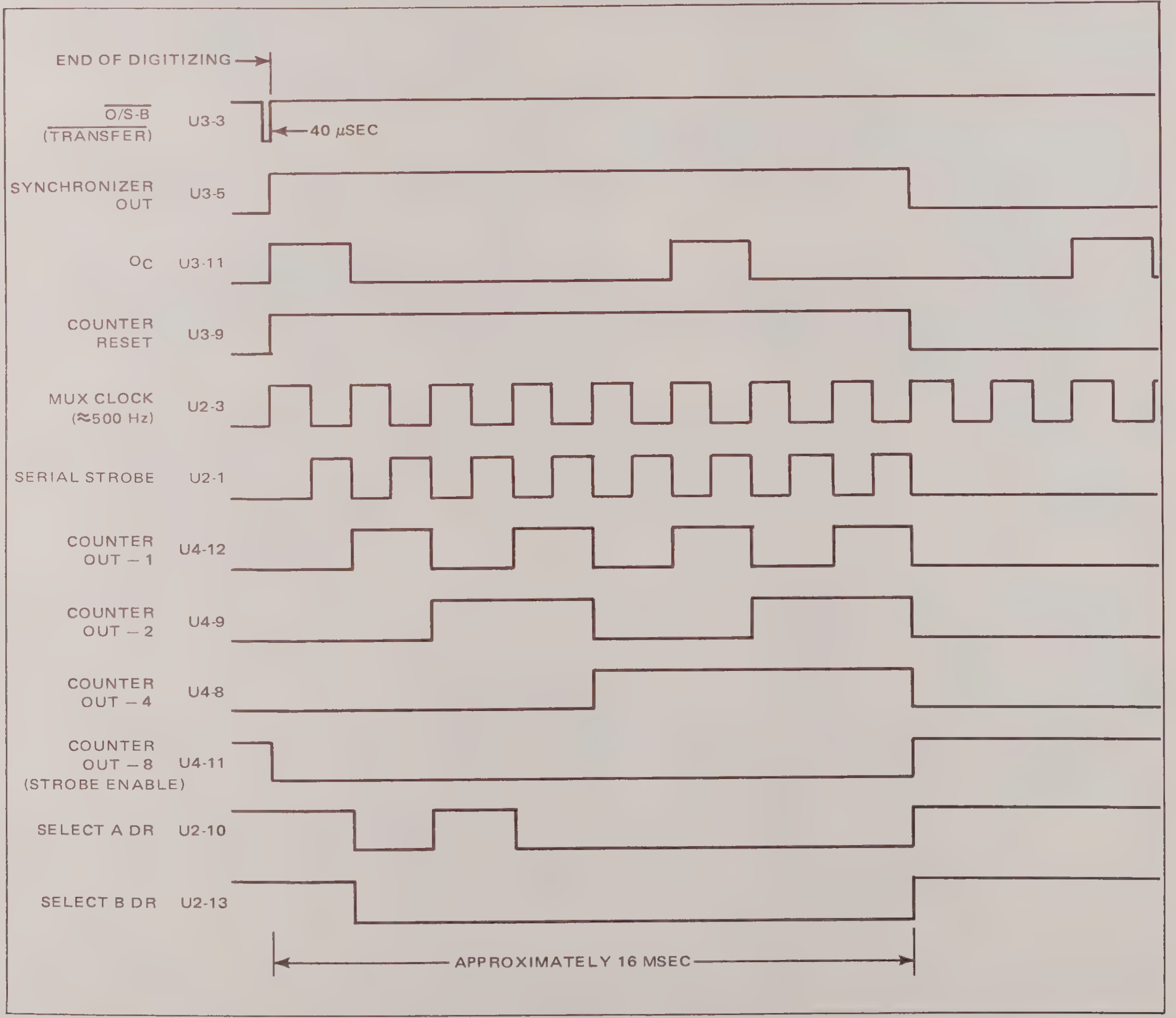

END OF DIGITIZING
O/S-B (TRANSFER)
U3-3
40 μSEC
SYNCHRONIZER OUT
U3-5
OC
U3-11
COUNTER RESET
U3-9
MUX CLOCK (≈500 Hz)
U2-3
SERIAL STROBE
U2-1
COUNTER OUT – 1
U4-12
COUNTER OUT – 2
U4-9
COUNTER OUT – 4
U4-8
COUNTER OUT – 8 (STROBE ENABLE)
U4-11
SELECT A DR
U2-10
SELECT B DR
U2-13
APPROXIMATELY 16 MSEC

Figure 3.11 - Control Logic Timing Diagram

pulse is received through Optical Coupler OCI-5 and applied to the clock inputs of the serial shift registers to also present a parallel data output format for a printer, recorder, or etc.

3.6.3.8 The Serial Strobe and (inverted) $\overline{\text{Serial Strobe}}$ provide the timing control to decode output data in serial form. The Inhibit Parallel Data and Parallel Data Valid provide the timing control to decode output data in parallel form.

3.6.3.9 The Hold circuit permits the operator to electrically stop the DMM from taking new readings by driving the $\overline{\text{Hold}}$ input (J203-3) to Data Output common (J203-4). The circuit consists of two Inverters (U8 and U1) and an optical isolator (OCI-6).

3.6.4 Operation.

3.6.4.1 The Option (51) is provided with a mating connector (Dana P/N 600810), a connector Key (Dana P/N 600811) to prevent misalignment, mounting screws and 44 connector pins (Dana P/N 600809). Pin identification is provided in table 3.3 for serial and parallel outputs, depending upon the type of operation selected by the user.

Table 3.3 - J203 Pin Identification

Bottom	J203		Top
Not Used	1	A	Not Used
Not Used	2	B	Not Used
$\overline{\text{HOLD}}$	3	C	Not Used
Data Output Ground	4	D	$\overline{\text{Inhibit Parallel Data}}$
Inhibit Parallel Data	5	E	8
$\overline{\text{Serial Strobe}}$	6	F	80
RC3	7	H	800
4	8	J	8K
40	9	K	4-Bit Serial (8)
400	10	L	80K
4K	11	M	Serial Strobe
40K	12	N	Polarity
3-Bit Serial (4)	13	P	FC2
FC1	14	R	RC2
RC1	15	S	2
1	16	T	20
10	17	U	200
100	18	V	2K
1K	19	W	2-Bit Serial (2)
1-Bit Serial (1)	20	X	O/L
100K	21	Y	20K
10K	22	Z	VGG

3.6.4.2 All output lines are TTL logic and are referenced to J203 pin 4. A reference +5 volt output is provided at J203 pin Z for printer reference. Output levels of the data are defined as:

Logic High: +2.4 volts (minimum)
Logic Low: +0.8 volts (maximum –8 mA current sink)

3.6.4.3 FUNCTION CODES.

3.6.4.3.1 The function codes are shown in table 3.4.

Table 3.4 - Function Codes

	FC1	FC2	Binary Weight
DCV	1	1	3
ACV	0	1	2
KΩ	1	0	1
kHz	0	0	0

3.6.4.4 RANGE CODES.

3.6.4.4.1 The range codes are shown in table 3.5.

Table 3.5 - Range Codes

	RC1	RC2	RC3	Binary Weight
.2	0	1	0	2
2	1	1	0	3
20	0	0	1	4
200	1	0	1	5
2000	0	1	1	6
20000	1	1	1	7

3.6.4.5 POLARITY CODES.

3.6.4.5.1 The polarity codes are:

(+) PLUS POL = 1
(–) MINUS POL = 0

3.6.4.6 SERIAL OUTPUT.

3.6.4.6.1 The data output is available in serial form on four lines. Serial Strobe is available in logic true and its complement form. Pin identification for lines used in serial output is provided in table 3.6.

Table 3.6 - Serial Output Pin Identification

Bottom	J203		Top
$\overline{\text{HOLD}}$	3	K	4-Bit Serial (8)
Data Output Ground	4	M	Serial Strobe
$\overline{\text{Serial Strobe}}$	6	W	2-Bit Serial (2)
3-Bit Serial (4)	13	Z	VGG
1-Bit Serial (1)	20		

3.6.4.6.2 At the completion of a measurement (digitize), the data strobe output generates eight 1 millisecond pulses at approximately a 500 Hz rate. During each strobe pulse, a new data byte appears at the serial data output lines. The serial data is shown in table 3.7.

3.6.4.7 PARALLEL OUTPUT.

3.6.4.7.1 The parallel data output is available in standard BCD form on 33 lines of J203 as shown in table 3.8.

3.6.4.7.2 Data at the output pins is available when Inhibit Parallel Data at J203 pin 5 is true (approximately 16 milliseconds). $\overline{\text{Inhibit Parallel Data}}$ at J203 pin D can be used when negative true logic is required for a print pulse.

3.6.4.8 HOLD.

3.6.4.8.1 The hold line is an external command. When held at a logic low, the DMM is inhibited from updating display and data output information. If Hold is commanded during a digitize cycle, the reading will be inhibited after the cycle has been completed. The Hold F/F (U9) on the Main Logic and Interconnection board disables the One-Shot A (U11) and prevents LSD and CMOS latches from being updated.

Table 3.8 - Parallel Output Pin Identification

Bottom	J203		Top
$\overline{\text{HOLD}}$	3	D	$\overline{\text{Inhibit Parallel Data}}$
Data Output Ground	4	E	8
Inhibit Parallel Data	5	F	80
RC3	7	H	800
4	8	J	8K
40	9	L	80K
400	10	N	Polarity
4K	11	P	FC2
40K	12	R	RC2
FC1	14	S	2
RC1	15	T	20
1	16	U	200
10	17	V	2K
100	18	X	O/L
1K	19	Y	20K
100K	21	Z	VGG
10K	22		

3.6.4.8.2 The value of the last measurement remains in the display and is available at the parallel data output lines (although no new parallel data and its complement pulse is generated). The data is not present at the serial data output lines following the last measurement taken.

Table 3.7 - Serial Data Output

	Word							
	1	2	3	4	5	6	7	8
1-Bit Serial (1)	FC1	RC1	1	10	100	1K	10K	100K
2-Bit Serial (2)	FC2	RC2	2	20	200	2K	20K	O/L
3-Bit Serial (4)	POL	RC3	4	40	400	4K	40K	Logic Lo
4-Bit Serial (8)	Logic Hi	Logic Lo	8	80	800	8K	80K	Logic Lo

4.1 INTRODUCTION.

4.1.1 This section describes the operation of the Model 5100 DMM and includes the basic technique used as well as a more detailed explanation of the major functional portions.

4.2 CIRCUIT DESCRIPTION.

4.2.1 A functional block diagram of the instrument is presented in figure 4.1. The diagram is divided into four major areas for purposes of discussion; (1) Signal Conditioning, (2) Digitizing, (3) Ranging, and (4) Display. Measurement signals applied to the input terminals are routed to the appropriate signal conditioning device by the function controls. Because the isolator amplifier operates with low voltages, dc measurement signals higher than 2 volts must be scaled down. This is accomplished by the attenuator. The attenuator also changes the source current flow on the ohms ranges. The ac converter contains its own voltage attenuator for the ac voltage ranges above 2 volts.

4.2.2 The ac converter produces a dc output level proportional to the ac measurement applied to its input. On the ac ranges this dc signal is applied to the isolator.

4.2.3 The ohms amplifier produces a dc output level proportional to the direct current at its input on the ohms ranges. Like the ac converter, the dc output voltage produced by the ohms configuration is applied to the isolator input.

4.2.4 The isolator functions as a buffer to prevent application of "normal-mode" noise or "common-mode" voltages to the integrator circuit. It also serves to provide a high input impedance on all dc ranges of the instrument except the 1000 range. The output of the isolator is applied to the integrator for conversion to a digital count.

4.2.5 The integrator is a dual-slope conversion device which charges a capacitor for a fixed time period to a level which is dependent upon the level of the measurement signal (see figure 4.3). The capacitor is then discharged at a fixed rate by switching a reference signal of opposite polarity onto the input of the integrator. As the capacitor discharges it crosses the zero volt level and begins to charge in the opposite direction. A null detector in the integrator circuit senses this zero-crossing and produces a "null-detect" signal. The null detect signal is used by the Timing and Control circuits to stop the measurement counter. Thus, the count value in the measurement counter is a direct digital representation of the measurement signal voltage applied to the instrument.

4.2.6 The Timing and Control circuits provide the integrator and counter with the synchronization required to perform the analog to digital conversion of the measurement signal. The instrument performs continuous measurement cycles. The measurement cycle is illustrated in figure 4.2.

4.2.7 Note that the digitize cycle is divided into four major periods. The first, which is 100 milliseconds long, is the signal integrate period. During this time the Timing and Control circuits apply the measurement signal to the input of the integrator. The integrator, during this period, charges a capacitor to a level determined by the value of the measurement signal. During the next period, the Timing and Control circuits apply a reference voltage, opposite in polarity to the measurement signal, to this capacitor in order to discharge it. The capacitor is discharged at a fixed rate and as the charge on the capacitor reaches zero, the integrator produces a null detect signal which is used by the Timing and Control circuits to stop the count in the measurement counter. Thus, the value of the count in the measurement counter is directly proportional to the value of the measurement signal. During the signal integrate period, the Timing and Control circuits detect the polarity of the measurement signal and store this information in a flip-flop.

4.2.8 The measurement counter is a special integrated circuit chip which includes the measurement counter, a latch to store the count, a decoder, and multiplexer. The measurement count stored in the latch is in BCD code and must be converted to a 7-line code for application to the LED display. This is accomplished by the 4-to-7 line decoder. The multiplexer, in the measurement counter, transfers one digit of information at a time from the latch to the 4-to-7 line decoder. The 7-line code from the decoder is applied to all of the LED display digits in parallel. The MUX switching line turns on each LED digit as its code appears on the output of the 7-line decoder. Thus, the LED display devices are actually flashing in sequence but the display rate is of a frequency that makes the LEDs appear to be continuously illuminated.

4.2.9 Range control is accomplished either manually from the front panel or automatically by the internal range control logic. There are three switches on the front panel of the instrument labeled UP, DOWN, and AUTO. If the operator desires to use the auto ranging feature, he simply pushes in the Auto pushbutton (a latching type switch). If it is desired to use manual range control, the Auto range switch is unlatched and the operator then has control through use of the UP and DOWN pushbuttons. The range control logic configures the voltage attenuator to scale

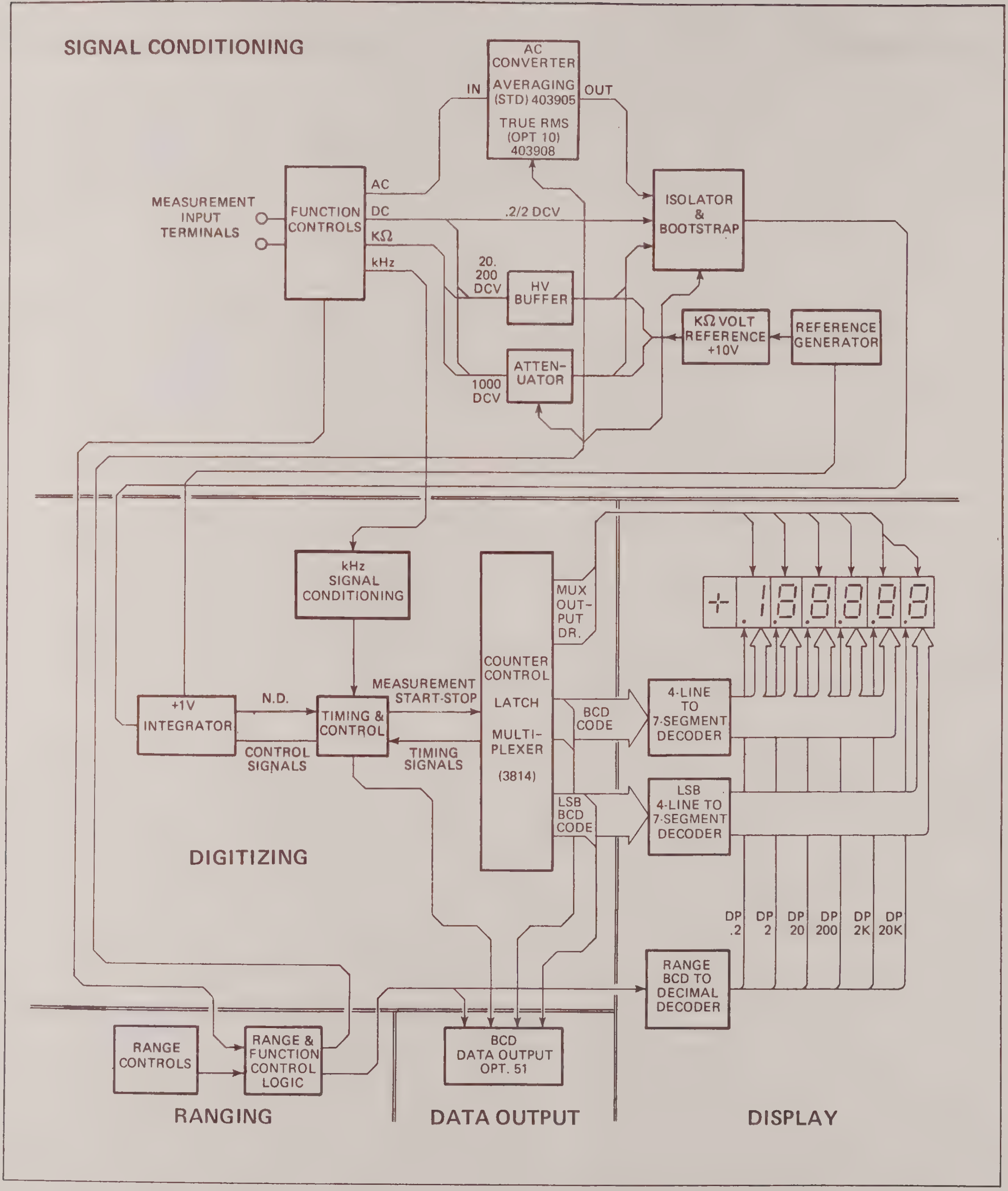

SIGNAL CONDITIONING
AC CONVERTER
IN
AVERAGING (STD) 403905
OUT
TRUE RMS (OPT 10) 403908
MEASUREMENT INPUT TERMINALS
FUNCTION CONTROLS
AC
DC
KΩ
kHz
.2/2 DCV
ISOLATOR & BOOTSTRAP
20. 200 DCV
HV BUFFER
KΩ VOLT REFERENCE +10V
REFERENCE GENERATOR
ATTEN- UATOR
1000 DCV
kHz SIGNAL CONDITIONING
MUX OUT- PUT DR.
COUNTER CONTROL
LATCH
MULTI- PLEXER
(3814)
MEASUREMENT START-STOP
+1V INTEGRATOR
N.D.
TIMING & CONTROL
CONTROL SIGNALS
TIMING SIGNALS
BCD CODE
4-LINE TO 7-SEGMENT DECODER
LSB BCD CODE
LSB 4-LINE TO 7-SEGMENT DECODER
+ .18888.8
DIGITIZING
DP .2
DP 2
DP 20
DP 200
DP 2K
DP 20K
RANGE BCD TO DECIMAL DECODER
RANGE CONTROLS
RANGE & FUNCTION CONTROL LOGIC
BCD DATA OUTPUT OPT. 51
RANGING
DATA OUTPUT
DISPLAY

Figure 4.1 - Functional Block Diagram

down measurement input signals. In addition, it controls the attenuator in the AC Converter circuit. The isolator gain is also controlled by the range control logic and is switched from X1 to X10 gain, depending on the selected operating range of the instrument. The range code from the range control logic is applied to the decimal decoder which provides the signals to the LED displays to properly locate the decimal point.

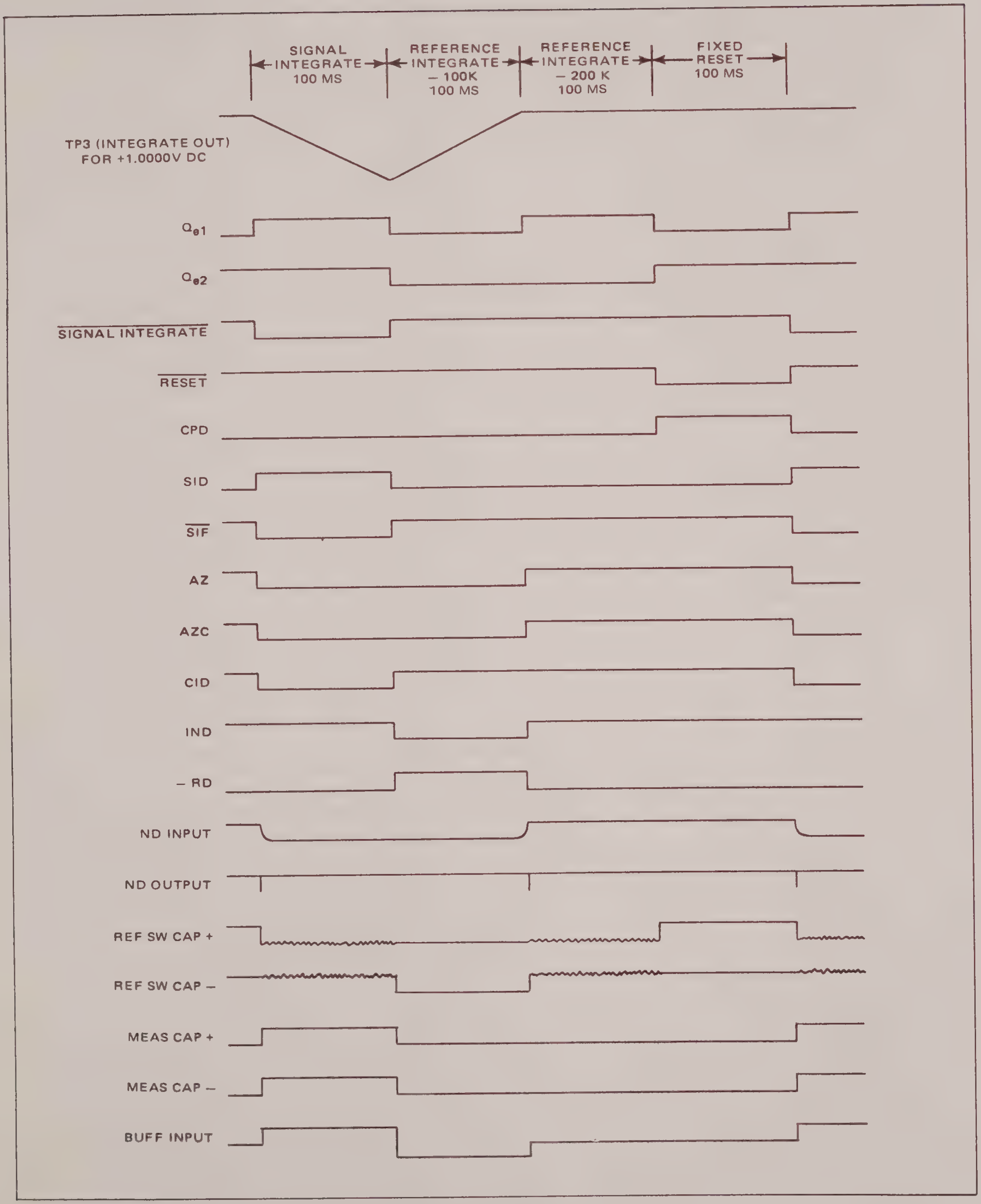

SIGNAL INTEGRATE 100 MS
REFERENCE INTEGRATE – 100K 100 MS
REFERENCE INTEGRATE – 200 K 100 MS
FIXED RESET 100 MS
TP3 (INTEGRATE OUT) FOR +1.0000V DC
$Q_{\theta 1}$
$Q_{\theta 2}$
$\overline{\text{SIGNAL INTEGRATE}}$
$\overline{\text{RESET}}$
CPD
SID
$\overline{\text{SIF}}$
AZ
AZC
CID
IND
– RD
ND INPUT
ND OUTPUT
REF SW CAP +
REF SW CAP –
MEAS CAP +
MEAS CAP –
BUFF INPUT

Figure 4.2 - Measurement Cycle

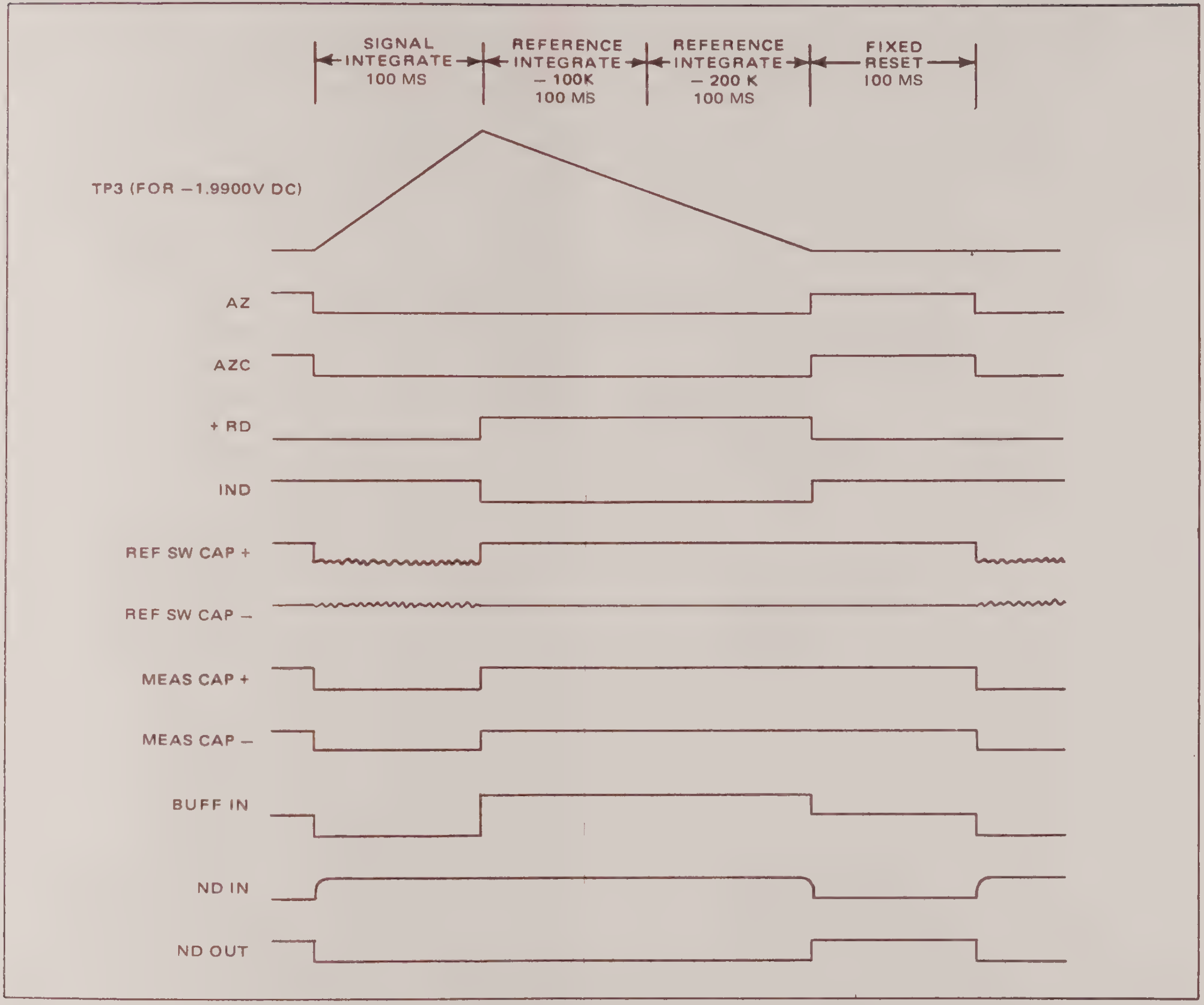


Figure 4.2 - Measurement Cycle continued

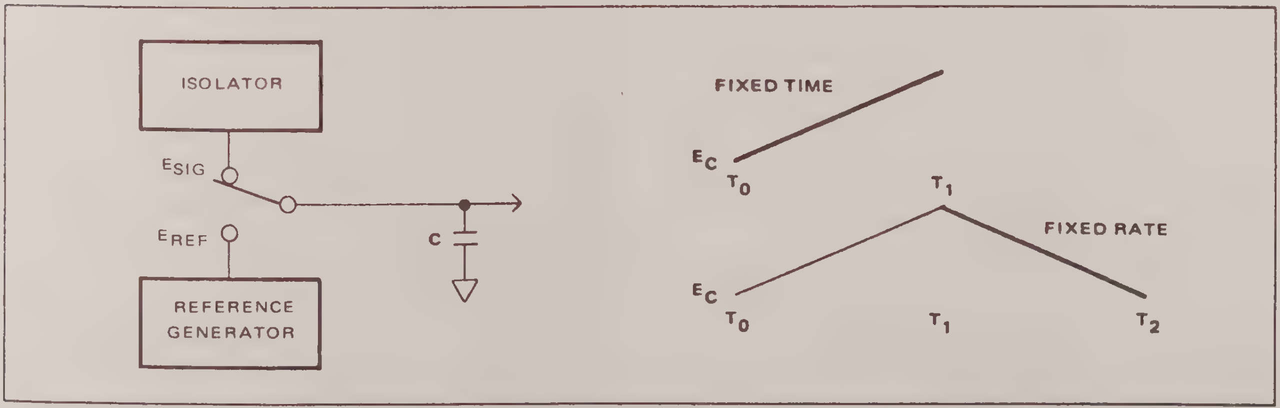

ISOLATOR
E_{SIG}
E_{REF}
REFERENCE GENERATOR
C
FIXED TIME
E_C
T_0
T_1
FIXED RATE
E_C
T_0
T_1
T_2

Figure 4.3 - Dual Slope Integration

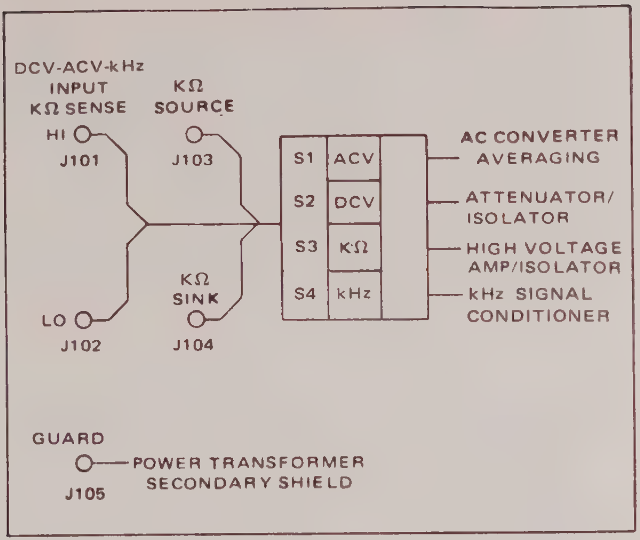

DCV-ACV-kHz INPUT KΩ SENSE
KΩ SOURCE
HI
J101
J103
LO
J102
KΩ SINK
J104
S1
ACV
S2
DCV
S3
KΩ
S4
kHz
AC CONVERTER AVERAGING
ATTENUATOR/ ISOLATOR
HIGH VOLTAGE AMP/ISOLATOR
kHz SIGNAL CONDITIONER
GUARD
J105
POWER TRANSFORMER SECONDARY SHIELD

Figure 4.4 - Function Controls

4.3 DETAILED CIRCUIT DESCRIPTION.

4.3.1 The following paragraphs present the detailed description of the individual functional circuits of the instrument. The circuit descriptions are arranged in the order that they appear on the overall block diagram, figure 4.1.

4.3.2 Note that the schematic diagrams in the Drawing Section (Section 6) of this manual contain outlines of the components included in a functional circuit group. These outlined areas contain the same title of the blocks shown in diagrams in the Theory Section.

4.3.3 Function Controls.

4.3.3.1 A simplified block diagram of the function controls is illustrated in figure 4.4. The function controls consist of

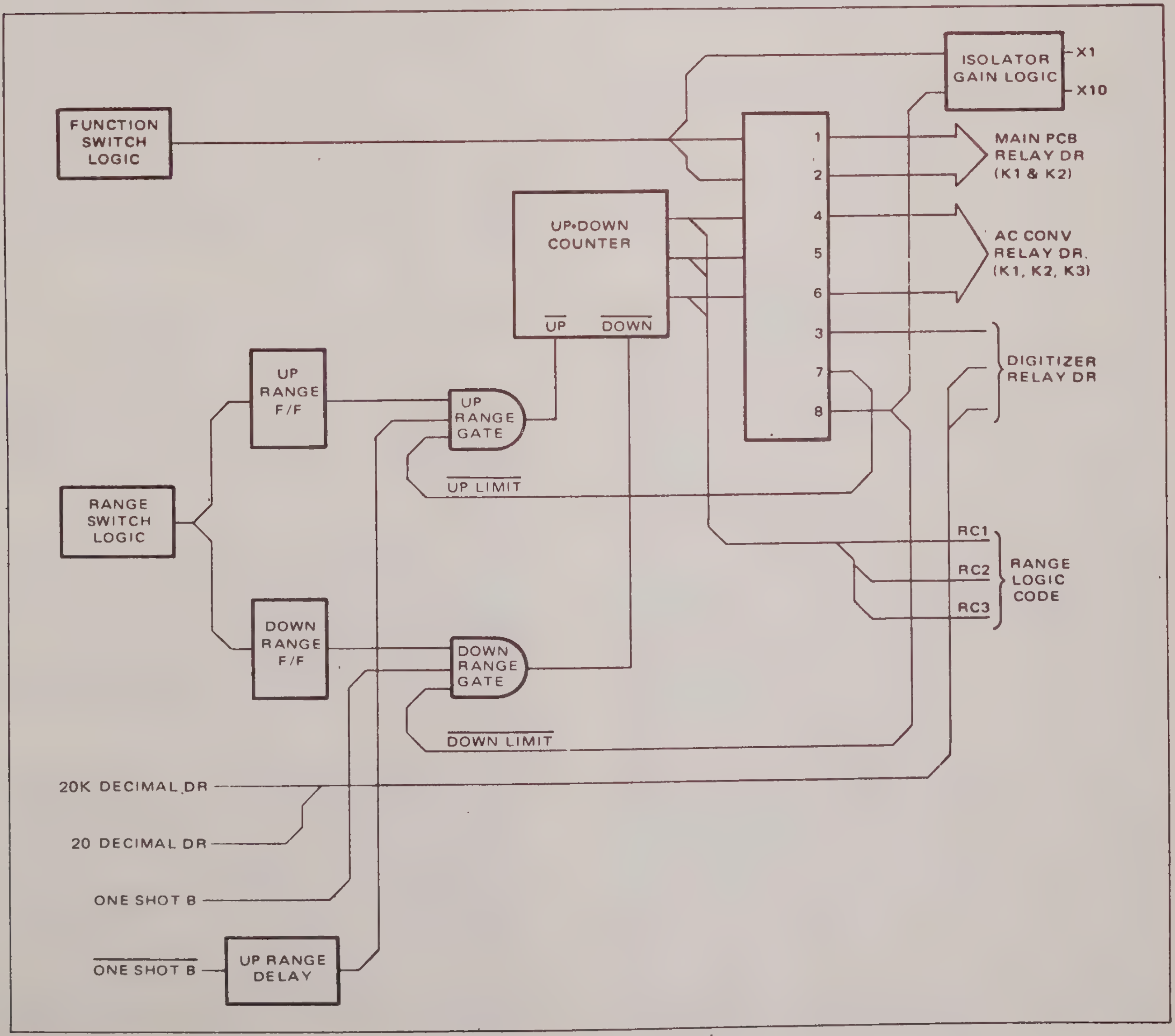

FUNCTION SWITCH LOGIC
ISOLATOR GAIN LOGIC
X1
X10
1
2
4
5
6
3
7
8
MAIN PCB RELAY DR (K1 & K2)
UP•DOWN COUNTER
UP
DOWN
AC CONV RELAY DR. (K1, K2, K3)
DIGITIZER RELAY DR
UP RANGE F/F
UP RANGE GATE
UP LIMIT
RANGE SWITCH LOGIC
RC1
RC2
RC3
RANGE LOGIC CODE
DOWN RANGE F/F
DOWN RANGE GATE
DOWN LIMIT
20K DECIMAL DR
20 DECIMAL DR
ONE SHOT B
ONE SHOT B
UP RANGE DELAY

Figure 4.5 - Function and Range Logic

front panel pushbuttons labeled AC Volts, DC Volts, Kohms, and kHz. Note that there are two sets of input terminals for applying measurement signals to the input of the instrument. One set is used to provide the full scale current for resistance measurements and the other set of input terminals is used for measuring dc volts, ac volts, Kohms and kHz. The four function control switches route the input measurement signal through one of three paths when making a measurement of either voltage. The measurement signal is routed from one set of input terminals to the input of the AC Converter. When making dc voltage measurements, the measurement signal is applied to the input of the isolator and, in like fashion, the ohms measurement signal is routed to the input of the ohms circuits. Although the block diagram shows that the measurement signal is applied to the input of one of these three circuits, measurement signals are actually routed through the voltage attenuator circuits for prescaling purposes. This is discussed in more detail in the following paragraph.

J101 – +IN ACV DCV kHz (KΩ with addition of J103)
J102 – –IN ACV DCV kHz (KΩ with addition of J104)
J103 – KΩ (with J101)
J104 – KΩ (with J102)
J105 – GUARD to be connected to J102 for all measurements except floating inputs

4.3.4 Range Control Logic.

4.3.4.1 The range control logic is illustrated in simplified form in figure 4.5. The range control circuits control the gain of the isolator, the attenuation in the AC Converter and in the voltage circuits. In addition, the range control circuits provide a range code to the decimal decoder for positioning of the decimal point on the front panel display. The heart of the range control circuits is the range counter, a three state UP/DOWN counter controlled by a pair of UP/DOWN flip-flops. When the range is to be stepped up manually, the switch closure from S8-B in combination with the clock, applies a pulse to the UP input of the range counter, thereby increasing the count. Manual down ranging is accomplished in exactly the same way by a switch closure from S9-A when the DOWN pushbutton is depressed. In auto range, the same UP or DOWN flip-flops are set by two signals which come from the counter. If the counter reaches a count which is greater than full scale of the measurement range prior to the null detect, it produces an overload (O/L) signal. This signal is applied to the step-up flip-flop and causes the range counter to step up one count. If the null detect signal should occur before the counter reaches the 5% point in its count, a signal termed divide by 2K (÷ 2K) is produced, indicating that the measurement is less than 5% of full scale. This divide by 2K signal is applied to the step-down flip-flop, which causes the range counter to count down one step. Thus, the manual pushbuttons, or the internal logic, cause the range counter to step to the proper range and produce the range codes RC1, RC2, and RC3. The range code is applied to the decimal decoder to locate the decimal point on the front panel display. In addition, the range codes are applied to the read-only memory (ROM), which is configured by internal firmware, to produce relay control signals which configure the attenuator relays. The isolator gain is controlled by the range counter, read-only memory, and by the switch positions of the function control switches on the front panel.

4.3.5 AC Converter (Averaging).

4.3.5.1 The AC Converter is shown in simplified form in figure 4.6. As shown on the diagram, it consists of an input attenuator network, a rectifier amplifier, and an output filter. The input attenuator network serves to scale down the input measurement voltage, controlled by the range relays K1, K2, and K3. The 2V range attenuation is controlled by the fixed R/C values of the input circuit and the input voltage is applied directly to the rectifier amplifier. On the 20, 200, and 1000 ranges, relays K1, K2, and K3 are respectively energized to provide the proper signal input attenuation. The ACV Function configures the isolator for a fixed gain of 1 for all ranges. The rectifier amplifier consists of a dual FET input stage that feeds an operational amplifier that drives a G_m stage and two rectifier feedback diodes that convert the input measurement signal to a dc voltage, which is smoothed by an output filter network.

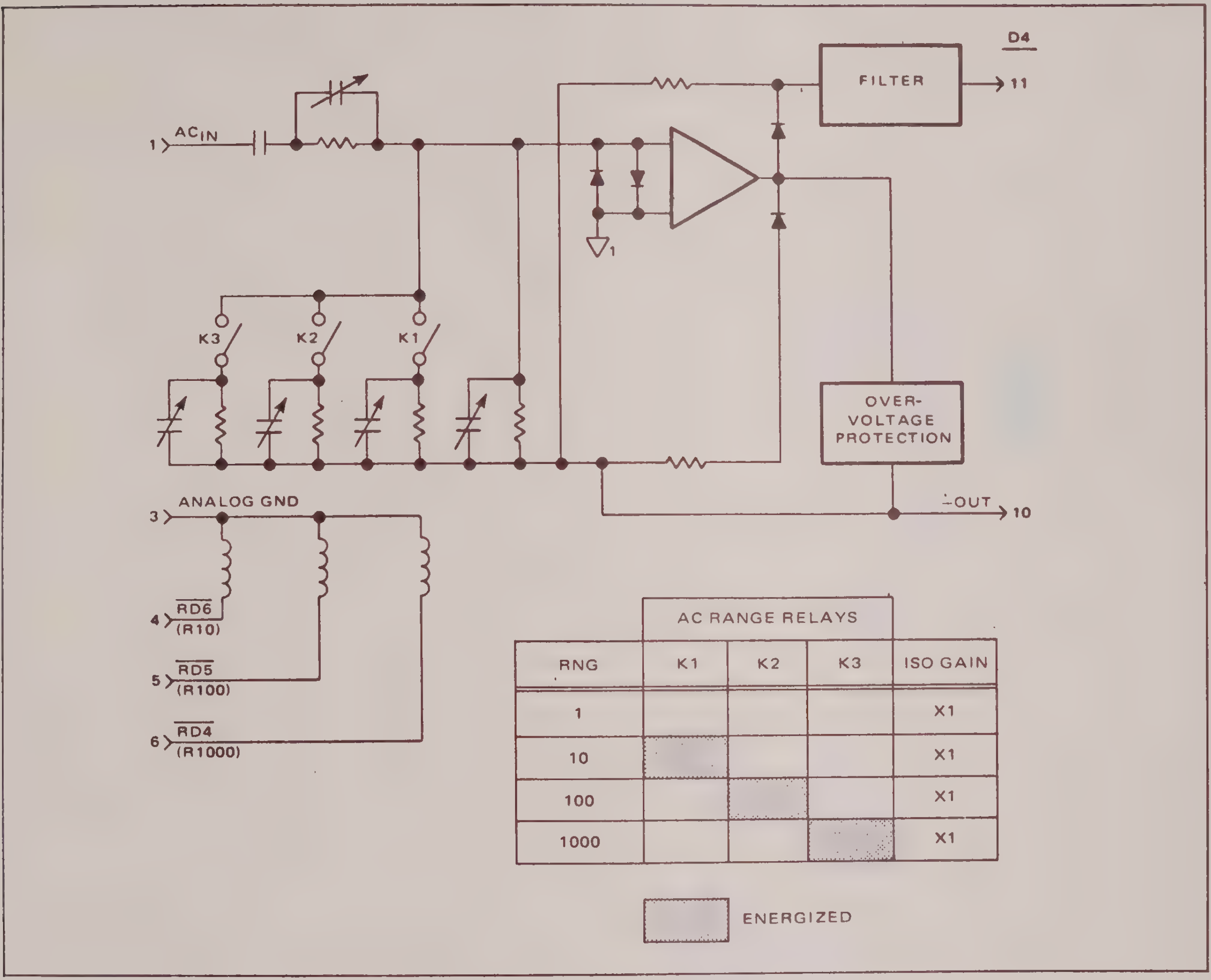
4.3.6 TRUE RMS AC CONVERTER.

4.3.6.1 The converter is shown in simplified form in figure 4.7. It consists of an input scaling attenuator amplifier, an absolute value taker rectifier amplifier, a logarithmic driving amplifier, an anti-log summing amplifier, an output attenuator, and filter.

4.3.6.2 The input scaling amplifier receives an input signal, de-coupled through C1, to the fixed R/C values in a potentiometric configuration with a gain of 1 for the 2 ACV range. The attenuator relay combinations reduce the overall gain by decade factors, as shown in figure 4.7. Transistors Q2 and Q3 are wired as back-to-back clamp diodes to protect the input to the OP AMP, AR1.

4.3.6.3 The output of the scaling amplifier is fed to the Absolute Value taker (AVT) or rectifier amplifier. This circuit consists of an OP AMP, AR2, feeding an output G_m stage (Q8 and Q9) used to drive the hot carrier rectifier diodes (CR8 and CR9) and their feedback components in a unity gain, inverting configuration. The output produces a +50 μA/Volt to the input of the LOG driving amplifier.

4.3.6.4 The LOG Amplifier drives four log transistors (Q4a, Q5a, Q4b, and Q5b) whose emitter currents are



	AC RANGE RELAYS			
RNG	K1	K2	K3	ISO GAIN
1				X1
10	▨			X1
100		▨		X1
1000			▨	X1

▨ ENERGIZED

Figure 4.6 - Averaging AC Converter

matched to provide temperature tracking. Q7 is a differential stage driving the emitter follower, Q10, that drives Q11. At high frequencies C20 and R37 shunt the drive signal of Q10 to ground and the main signal is through Q11 by way of C16. Q6 is a dynamic load for the differential stage, Q7, and CR10 produces a diode drop to help compensate for voltage drift. R32 adjusts voltage offset and R22 adjusts the input bias current.

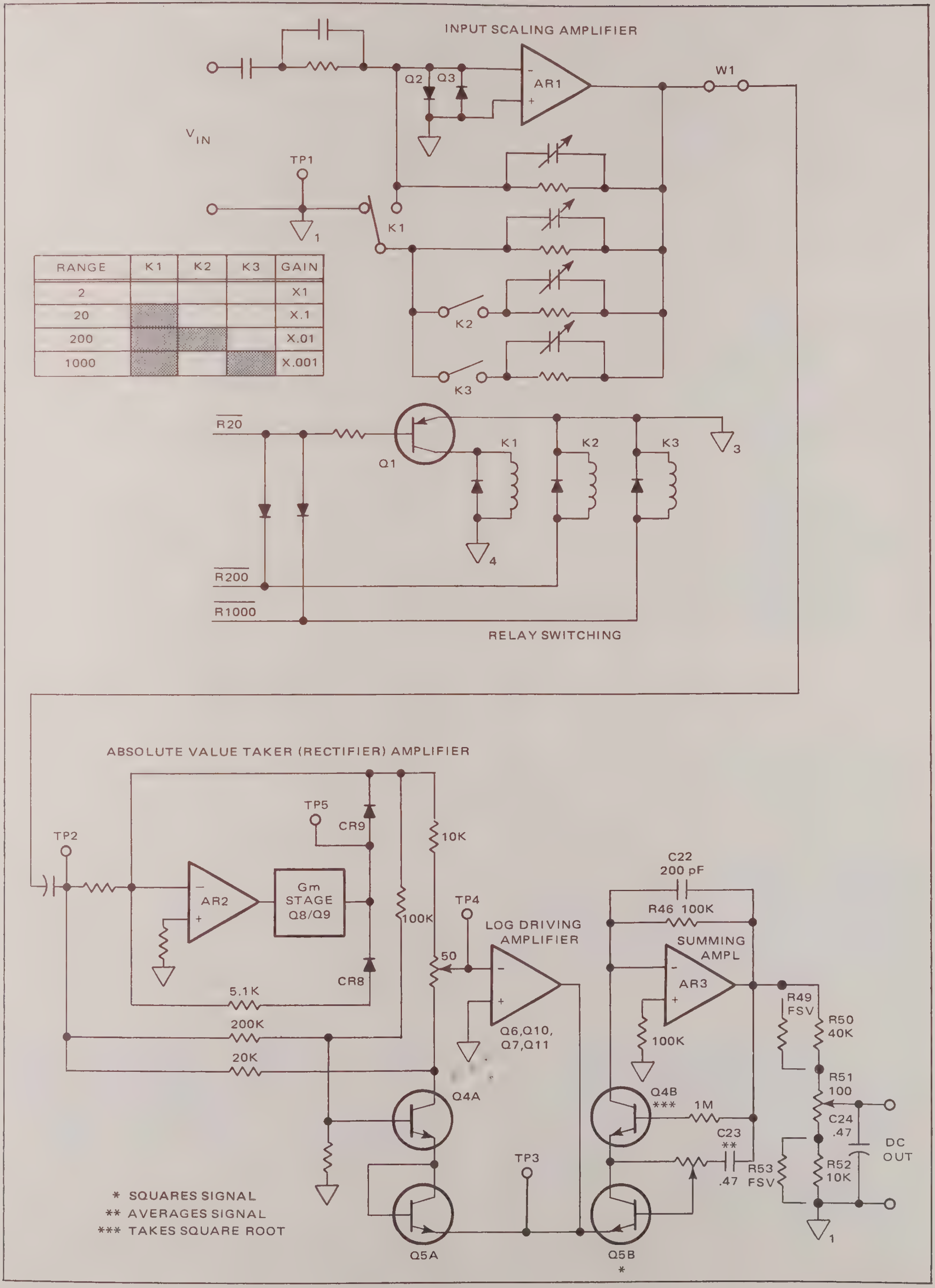
4.3.6.5 The output of the LOG amplifier is a negative current that drives Q5b, which squares the signal. C23 averages the signal by the small amount of ripple from the output of the Summing OP AMP, AR3, to the log transistors. Q4b extracts the square root of the signal and this is fed to the inverting input of the Summing OP AMP, where the current is converted to a voltage at the output by R46. C22 is used to provide phase compensation. The output of the summing amplifier produces a full scale signal of +10 Volts. This is attenuated by R50 and R52 (R49 and R53 are FSV's if necessary) and filtered by C24 to be routed to the isolator, set at a gain of 1.

4.3.7 High Voltage Buffer.

4.3.7.1 The high voltage buffer is illustrated in simplified form in figure 4.8. This circuit protects the isolator from high measurement voltages, presents a high impedance to the measurement circuit to prevent circuit loading and isolates the KΩ source terminal from the attenuator reference bridge on all KΩ ranges.

4.3.7.2 In operation, the two transistors (diode connected) Q1 and Q2, serve as an input clamp to prevent application of excessive voltage to the high impedance buffer Q4. The high impedance buffer is a dual FET device configured with the amplifier AR1 to form a unity gain amplifier of extremely high impedance.

4.3.7.3 The output of the AR1 is routed through the 1000 KΩ resistor to the attenuator and from the attenuator output to the isolator.


INPUT SCALING AMPLIFIER
W1
Q2
Q3
AR1
VIN
TP1
K1
K2
K3
R20
Q1
K1
K2
K3
3
4
1
R200
R1000
RELAY SWITCHING
ABSOLUTE VALUE TAKER (RECTIFIER) AMPLIFIER
TP2
TP5
CR9
10K
AR2
Gm STAGE Q8/Q9
100K
CR8
5.1K
200K
20K
TP4
50
LOG DRIVING AMPLIFIER
Q6,Q10, Q7,Q11
C22 200 pF
R46 100K
SUMMING AMPL
AR3
100K
R49 FSV
R50 40K
R51 100
C24 .47
DC OUT
Q4A
Q4B ***
1M
C23 **
.47
R53 FSV
R52 10K
TP3
Q5A
Q5B *
* SQUARES SIGNAL
** AVERAGES SIGNAL
*** TAKES SQUARE ROOT

RANGE	K1	K2	K3	GAIN
2				X1
20	▨			X.1
200	▨	▨		X.01
1000	▨		▨	X.001

Figure 4.7 - True RMS AC Converter, Simplified Schematic

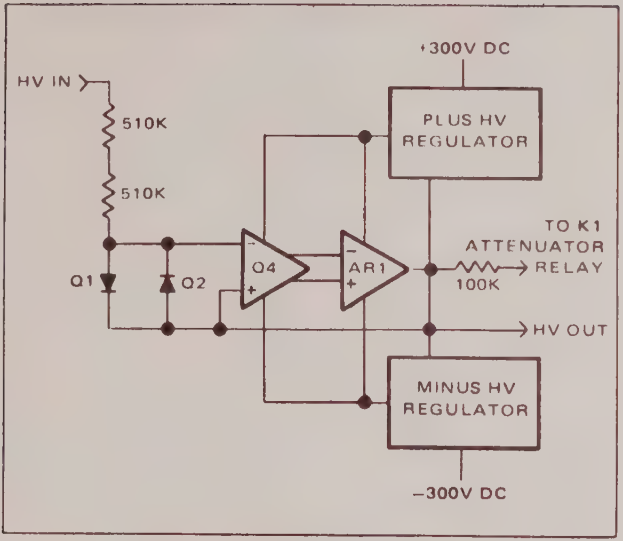

+300V DC
HV IN
510K
510K
PLUS HV REGULATOR
Q1
Q2
Q4
AR1
TO K1 ATTENUATOR RELAY
100K
HV OUT
MINUS HV REGULATOR
−300V DC

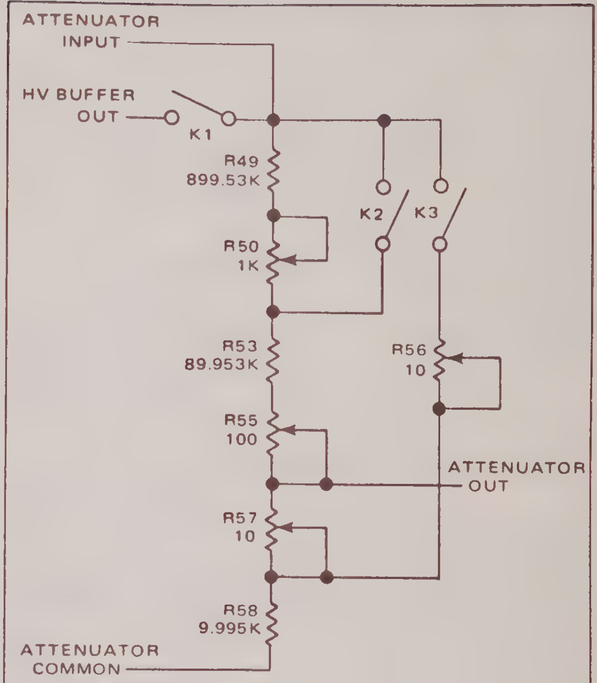
Figure 4.8 - High Voltage Buffer

4.3.7.4 In the Kohms function, the output of the AR1 is routed to the reference common line (refer to figure 5.16, KΩ Single Thread Diagram, upper right quadrant). The output of the high voltage buffer AR1 raises the reference common voltage as current is drawn from the ohms source terminal so that the current flow is constant through the resistance being measured (Rx).

4.3.8 Attenuator.

4.3.8.1 This circuit is shown in simplified form in figure 4.9. The attenuator performs the following functions; 1) attenuation of input measurement voltages on the 20, 200, and 1000 volt dc ranges, 2) scales down the ohms current source when the instrument is on the Kohms ranges, and 3) the attenuator contains a series resistance string with pick-off points selected by range relays. The attenuator, in the 20, and 200 DCV ranges, divide the HV Buffer output by 10:1 and 100:1, respectively, to provide full scale inputs to the isolator of ±2V DC. The attenuator, for the 1000 range, is preceded by a 9 MΩ resistor on the main PCB to provide a 1000:1 reduction in voltage from the measurement input to the isolator input.

4.3.8.2 When configured in the KΩ ranges, the attenuator uses the resistor elements in series with the KΩ reference generator voltage (+10V DC) to provide the required full scale currents at the KΩ source input terminal, J103. The 9 MΩ main PCB resistor is configured with the attenuator and HV Buffer in the 2000 KΩ and 20,000 KΩ ranges.


ATTENUATOR INPUT
HV BUFFER OUT
K1
R49 899.53K
K2
K3
R50 1K
R53 89.953K
R56 10
R55 100
ATTENUATOR OUT
R57 10
R58 9.995K
ATTENUATOR COMMON

	KΩ			DCV		
RNG	K1	K2	K3	K1	K2	K3
.2			▨			
2			▨			
20		▨			▨	
200						
2000						
20000	▨					

▨ ENERGIZED

Figure 4.9 - Attenuator

4.3.9 Isolator.

4.3.9.1 The isolator, shown in figure 4.10, consists of an input clamp, an isolator amplifier, a bootstrap amplifier, and a gain switching network. The various prescaled and processed input measurement voltages are applied to the input of the isolator which is clamped to prevent application of more than ±5V to the input of the isolator amplifier. The isolator amplifier is an operational amplifier with a

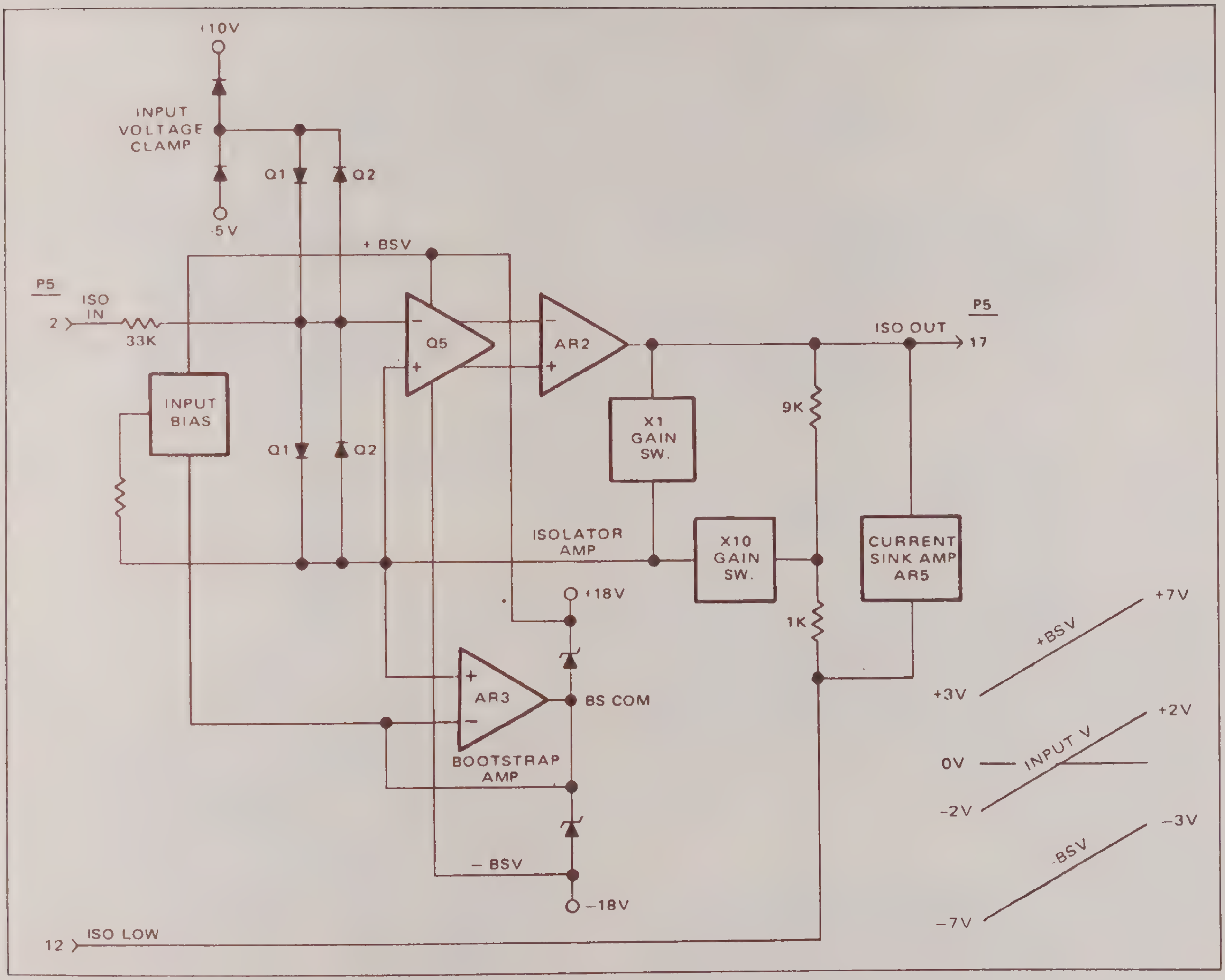

+10V
INPUT VOLTAGE CLAMP
Q1
Q2
-5V
+ BSV
P5
ISO IN
2
33K
Q5
AR2
P5
ISO OUT
17
INPUT BIAS
Q1
Q2
X1 GAIN SW.
9K
ISOLATOR AMP
X10 GAIN SW.
CURRENT SINK AMP AR5
+18V
+7V
+BSV
1K
+3V
AR3
BS COM
BOOTSTRAP AMP
+2V
0V
INPUT V
-2V
-3V
-BSV
− BSV
−18V
−7V
ISO LOW
12

Figure 4.10 - Isolator & Bootstrap

gain of 1 or a gain of 10, depending upon the control signals applied to the gain switches by the range control logic of the instrument. The isolator accepts either positive or negative voltage levels at its input on one of two ranges; 1) zero to .1999 volts or 2) zero to 1.99 volts. Because of the gain switching, controlled by the range control logic, the output of the isolator is always zero to 1.999 volts dc. Note that the negative and positive supply voltage for the isolator amplifier is supplied by the bootstrap amplifier. These voltage sources are labeled + bootstrap voltage (+ BSV) and − bootstrap voltage (− BSV). The purpose of the bootstrap amplifier is to provide the isolator amplifier with a supply voltage which is always centered about the input measurement signal to the isolator amplifier. The + BSV voltage is always 5 volts higher than the input signal and the − BSV is always 5 volts lower than the input signal voltage. Thus, the isolator amplifier is always supplied with source voltages centered around the input signal. This combination provides high input impedance to avoid loading the circuit under test. The Current Sink AMP circuit, at the output of the isolator, provides a voltage, i.e., current, equal and opposite to the isolator output. This effectively raises the input impedance of the signal "low" input terminal by cancelling the effects of signal current errors from the measurement input to the integrator.

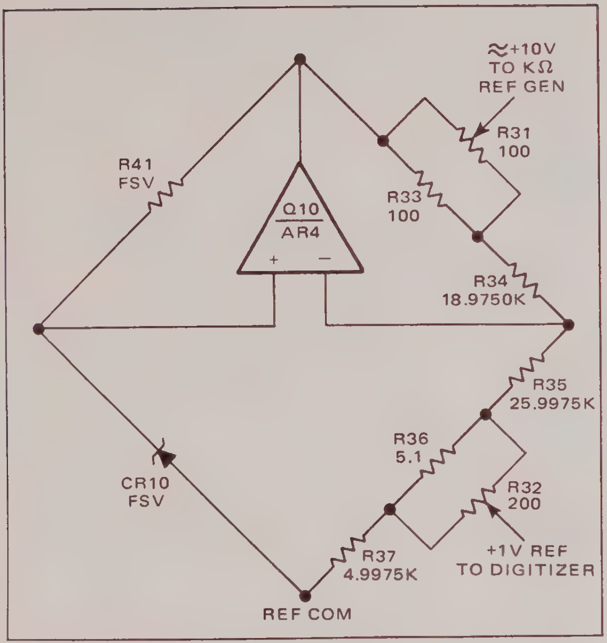


Figure 4.11 - Reference Generator

4.3.10 Reference Generator.

4.3.10.1 The reference generator produces the accurate one-volt to the digitizer circuits for measurement of AC and DC voltages. It also furnishes a 10 volt reference voltage to ohms reference circuit for use in the ohms measurement functions. The reference generator is shown in simplified schematic form in figure 4.11 and in complete schematic form on sheet 2 of drawing number 432074, page 6-13.

4.3.10.2 The circuit consists of a resistance bridge, an operational amplifier, transistor Q10, and reference zener CR10.

4.3.10.3 In operation the zener presents approximately 6.3 volts at the – input of AR4 maintaining a stable 10 volt DC output at Q10. The resistor network around CR10 consisting of resistors R39, R40, R41, R42, R45, R46, R50, and R51 is designed to operate the reference zener at a current which produces the highest voltage stability over a wide temperature range. These resistors are factory-selected-value (FSV) resistors and the schematic shows only nominal values. In addition, some of the resistors may not be installed in some instruments.

4.3.10.4 The resistance bridge contains two potentiometers for adjusting the one volt and 10 volt output voltages.

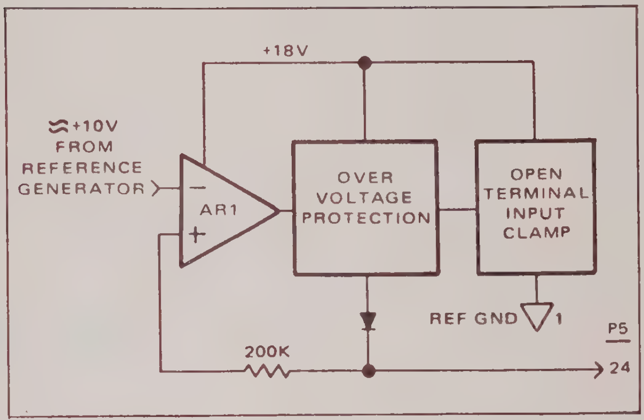


Figure 4.12 - KΩ Reference Generator

4.3.11 KΩ Reference Generator and Overvoltage Protection Circuit.

4.3.11.1 The KΩ reference generator provides a stable 10 volt reference voltage for application to the ohms source terminal via the attenuator circuit. The circuit is shown in simplified form in figure 4.12 and schematically on sheet 2 of drawing 432074, page 6-13. The circuit consists of an operational amplifier, a five-volt zener diode, driver transistor Q4 and protection diode, CR3. When supply voltages are applied to the circuit the overvoltage circuit rises to +10 volts. At this point the op-amp AR1 biases Q4 so that the collector remains at 10 volts. As current is drawn during a resistance measurement the op-amp adjusts the bias so the output of Q4 remains at 10 volts under load. Thus the ohms reference voltage is held stable and the reference circuit is isolated from the ohms load. The overvoltage protection circuit is included to protect the instrument from accidental application of voltage while set for KΩ function.

4.3.12 Open Input Terminal Clamp.

4.3.12.1 When there is no connection to the input terminals on the KΩ function, the +10 volt reference line and reference common would tend to soar to the level of the power sources. To limit the drift Q9 and Q6 are biased to turn on and clamp these lines. This keeps the voltage on the test leads at a safe level and protects the components in a circuit under test.

4.3.13 Integrator.

4.3.13.1 The integrator is the circuit which performs the analog-to-digital conversion of the measurement signal and is illustrated in figure 4.13. The integrator uses the dual

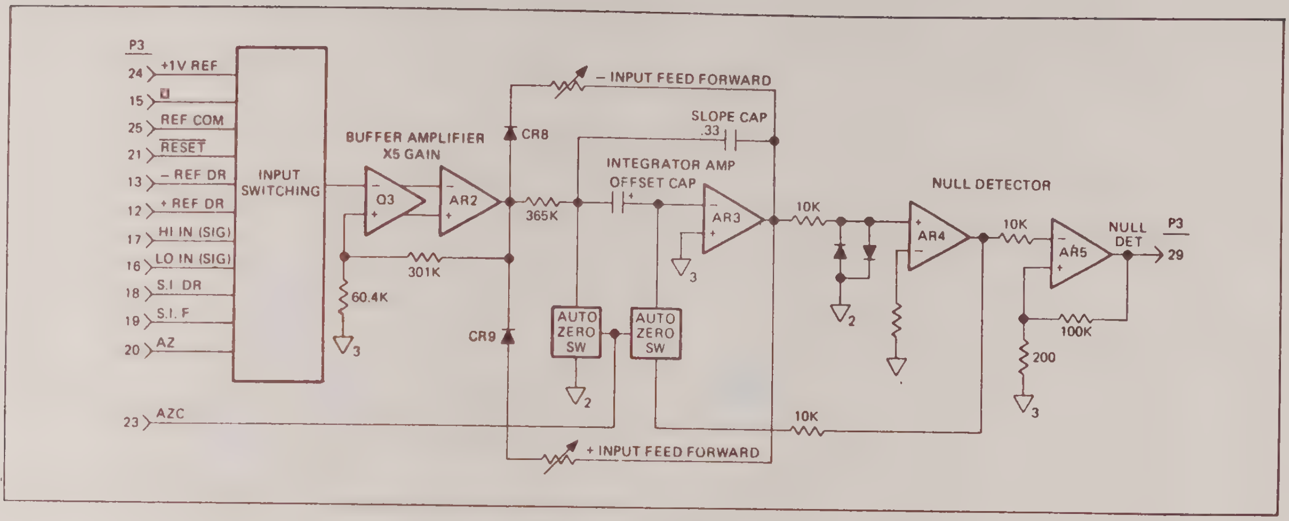
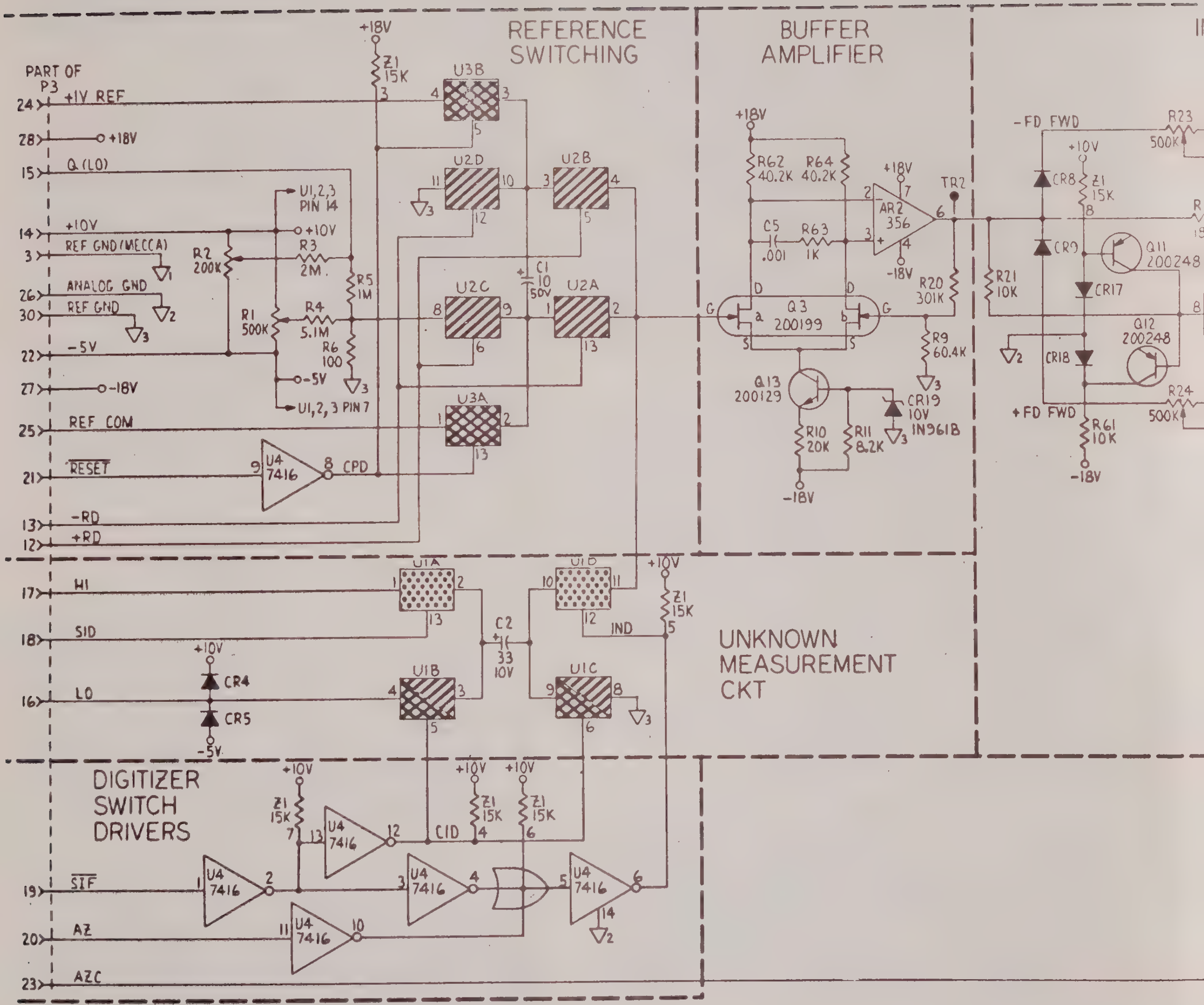


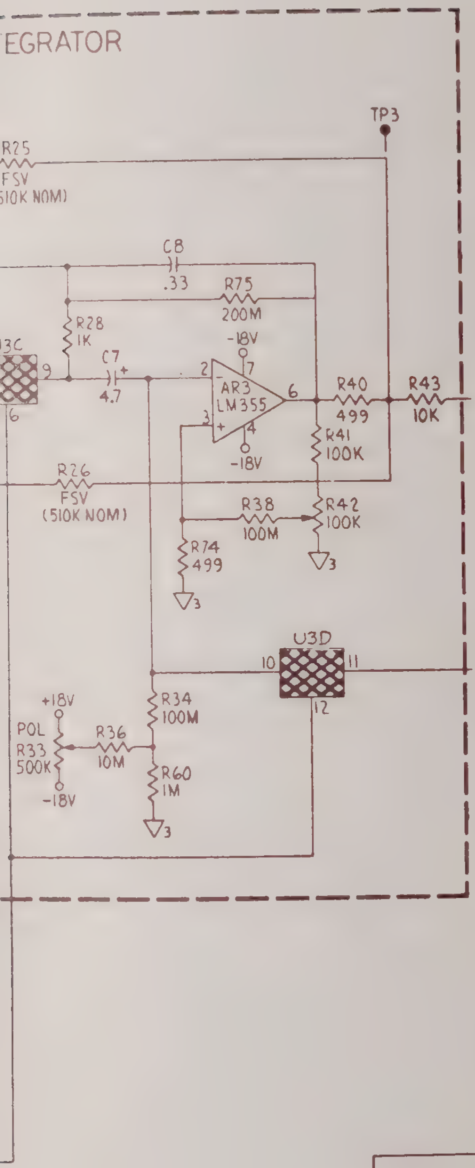
Figure 4.13 - Digitizer

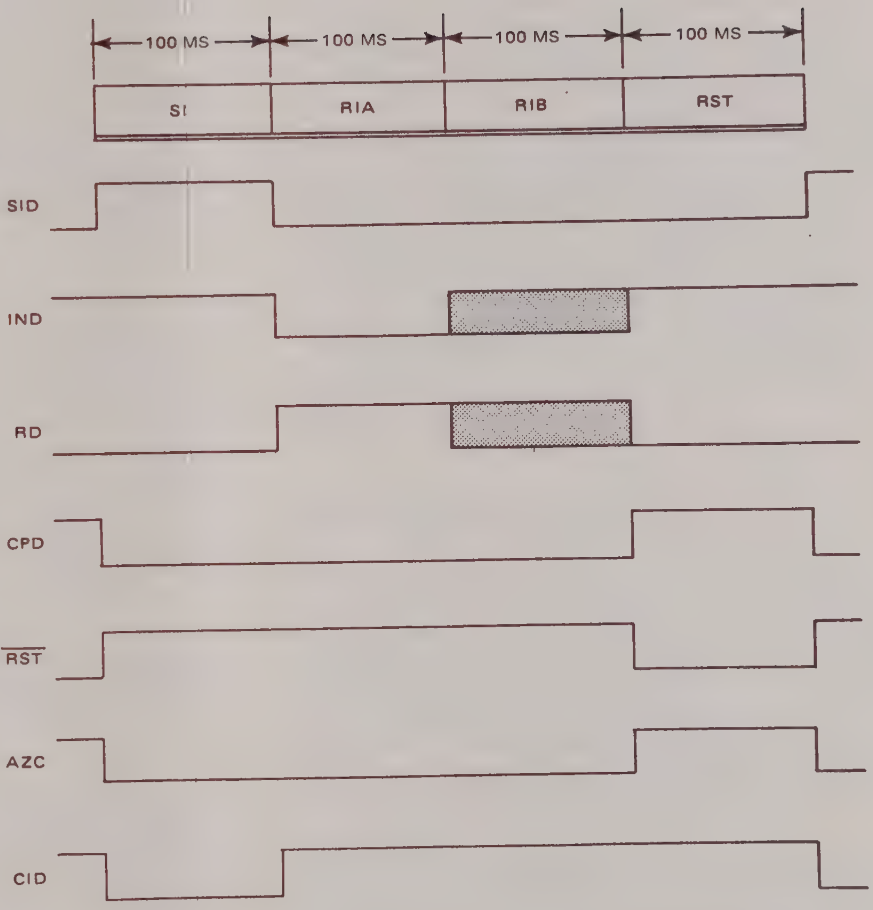
slope integration technique to perform the analog-to-digital conversion. Refer to figure 4.2 for the cycle timing relationships that relate to the dual slope integration. During the reset portion of the measurement cycle, the two reset switches close placing the offset capacitor across the output of the null detector amplifier. This charges the offset capacitor to a level equal to any offset voltage that appears at the output of the null detector amplifier. At the beginning of the signal integrate portion of the measurement cycle, the reset switches open and the signal switch closes, thus placing the offset capacitor in series with the measurement signal from the isolator at the input of the integrator amplifier. Thus a positive or negative offset voltage is added to or subtracted from the signal being measured. The output of the integrator amplifier charges the slope capacitor for a fixed period of time (100 milliseconds). The charge placed on the capacitor is dependent on the magnitude or level of the measurement signal from the isolator. Refer to figure 4.2, note that there are two slopes shown representing the capacitor charging slope; these represent two measurement levels. Note that the time is the same for the charge for both measurements but that the charging rate and the final charge level is different. From this it can be seen that the signal integrate period is always the same length but the charging rate and level of the capacitor varies with the measurement signal. At the end of the signal integrate period the feed forward switch adds a small amount of charge to the capacitor to make up for a slight delay which is incorporated to allow similar lines and circuits to settle out between the reference integrate and signal integrate portions of the measurement cycle. This causes the slope capacitor charge voltage to increase slightly. At the beginning of the reference integrate period of the measurement cycle, the signal switch opens and either the -- reference switch or the + reference switch closes to apply a reference voltage to the input of the integrator amplifier opposite in polarity to the voltage of the measurement signal previously applied. This reference voltage is applied to the integrator amplifier and causes the slope capacitor to discharge at a fixed rate. When the slope capacitor reaches the zero level, the null detector amplifier produces a null detect pulse. Note that in figure 4.2 that for both measurements, the rate of discharge was the same, e.g., the slope is the same angle. Also note that for different measurement signal inputs, the zero crossing occurs at a different point in time. Thus, it can be seen that the time periods of the reference integrate portion of the measurement cycle is proportional to the value of the measurement signal. The output of the null detector is used by the Timing and Control circuits to stop the measurement counter. On figure 4.2 the Q_{e1} and Q_{e2} signals shown are timing signals generated by the measurement counter chip and used by the Timing and Control circuits for circuit synchronization and generation of control signals.

4.3.13.2 INTEGRATOR INPUT SWITCHING.

4.3.13.2.1 The A-to-D process called integration requires that the measurement signal from the isolator output, which has been conditioned (filtered, amplified, or attenuated), to be applied to the input of the integrator, whose R/C components allow the output to charge at a linear rate for


REFERENCE SWITCHING
BUFFER AMPLIFIER
UNKNOWN MEASUREMENT CKT
DIGITIZER SWITCH DRIVERS
PART OF P3
24 +1V REF
28 +18V
15 Q (LO)
14 +10V
3 REF GND (MECCA)
26 ANALOG GND
30 REF GND
22 -5V
27 -18V
25 REF COM
21 RESET
13 -RD
12 +RD
17 HI
18 SID
16 LO
19 SIF
20 AZ
23 AZC
U1,2,3 PIN 14
U1,2,3 PIN 7
R2 200K
R3 2M
R1 500K
R4 5.1M
R5 1M
R6 100
Z1 15K
U3B
U2D
U2B
U2C
U2A
U3A
C1 10 50V
U4 7416
CPD
+18V
R62 40.2K
R64 40.2K
C5 .001
R63 1K
AR2 356
TR2
Q3 200199
R20 301K
R9 60.4K
Q13 200129
R10 20K
R11 8.2K
CR19 10V 1N961B
-18V
-FD FWD
R23 500K
+10V
CR8
CR9
Q11 200248
CR17
R21 10K
Q12 200248
CR18
R24 500K
+FD FWD
R61 10K
U1A
U1D
U1B
U1C
C2 33 10V
IND
CR4
CR5
CID


EGRATOR
TP3
R25
FSV
510K NOM)
C8
.33
R75
200M
R28
1K
-18V
3C
9
C7
4.7
2
7
AR3
LM355
6
3
4
-18V
R40
499
R43
10K
R41
100K
6
R26
FSV
(510K NOM)
R38
100M
R42
100K
R74
499
3
3
3
U3D
10
11
12
+18V
POL
R33
500K
-18V
R36
10M
R34
100M
R60
1M
3


100 MS
100 MS
100 MS
100 MS
SI
RIA
RIB
RST
SID
IND
RD
CPD
RST
AZC
CID

SWITCH		░	▨	▨	▩
U1-13	SID	▒			
U1-12	IND	▒			
U2-5/6	+ RD		▒	▒	
U2-12/13	– RD		▒	▒	
U3-5/13	CPD				▒
U3-6/12	AZC				▒
U1-5/6	CID		▒	▒	▒

Figure 4.14 - Integrator Input Switching

100 msec, called signal integration. The process now disconnects the measurement signal and applies a stable reference voltage opposite in polarity (of the measurement signal) to return the integrator output back to a zero voltage, to be sensed by the null detector as "zero crossing," called reference integration. The reference integration period is approximately 100 μsec for zero input signal, 100 ms for half scale signals (100,000 counts) and 200 msec for full scale signals (199,999 counts). A period of 100 msec follows the reference integration period called "reset." During the Reset period, the +1V Reference Voltage from the Reference Generator is applied to a 10 μF/50V capacitor (C1) by COS/MOS bilateral switches to store the Ref +1V until use during the reference integration period. The drive signal for this sequence is called CPD or inverted Reset from the Timing and Control circuitry on the main PCB.

4.3.13.2.2 At the start of the Reference integration period, the Voltage stored on C1 must be applied to the integrator. If the measurement signal were plus, a −1 volt Reference must be used to complete the integration sequence. This is accomplished by use of COS/MOS bilateral switch configurations that reference C1 "+" to (Mecca) ground and connect C1 "−" to the integrator input. The drive signal required during the reference integrate sequence is "−" RD from the Timing and Control logic circuits on the main PCB, which was established by the polarity detection circuits during the start of signal integration.

4.3.13.2.3 Measuring a negative signal requires that a positive reference voltage be configured during reference integration by a drive signal called "+" RD.

4.3.13.2.4 The capacitor is used to store a voltage potential at Reset to be used, either positively or negatively, during the following reference integrate period. The "store" to "use" period, signal integrate, is 100 msec which, because of the high COS/MOS "OFF" resistance, does not "load" and/or derate the voltage on the capacitor. Following the reference integrate period is Reset which again "charges" or "refills" the capacitor should any de-rating of the reference +1V occur.

The measurement signal, from the isolator output, is coupled to the integrator input through a configuration of COS/MOS bilateral switches and a measurement capacitor, C2. During the reset period, before signal integrate, the input to the integrator and C2 "−" are connected to (Mecca) ground while C2 "+" is connected to isolator "low" which removes any residual charge on the measurement cap. At the start of signal integration, C2 "−" is released from (Mecca) ground; C2 "+" is released from isolator output low and switched to isolator output high that places a measurement voltage on the integrator input to start a positive or negative output slope for the next 100 msec.

4.3.13.3 BUFFER AMPLIFIER.

4.3.13.3.1 The maximum measurement signal that can be resolved is ±2 volts while the reference voltage is ±1 volt. For the integrator to perform properly, a higher voltage is required by the integrator circuit to produce a slope with more velocity to prevent false triggering (at low level signals) and provide a more defined reference slope to detect zero or null. An amplifier with a gain factor of 5 is used to interface the input switching circuits and the actual integration amplifier circuit. With the gain as a constant, it applies to both the measurement signal for the signal integrate period and for the reference voltage during the reference integration sequence. It consists of a discrete dual FET input stage with a constant current generator, an operational amplifier, and the resistor values to achieve the required gain (x5).

4.3.14 Timing & Control Circuit.

4.3.14.1 Operation of the 5100 is controlled by the Timing and Control circuits (figure 4.15, block diagram). These circuits provide synchronization and control signals which control the sequence of operation referred to as the measurement cycle. Figure 4.2 illustrates the measurement cycle timing. Note that the timing waveforms in the left portion of the figure illustrate timing and polarities for a positive measurement signal while the right portion illustrates the negative input example.

4.3.14.2 The differences between the left and right portions of the figure are the polarity of the input signal, the integrator slope and polarity, the timing of signal switch, reference switch and reset switch. The following description of the operation of the timing and control circuits refers to the simplified block diagram (figure 4.15) and the timing chart (figure 4.2).

4.3.14.3 Four timing events are established by the CMOS chip, 3814 counter, U10 on the main PCB. Since the 3814 counter only has the capability of resolving a 4-1/2 display an additional counter is used between the clock circuit and the 3814 counter to provide the least significant digit (LSD) for a total of 5-1/2 full digits on the readout PCB. An internal clock frequency of 1 MHz drives the LSD counter, whose output of 100 kHz is fed to the 3814 counter. The

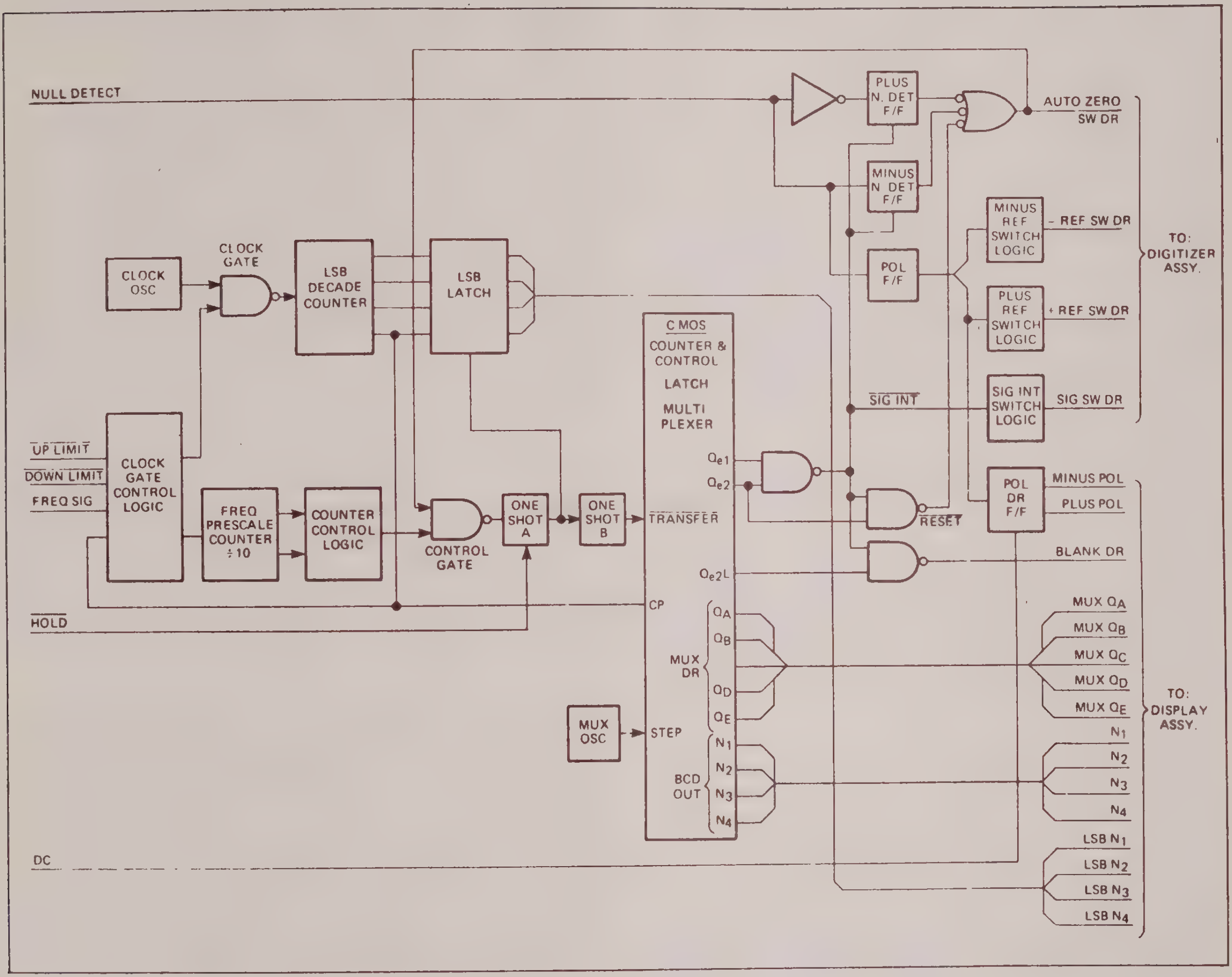

NULL DETECT
PLUS N. DET F/F
MINUS N. DET F/F
AUTO ZERO SW DR
MINUS REF SWITCH LOGIC
- REF SW DR
TO: DIGITIZER ASSY.
POL F/F
PLUS REF SWITCH LOGIC
+ REF SW DR
SIG INT
SIG INT SWITCH LOGIC
SIG SW DR
CLOCK OSC
CLOCK GATE
LSB DECADE COUNTER
LSB LATCH
C MOS COUNTER & CONTROL LATCH MULTI PLEXER
UP LIMIT
DOWN LIMIT
FREQ SIG
CLOCK GATE CONTROL LOGIC
FREQ PRESCALE COUNTER ÷10
COUNTER CONTROL LOGIC
CONTROL GATE
ONE SHOT A
ONE SHOT B
TRANSFER
Qe1
Qe2
Qe2L
RESET
POL DR F/F
MINUS POL
PLUS POL
BLANK DR
HOLD
CP
QA
QB
QD
QE
MUX DR
MUX QA
MUX QB
MUX QC
MUX QD
MUX QE
TO: DISPLAY ASSY.
MUX OSC
STEP
BCD OUT
N1
N2
N3
N4
LSB N1
LSB N2
LSB N3
LSB N4
DC

Figure 4.15 - Timing and Control

3814's 1/2 digit counter has two outputs, Q_{e1} and Q_{e2}, that establish four timing events of 100 msec each that will be used to convert (digitize) an analog expression into its digital equivalent. The timing sequences are as follows:

$Q_{e1} = 1, Q_{e2} = 1$
100 msec, counts from 300,000 to 399,999 called Signal Integrate

$Q_{e1} = 0, Q_{e2} = 0$
100 msec, counts from 000,000 to 099,999 called Reference Integrate. This count total is referred to as half scale

$Q_{e1} = 1, Q_{e2} = 0$
100 msec, counts from 100,000 to 199,999 also called Reference Integrate. This count total is referred to as full scale

$Q_{e1} = 0, Q_{e2} = 1$
100 msec, counts from 200,000 to 299,999 called reset (FIXED)

4.3.14.4 In the following example a +1.0V DC input signal is applied to the isolator amplifier input. The isolator, at a gain of 1, has an output of +1.0V DC. When the signal integrate period is detected, this +1.0V DC is coupled to the Buffer/Integrator by the configuration of the bilateral switches and measurement cap of the input switching circuit resulting in a negative going slope at the integrator output of approximately −5.0V at the end of the 100 msec period. The null detector senses the negative slope voltage and causes its output to go to a positive TTL level to be applied to U16-2, the D input of the polarity F/F. This causes U16-5, the Q output to be logic high, which when applied to the D input of the Polarity Drive F/F, U16-12, causes the $\overline{Q}$ output, U16-8 to be logic low to annunciate the "plus" symbol on the readout.

4.3.14.5 At the start of the signal integrate period, the outputs of U13-6 and U6-12, $\overline{\text{Signal Integrate}}$, go logic low. The low level of U6-12 is applied to the "clear" inputs, pin 1 and 13 of U15, that cause the $\overline{Q}$ outputs, pin 6 and 8, to go logic high to be applied to U14, pins 1 and 2 respectively. $\overline{\text{Signal Integrate}}$ at a logic low causes the output of U13-11, $\overline{\text{Reset}}$, to go logic high, which is also applied to U14 at pin 13, which results in the output U14-12 to be logic low called "internal reset" or auto zero (AZ). The counter control F/F $\overline{Q}$ output of U9-6 goes logic high at the start of reference integration, arming the input to the gate at U8-5. When the null detector senses zero, "internal reset" will go logic high at U8-4, causing a falling edge at U8-6 to trigger one-shot A to transfer the BCD count in the LSD counter, U3, into the LSD latch, U7. The $\overline{Q}$ output of one-shot A, U11-4, triggers one-shot B, causing a negative pulse (40 μsec) at U10-2, $\overline{\text{Transfer}}$ for the 3814, which stores the BCD count in the 4-1/2 decade counters into the latches to be multiplexed and decoded for the seven-segment display LEDs.

4.3.14.6 The internal reset (AZ) that goes low at the beginning of signal integration, is inverted twice through U5 and U18, called AZC, and used in the integrator to disable U3C and U3D bilateral switches from a reset state called "Auto Zero."

4.3.14.7 The $\overline{\text{Signal Integrate}}$ output from U13-6 is inverted at U13-3 and applied to U19-12 where the output at pin 11 is inverted, designated $\overline{\text{SIF}}$ on the digitizer PCB, after three inversions through U4 to become the IND drive signal for U1D. The $\overline{\text{SIF}}$ on the main PCB at U19-11 is inverted through U18-2 to drive bilateral switch U1A which, with bilateral switch U1D couple the isolator output voltage to the buffer/integrator during the signal integrate period. Pin 13 of U19 on the main PCB, labeled $\overline{\text{FQ}}$, is a control line from S4 (kHz) at a logic high; thus, in effect, making U19 from pin 12 to 11 an inverter with a positive input.

4.3.14.8 During signal integration U17-12, internal reset, (AZ) is logic low and U17-11, signal integrate, is logic high causing the output, U17-13 to be logic low. At the beginning of signal integration, it was established that the polarity was positive as a result of the logic high at the polarity F/F, U16-5, coupled to U19-9 to enable the NAND gate input. The logic high at the output of U19-8 is inverted through U18 and becomes logic low at pin 6.

4.3.14.9 All functions of signal integration have now been accomplished. The measurement signal from the isolator output has been coupled to the buffer/integrator input. The integrator has been released from Auto Zero by the switches and the output is moving at a negative slope and polarity has been sensed and annunciated.

4.3.14.10 At the end of signal integration, the CMOS counter is reset to zero. The output of U19-11 goes to logic high and U18-2 goes logic low disconnecting the measurement signal from the buffer/integrator input. Signal integrate at U17-11 goes logic low, causing the output at U17-13 to go logic high enabling U19-10. The low output of U19-8 is inverted to a logic high, designated – RD, to drive the logic switching circuitry on the digitizer PCB to configure the reference capacitor using U2A and U2D bilateral switches to apply a –1V to the buffer/integrator input. The CMOS counter will reset to zero again after the first 10 counts (100 counts for the LSD counter) or approximately 100 μsec. This is used to "mask" the switching transients during the transition from signal integrate to reference integrate, which is known as "delayed dual slope." The susceptibility to false triggering during signal to reference integration is much greater with signal inputs at or near zero. The feed forward (+ and –) circuit in the integrator compensates for the delay caused by the CMOS counter 10 count reset as the integrator output ramps back toward zero; hence, null detect.

4.3.14.11 When zero is detected by the null detector for the +1V signal, the output is a negative going pulse of 1.6 msec duration. When applied through U6 inverter to the clock input of the + ND F/F, U15-3, the $\overline{Q}$ output at pin 6 goes logic low. This causes the internal reset (AZ) line at U14-12 to go high which disconnects the –1V reference voltage from the buffer/integrator input, configures the integrator to the condition called "Auto Zero," and triggers the one-shots (A and B) to transfer the BCD value of the LSD and CMOS counters into their respective latches to be coded (seven segment), multiplexed, and displayed.

4.3.14.12 The digitizing sequences used thus far, signal and reference integrate (half scale), have only taken 200 msec. The remaining sequences, reference integrate (to full scale) and "fixed" reset, will account for the other 200 msec. The remaining reference integrate sequence will be an internal reset time as null detect has taken place. When the "fixed" reset period is initiated, caused by a logic low at the output of U13-11, $\overline{\text{Reset}}$ is inverted on the digitizer PCB, labeled "CPD," and drives the bilateral switches U3 A and B to "refill" the Reference Capacitor from the +1V output of the Reference Generator.

4.3.14.13 If a null detect is sensed, during reference integrate, sequence state 2, before 10,000 counts (5% of range) and the DMM is not on the lowest range (in auto range) a "Down Range" is commanded.

Table 4.1 - Sequence Chart

+ Signal = 1.0000V DC, 1 Range

Q_{e1} = High, Q_{e2} = High	(1) $\overline{\text{SIG INT}}$ goes low (2) + N.D. F/F (U15) $\overline{Q}$ goes high (3) – N.D. F/F (U15) $\overline{Q}$ goes high (4) $\overline{\text{RESET}}$ goes high (5) INTERNAL RESET goes low (caused by 2, 3, 4) (6) ONE-SHOTS (Armed for digitizing sequence) (7) RESET SW goes low (releases sw's from Auto Zero) (8) SIG SW goes high (connects iso out to integrator in) (9) NULL DETECTOR OUTPUT goes high (to detect polarity) (10) POL F/F Q OUTPUT goes high (to enable – ref sw @ ref int) and (set pol dr F/F Q output low)
Q_{e1} = Low, Q_{e2} = Low	(1) $\overline{\text{SIG INT}}$ goes high (2) SIG SW goes low (disconnects iso out from integrator in) (3) – REF SW goes high (connects –1V ref to integrator in)
Q_{e1} = High, Q_{e2} = Low	(1) NULL DETECTOR OUTPUT goes low pulse (zero detect) (2) + N.D. F/F (U15) $\overline{Q}$ goes low (causes internal reset to go high) (3) INTERNAL RESET goes high (causes one-shots to go low pulse) (4) ONE-SHOTS pulse low (signals LSD & CMOS counter to stop count) (5) – REF SW goes low (disconnects –1V ref from integrator in) (6) RESET SW goes high (closes reset switches – Auto Zero)
Q_{e1} = Low, Q_{e2} = High	(1) RESET SW is high (Auto Zero) (2) $\overline{\text{RESET}}$ goes low (CPD refills ref cap)

4.3.14.14 If a null detect is not sensed before 199,999 counts is accumulated in the LSD and CMOS counter, an "overload" is annunciated on the readout by a flashing 200000 at the read rate for a manual range or highest range per function. If the DMM is in auto range and overload is sensed, the range counter, U20, is advanced one range. This is a result of the Q_{e2} output of the CMOS 3814 counter, which is latched as an output called $Q_{e2}L$ or O/L. When null detect has not been sensed when the 4th sequence (fixed reset) is entered, the $Q_{e2}L$ (O/L) output of U10-9 goes logic high to detect "overload" or "uprange."

4.3.14.15 If the input signal to the DMM is of negative polarity, the null detector output is applied to U16-2 of the polarity detect F/F, which is a logic low during signal integration. This causes the polarity F/F Q output at pin 5 to be applied to the D input of the Polarity Drive F/F, U16-12, to cause the Q output at pin 9 to go logic low and annunciate the minus polarity symbol on the display. The $\overline{Q}$ output of the polarity detect F/F, U16-6, goes logic high and enables the circuitry for the + RD (plus reference drive) when the reference integrate sequence is started. This causes the bilateral switches, U2 B and C, on the digitizer PCB to configure the charge on the reference cap so that a +1V is applied to the buffer/integrator input.

4.3.14.16 The null detector output, for a negative input signal, goes logic high at the end of reference integrate (zero detect) and is applied to the "clock" input of the – ND F/F, U15-11, and causes the $\overline{Q}$ output at pin 8 to go logic low at null detect to terminate the LSD and CMOS count.

4.3.14.17 In addition to the illustrations, a sequence chart is presented in table 4.1. This chart is a synopsis of the sequence of operation of the timing and control circuits for one measurement cycle. Its basic purpose is for reference after reading the detailed description presented in the following paragraphs. It will also serve as a handy reference to use while reading the detailed description.

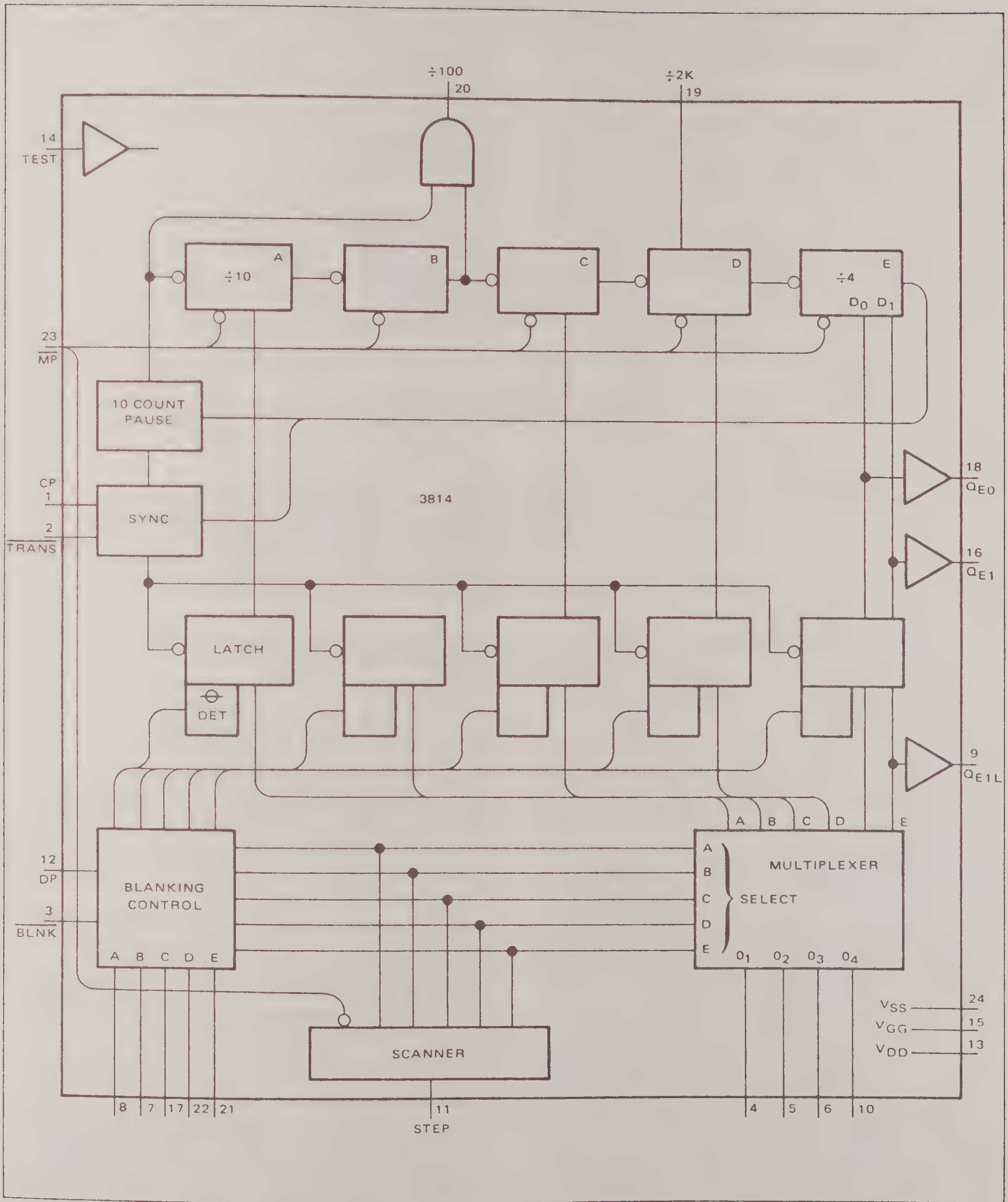

÷100
20
÷2K
19
14
TEST
÷10
A
B
C
D
÷4
E
D0
D1
23
MP
10 COUNT
PAUSE
CP
1
SYNC
2
TRANS
3814
18
QE0
16
QE1
LATCH
DET
9
QE1L
A
B
C
D
E
BLANKING
CONTROL
12
DP
3
BLNK
A B C D E
MULTIPLEXER
SELECT
O1 O2 O3 O4
VSS 24
VGG 15
VDD 13
SCANNER
8
7
17
22
21
11
STEP
4
5
6
10

Figure 4.16 - Logic Array

4.3.15 Large Scale Integration Logic Array (Counter).

4.3.15.1 The heart of the instrument is the 3814 Digital Voltmeter logic array, shown on figure 4.1 as the counter, latch, 4-line decoder, and multiplexer. A more detailed illustration of this device is shown in figure 4.16. It contains four full decade counters, two overflow latches, an underrange output, an overrange output, outputs to drive a BCD to seven segment converter, and decoded outputs to strobe the display. The 3814 counts four full digits and the overrange digit. The output of the LSD decade counter is 100 kHz which drives the CP input to the 3814 chip. The decade counters change state on the rising edge of the clock pulse.

4.3.15.2 A MUX oscillator is used to drive the step input to the 3814. The frequency of the output at U1-4 is 500 Hz ±10%. The step input clocks a ring counter that drives the multiplexer.

4.3.15.3 The 1 output of the fourth decade counter in the 3814 is buffered and used as a divide-by-two thousand (÷2,000) output. This output is used to indicate a signal that is less than 5% of full scale. If the transfer pulse is enabled before the divide-by-2,000 output goes high the output will signal the auto range circuitry that a down range change must be made.

4.3.15.4 The Q0 and Q1 flip-flop outputs of the 5th counter are designated as Q_{e1} and Q_{e2} outputs. These outputs step the DMM through the various periods of the integration process. The signal codes are:

Q_{e1}	Q_{e2}	
1	1	100 ms · Signal integration – decade counts from 300,000 to 399,999
0	0	100 ms · Reference integration -- decade counts from 000,000 to 099,999 (half scale)
1	0	100 ms Reference integration – decade counts from 100,000 to 199,999 (full scale)
0	1	100 ms - Reset - decade counts from 200,000 to 299,999

4.3.15.5 The Q_{e2} output is latched and used as the $Q_{e2}L$ output. If a DMM has a full scale count of 199,999 using the 3814, the high state of $Q_{e2}L$ is used to indicate an overrange condition. The $Q_{e2}L$ output causes the display to read 200,000 at a flashing rate.

4.3.15.6 The edge sensitive transfer input causes the BCD data in the counters to be stored in the latches on the falling edge. Synchronization with the clock is necessary to prevent loading and storing erroneous counter states as a "carry" is trickling through the counters. A transfer command is accepted once during an integration cycle. An internal flip-flop is reset by the counter transition from 399,999 to 000,000. It is set when a transfer occurs and remains set until the next integration sequence. No transfers will be accepted when this flip-flop is set.

4.3.15.7 The clock pulse is constantly adding counts to the counter. As previously mentioned the states of Q_{e1} and Q_{e2} control the state of events that take place during an integration sequence.

4.3.15.8 $Q_{e1} = 1$ and $Q_{e2} = 1$. The counter advances from 300,000 to 399,999. This is the signal integration period. At this time the DMM input signal which has been attenuated, amplified, converted, and/or filtered and connected to the integrator input through a bilateral switch and measurement cap. The feed forward circuit of the integrator adds 10 digits of voltage to the integrator output to mask the switching transients that occur during the transitions from signal integrate to reference integrate.

4.3.15.9 $Q_{e1} = 0$ and $Q_{e2} = 0$. During this period the signal switch is turned off and a reference (plus or minus) is connected to the input of the integrator through bilateral switches and reference cap. The decade counter is set to 000,000 and the 3814 will ignore the next 10 counts. Because of the 3814, the first 10 counts are ignored. This period allows for masking the noise at the time when the signal integration is switched to the reference integration to prevent false zero detection at or near zero analog input signals. The count is started from 000,000 until the null detector crosses zero and signals the end of the reference integration period. Zero detect signals the transfer input to store the BCD count of the decade counters into the latches. If the transfer occurs before the ÷2000 output goes true, the signal is less than 5% of full scale and a down range is commanded if the DMM is in auto range.

4.3.15.10 $Q_{e1} = 1$ and $Q_{e2} = 0$. This reference integration period is from 100,000 to 199,999 which is the F/S capability of the DMM.

4.3.15.11 $Q_{e1} = 0$ and $Q_{e2} = 1$. This is the reset period when the analog and reference inputs to the integrator are removed and bilateral switches short the integrator input to the output in a configuration called auto zero. The count of this period is from 200,000 to 299,999. If the $Q_{c2}L$ output goes true before zero detect signals a transfer, an uprange is commanded if the DMM is in auto range and/or overload is detected and the display indicates overrange.

4.3.15.12 The step input from the MUX oscillator output presents the multiplexed BCD outputs capable of driving a single decoder/driver, such as a SN7447. The decoded outputs 0_a to 0_e drive transistor circuitry that strobes the anodes of the display devices one at a time.

4.3.16 4-to-7 Line Decoder.

4.3.16.1 The 4-to-7 line decoder is shown on figure 4.17. This device is simply a matrix decoder that converts BCD code to 7-line code for display purposes. It's driven by the BCD code from the 3814 counter chip and its 7-line output is tied in parallel to all of the display LEDs.

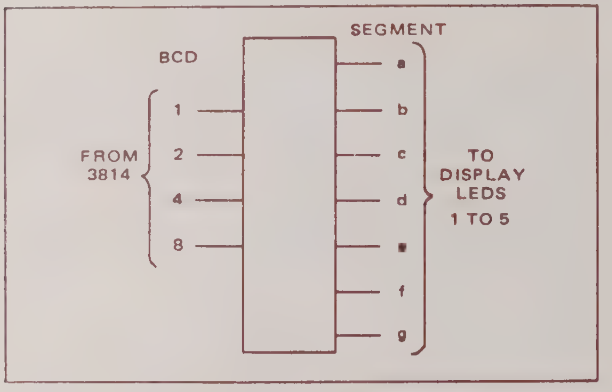


Figure 4.17 - 4-to-7 Line Decoder

4.3.17 BCD to Decimal Decoder.

4.3.17.1 The BCD to Decimal converter shown in figure 4.18 uses the range information from the range circuits to control the position of the decimal point on the display. This device is simply a 3-line to 7-line converter. The range code input determines which decimal point is lit.

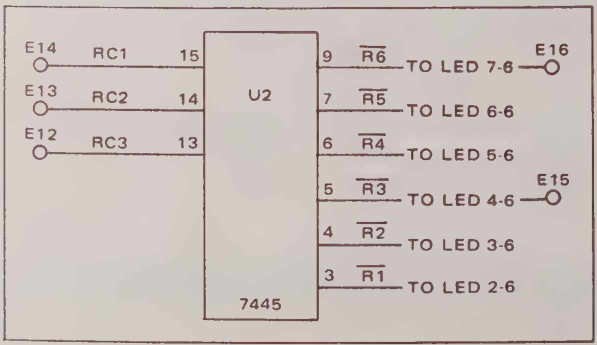


Figure 4.18 - BCD to Decimal Decoder

4.3.18 LED Display.

4.3.18.1 A functional diagram of the display circuit is shown on figure 4.19. The display consists of six 7-bar LED display devices and the polarity display device. The output of the 7-segment decoder is tied in parallel to the inputs of the five 7-line display devices. When the digit code in 7-bar form is on the line for the low order digit display device, the multiplexer in the counter chip will energize the enable line A and the device will display the numeric value on the 7-line bus at that time.

4.3.19 Frequency (kHz) Measurement Function.

4.3.19.1 When the DMM is used to measure frequency, the signal is applied to the input terminals at J101 (Hi) and J102 (Low) and the kHz switch (S4) is enabled. This routes the signal being measured to the Frequency Mode Signal Conditioner (refer to the Main Logic & Interconnection schematic drawing 432095, sheet 3 of 5). This circuit amplifies, shapes, and filters the sinewave measurement signal from 350 mV RMS (sensitivity specification) to 350V RMS (±500 peak) for application to the counter and control circuits.

4.3.19.2 TIMEBASE & MEASUREMENT SIGNAL SWITCHING.

4.3.19.2.1 The dual integration slope timing events established by the Q_{e1} and Q_{e2} outputs of the CMOS 3814 (U10) are essentially the same as those used to digitize a DC measurement, except that the reference integration period is not controlled by the analog voltage level of the isolator amplifier output.

4.3.19.2.2 The FQ (logic high) signal from S4 section C is routed to pin 4 of And gate U12 to enable the Signal Integrate output of U13-3; which causes the (+ RD) plus reference drive to go high. The result is that a +1V DC level is applied to the input of the Buffer Amplifier (Integrator) on the Digitizer PCB during the Signal Integrate sequence, causing a negative slope for 100 msec. The $\overline{\text{FQ}}$ (logic low) signal from S4 section C is routed to pin 13 of NAND gate U19 to disable the $\overline{\text{SIF}}$ (logic high) and SID (logic low) drive signals used to normally switch the output of the isolator during Reference Integration.

4.3.19.2.3 At the end of Signal Integration, the reference capacitor, C1, on the Digitizer PCB is driven by the (– RD) minus reference drive signal; which applies a –1V DC to the input of the Buffer Amplifier (Integrator) during the Reference Integration sequence for 100 msec. This causes the output of the Integrator to ramp back to zero. The count is terminated in the LSD and CMOS Counters, and displayed on the readout.

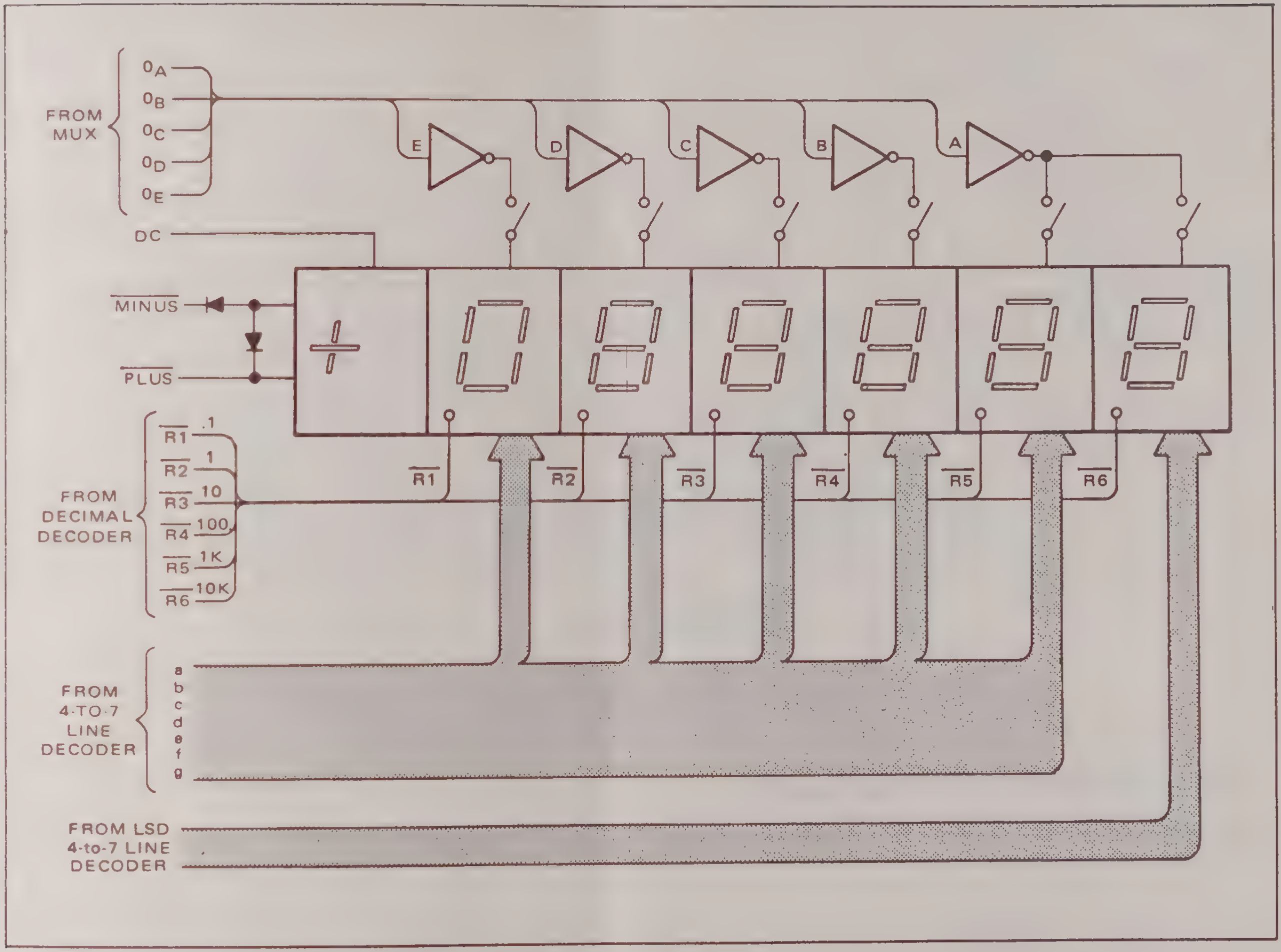


Figure 4.19 - LED Display

4.3.19.2.4 The clock signal from the crystal oscillator (1 MHz) is applied through And gate U2-11, Or gate U2-6, and And gate U2-8 to the (LSD) least significant digit counter, U3-15. The output of the LSD counter, U3-9, is inverted through U5-8 (÷10 clock) and used as the clock pulse (CP) input to the CMOS counter U10-1; which produces the Q_{e1} and Q_{e2} timing control outputs required to establish the sequences for digitizing.

4.3.19.2.5 During the Signal Integration period, the 1 MHz oscillator is used to step the LSD and CMOS counters for 100,000 counts or 100 msec. The LSD and CMOS counters are stepped by the output of the Frequency Mode Signal Conditioner during the 100 msec (Timebase) Reference Integration sequence.

4.3.19.2.6 The FQ (logic high) signal from S4 section C is routed to pin 12 of And gate U12 to enable its input with the output of U17-13, Reference Interval, at U12-13 to enable U2-2. The result is that U4-4 is logic high during Reference Integration, allowing the output frequency of the Signal Conditioner to be gated to the LSD and CMOS counters through U4-8 to U2-5.

4.3.19.3 2,000 kHz (2 MHz) RANGE.

4.3.19.3.1 The route the frequency of the measurement signal takes is dependent on the range selected by the operator. If the DMM is on the 2 MHz range, the $\overline{\text{UP LIMIT}}$ is logic high, enabling the Direct Count gate at U4-10. This allows the frequency of the measurement signal to flow into U4 at pin 5, out of U4 at pin 6, into the enabled, Direct gate at U4-9, and out of U4 at pin 8 to U2-5 to be applied to the LSD and CMOS counters, until zero crossing (NULL DETECT). See figure 4.20.

4.3.19.4 20,000 kHz (20 MHz) RANGE.

4.3.19.4.1 When the instrument is set to the 20 MHz range, the $\overline{\text{DOWN LIMIT}}$ control signal at U4-13 is logic

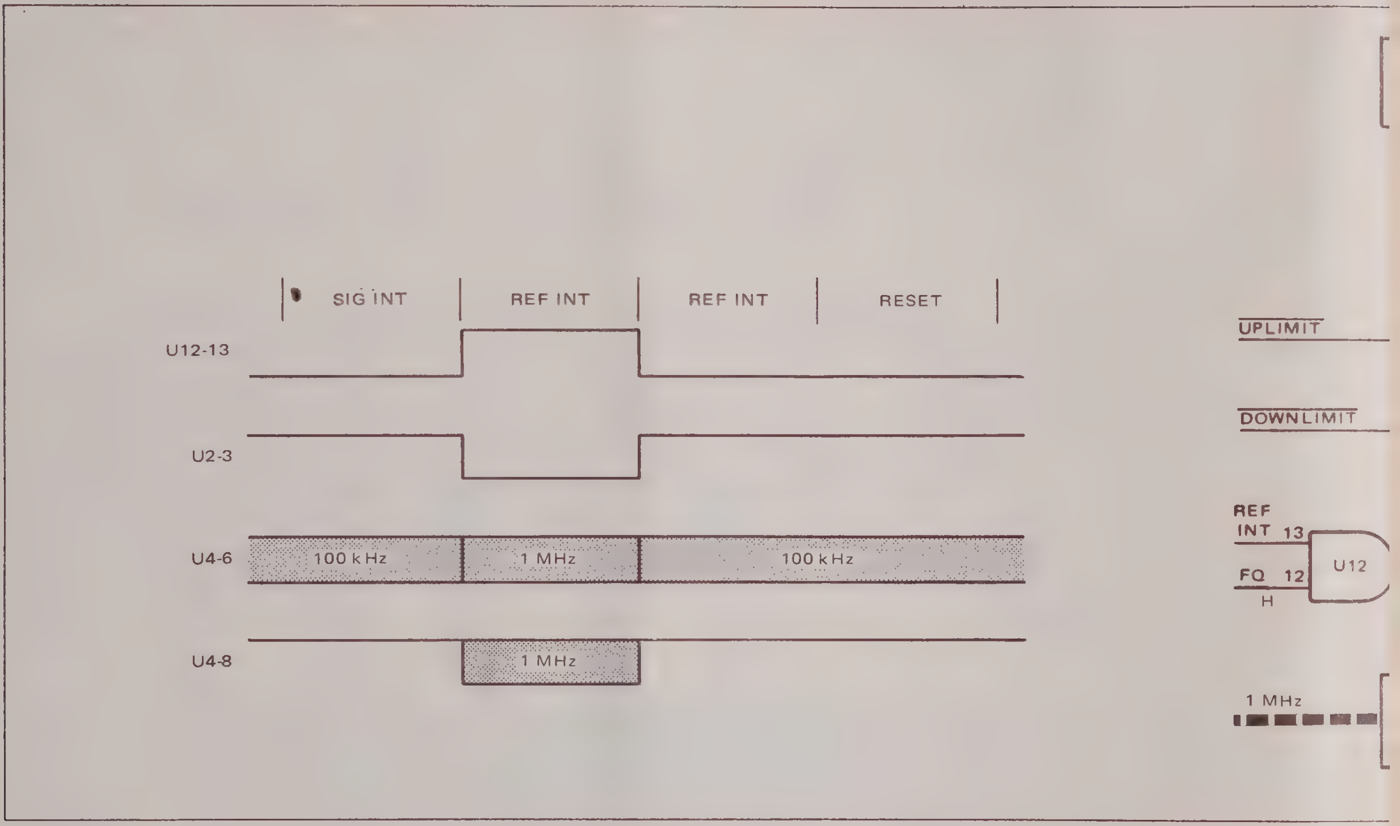

SIG INT
REF INT
REF INT
RESET
U12-13
U2-3
U4-6
100 kHz
1 MHz
100 kHz
U4-8
1 MHz
UPLIMIT
DOWNLIMIT
REF INT 13
FQ 12
H
U12
1 MHz

Figure 4.20 - 2,000 kHz (2 MHz) Range Signal Flow

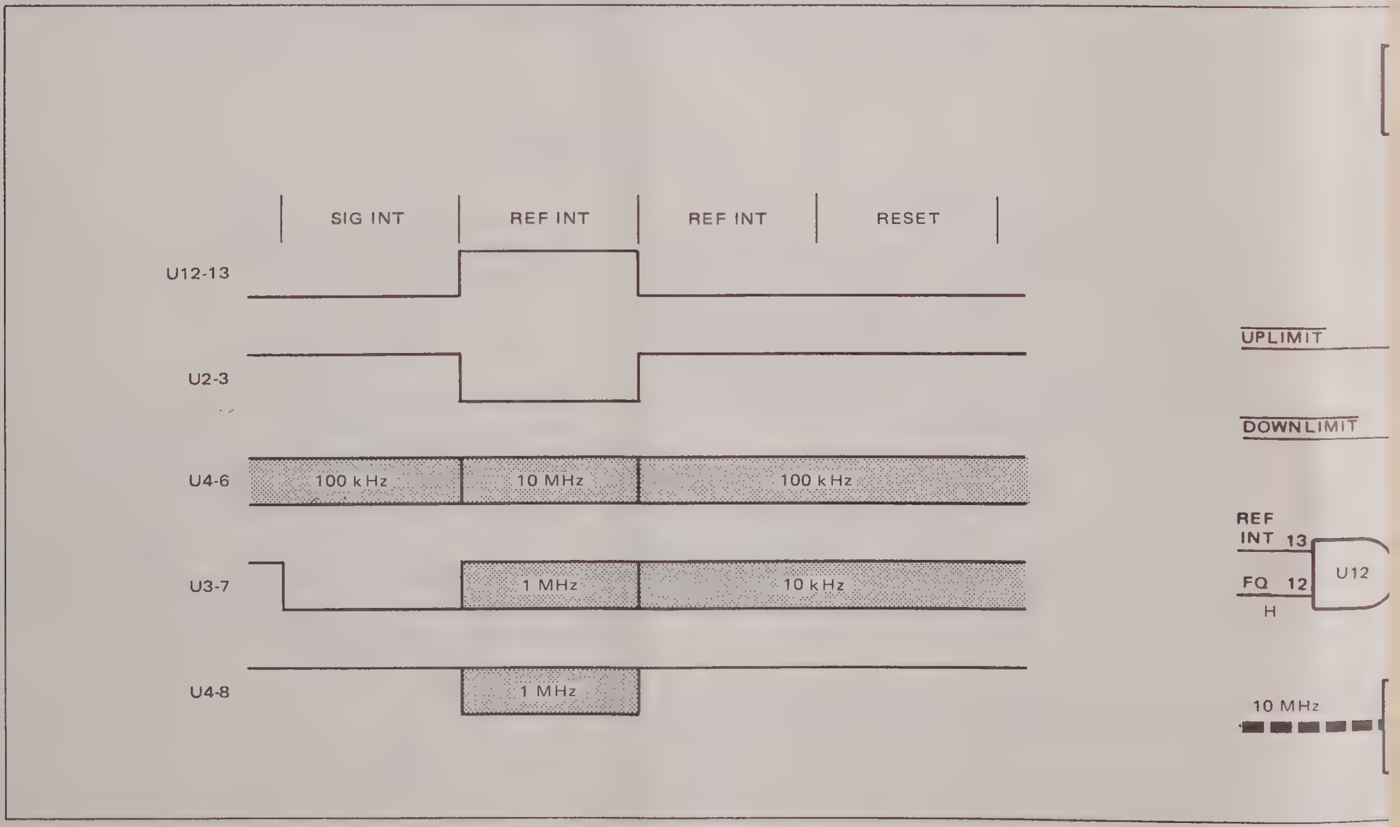
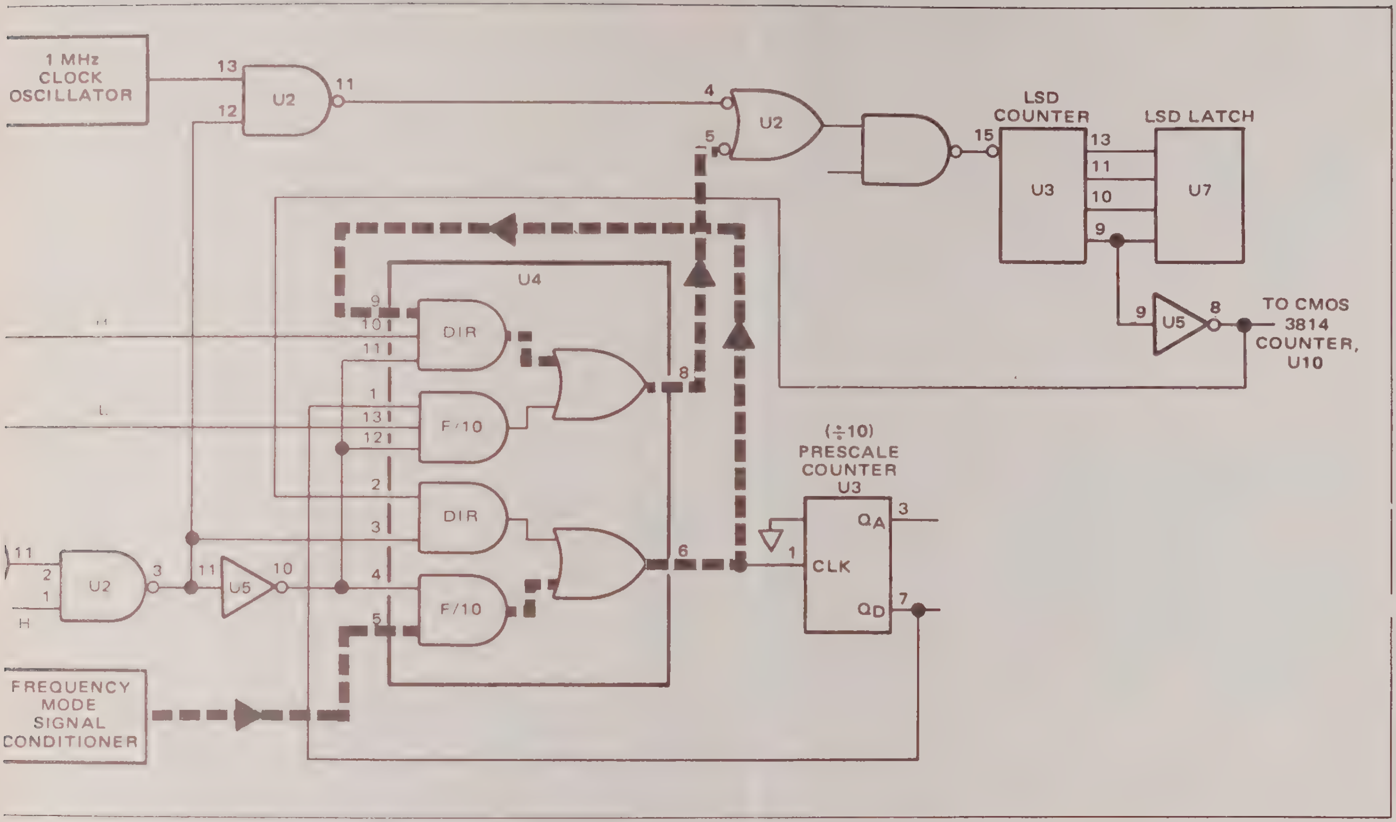
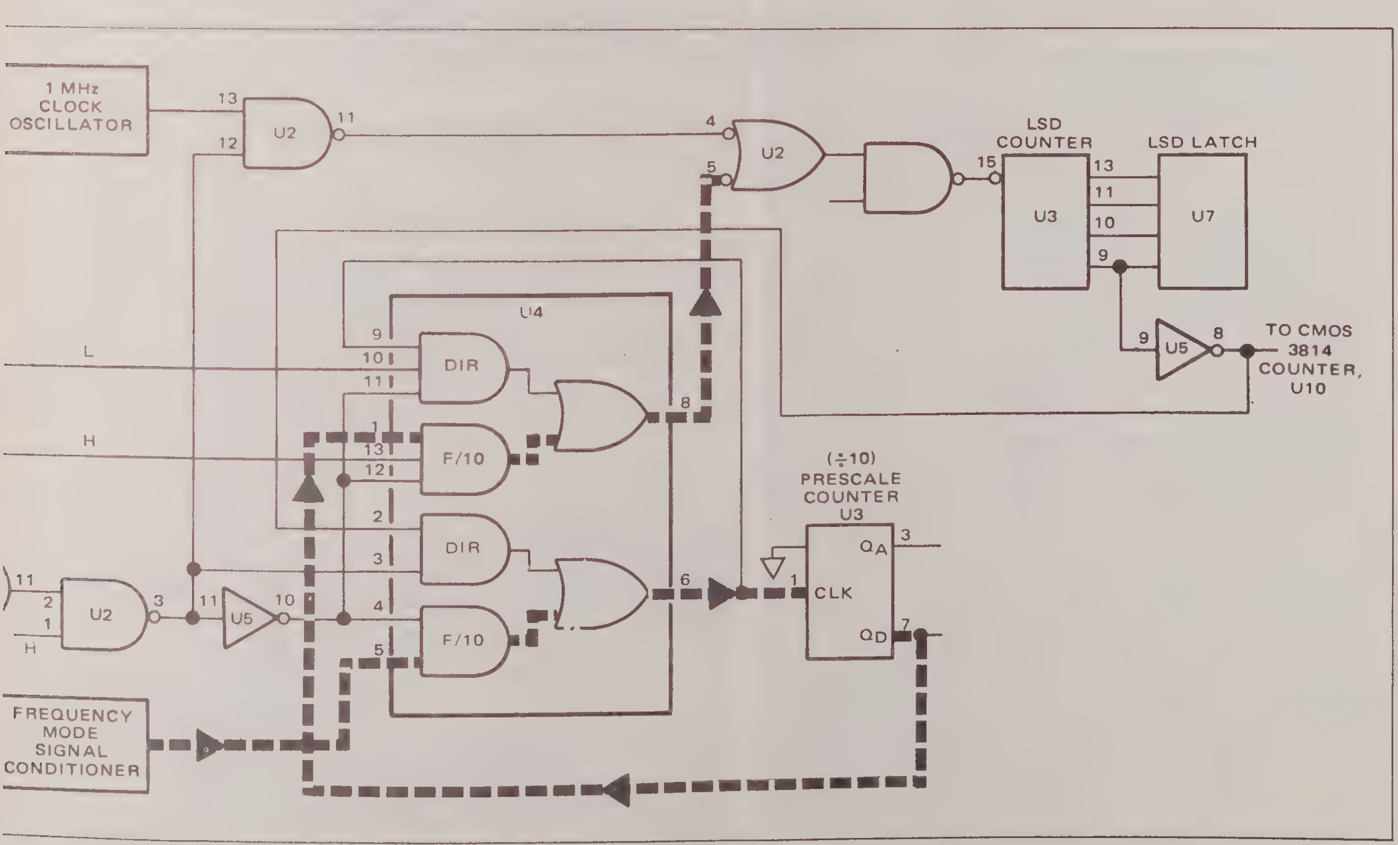

SIG INT
REF INT
REF INT
RESET
U12-13
U2-3
U4-6
100 kHz
10 MHz
100 kHz
U3-7
1 MHz
10 kHz
U4-8
1 MHz
UPLIMIT
DOWNLIMIT
REF INT 13
FQ 12
H
U12
10 MHz

Figure 4.21 - 20,000 kHz (20 MHz) Range Signal Flow


1 MHz CLOCK OSCILLATOR
U2
13
12
11
4
5
U2
15
LSD COUNTER
U3
13
11
10
9
LSD LATCH
U7
U4
9
10
11
DIR
1
13
12
F/10
8
2
3
DIR
4
F/10
5
6
L
11
2
1
H
U2
3
11
U5
10
(÷10) PRESCALE COUNTER U3
QA
3
1
CLK
QD
7
9
U5
8
TO CMOS 3814 COUNTER, U10
FREQUENCY MODE SIGNAL CONDITIONER


1 MHz CLOCK OSCILLATOR
U2
13
12
11
4
5
U2
15
LSD COUNTER
U3
13
11
10
9
LSD LATCH
U7
U4
9
10
11
DIR
L
1
13
12
F/10
H
8
2
3
DIR
4
F/10
5
6
11
2
1
H
U2
3
11
U5
10
(÷10) PRESCALE COUNTER U3
QA
3
1
CLK
QD
7
9
U5
8
TO CMOS 3814 COUNTER, U10
FREQUENCY MODE SIGNAL CONDITIONER

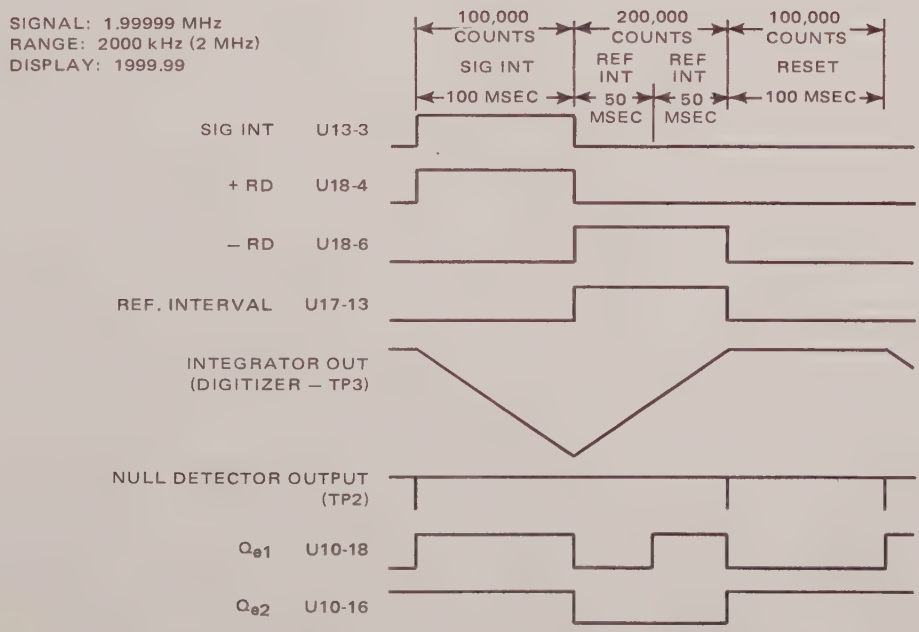
high, enabling the F/10 gate. The frequency of the measurement signal into U4 is at pin 5, out at pin 6, into the (÷10) Prescale Counter at U3-1, out of U3 at pin 7 to the enabled F/10 gate at U4 pin 1, and out of U4 at pin 8 to U2-5 to be applied to the LSD and CMOS counter. The net result is that the frequency from the Signal Conditioner output is divided-by-ten through the Prescale Counter during the Reference Integration sequence. See figure 4.21.

4.3.19.5 REFERENCE INTEGRATION vs. TIMEBASE.

4.3.19.5.1 As all sinewave signal frequencies on the 20 MHz range are divided-by-ten, the following discussion will be directed to the 2 MHz (direct-counting) frequency range. Frequency is inversely proportional to the duration of a cycle. With a timebase limitation of 100 msec, caused by the Reference Integration slope, and a maximum display count of 199,999; a signal frequency of 2 MHz (duration of .5 μsec per cycle) times the displayed count of 199,999 equals 100 msec. The input frequency, during the Reference Integration sequence is used to advance the counters (LSD and CMOS) and register the count of the input signal. If the input signal frequency is below 1 MHz on the 2 MHz range (10 MHz on the 20 MHz range), for example: 10 kHz; the display will read 0010.00 or the count accumulation during Reference Integration will be 1000 for 100 msec. The counter still will have to accumulate 100,000 counts before Q_{e1} changes state, which means that an additional length of time must be added to sequence 3 of the digitizing cycle.

4.3.19.5.2 The timing sequences in figure 4.22 depict the Q_{e1}/Q_{e2}, integration slopes, and null detect signals for a 2 MHz, 1 MHz, and 100 kHz signal frequency. Notice that in the timing diagrams the count total per sequence and that the Q_{e1} and Q_{e2} signals are complete for each digitize sequence, as follows:

Qe1	Qe2	Sequence
1	1	Signal Integrate
0	0	Reference Integrate/Timebase
1	0	Reference Integrate
0	1	Reset


SIGNAL: 1.99999 MHz
RANGE: 2000 kHz (2 MHz)
DISPLAY: 1999.99
100,000 COUNTS
200,000 COUNTS
100,000 COUNTS
SIG INT
REF INT
REF INT
RESET
100 MSEC
50 MSEC
50 MSEC
100 MSEC
SIG INT U13-3
+ RD U18-4
– RD U18-6
REF. INTERVAL U17-13
INTEGRATOR OUT (DIGITIZER – TP3)
NULL DETECTOR OUTPUT (TP2)
Qe1 U10-18
Qe2 U10-16

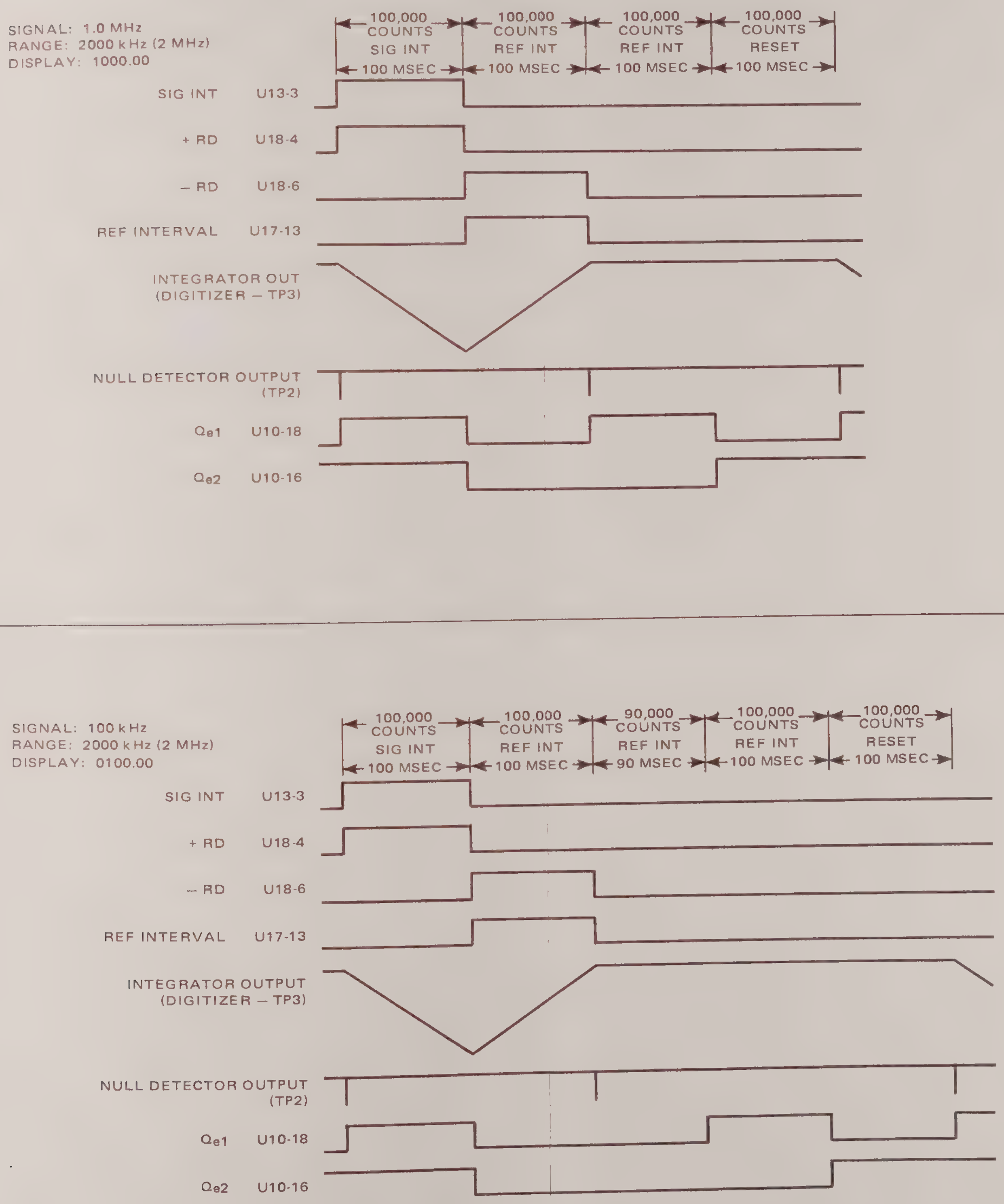

SIGNAL: 1.0 MHz
RANGE: 2000 kHz (2 MHz)
DISPLAY: 1000.00
100,000 COUNTS SIG INT 100 MSEC
100,000 COUNTS REF INT 100 MSEC
100,000 COUNTS REF INT 100 MSEC
100,000 COUNTS RESET 100 MSEC
SIG INT U13-3
+ RD U18-4
– RD U18-6
REF INTERVAL U17-13
INTEGRATOR OUT (DIGITIZER – TP3)
NULL DETECTOR OUTPUT (TP2)
Qe1 U10-18
Qe2 U10-16
SIGNAL: 100 kHz
RANGE: 2000 kHz (2 MHz)
DISPLAY: 0100.00
100,000 COUNTS SIG INT 100 MSEC
100,000 COUNTS REF INT 100 MSEC
90,000 COUNTS REF INT 90 MSEC
100,000 COUNTS REF INT 100 MSEC
100,000 COUNTS RESET 100 MSEC
SIG INT U13-3
+ RD U18-4
– RD U18-6
REF INTERVAL U17-13
INTEGRATOR OUTPUT (DIGITIZER – TP3)
NULL DETECTOR OUTPUT (TP2)
Qe1 U10-18
Qe2 U10-16

Figure 4.22 - Timing Sequences

SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.1.1 This section contains information necessary to check the calibration of the Model 5100, perform calibration adjustments and to troubleshoot the instrument in case of malfunction. The calibration checks are also used for receiving inspection or specification validation purposes. This maintenance information is organized to provide for two levels of maintenance.

5.1.2 The section is divided into three major subsections; (1) Calibration Checks, (2) Calibration Adjustment and (3) Troubleshooting Performance Tests. The troubleshooting is further divided into Unit Performance Tests and Subassembly Performance Tests. The unit level performance tests are designed to check the instrument by function, such as AC Volts, and enable isolation of a malfunction to a replaceable module or subassembly. The subassembly performance tests are designed to check the operation of a module or subassembly and isolate a malfunction to an individual component or circuit.

5.2 CALIBRATION CHECKS.

5.2.1 This subsection of the Maintenance section contains instructions and reference information for checking the calibration of the Model 5100 DMM. The instructions are presented in tabular form and are organized by instrument function. In addition, the test setup, input and control settings are provided for each step in the procedure. Test equipment required is listed in table 5.1.

Table 5.1 - Test Equipment Required for Calibration Checks and Adjustment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106, GUIDELINE 9152/T6
	(2)	DC Calibrators	0.1 ppm resolution	FLUKE 332B, HP740B
	(1)	Fixed High Voltage Divider	1 ppm, certified	GUIDELINE 9700
	(1)	Voltage Divider Adjustable	0.1 ppm resolution	FLUKE 720A, JRL SVD-108
	(1)	Null Detector/μVoltmeters	1 μV sensitivity	FLUKE 845AR, HP419A
AC	(1)	Thermal Transfer Standard	35 ppm @ 400 Hz, 50 ppm @ 40 kHz	HOLT 6A
	(1)	Thermal Voltage Converter	50 ppm @ 100 kHz	HOLT 11
	(1)	AC Voltage Source	1 ppm resolution	HP745A/746A
Ω	(7)	Resistance Standards		
		100Ω	10 ppm	ESI SR1 with corrections
		1 KΩ	10 ppm	ESI SR1 with corrections
		10 KΩ	10 ppm	ESI SR1 with corrections
		100 KΩ	10 ppm	ESI SR1 with corrections
		1 MΩ	10 ppm	ESI SR1 with corrections
		10 MΩ	50 ppm	ESI SR1 with corrections
OTHER	(1)	Phillips head screwdriver #1	-	–
	(1)	Insulated Adjustment tool		JFD5284
	(1)	10 Kohm 1/4 Watt, 5% Carbon Resistor	5%	--
	(1)	1 Megohm 1/4 Watt, 5% Carbon Resistor	5%	
	(2)	Minigator Clip Leads with Shields	-	--

Table 5.2 - DCV Calibration Check (90 Day, 23°C ± 5°C Spec)

Input and Control Setting		
Function: DCV Range: .2, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper		Note: Offset greater than ±8 digits will require adjustment of R32 (front panel) on .2 range. Note: Guard (J105) must be strapped to SIG LO (J102).
Signal Range	Signal Input	Readout Performance Standard
.2 (manual)	.000000	±.000008
2 (manual)	.000000	±.000002
20 (manual)	.000000	±.000002
200 (manual)	.000000	±.000002
1000 (manual)	.000000	±.000004
Remove the jumper and apply the input voltages shown		
.2 (manual)	±.199000	±.19890 to ±.199020
2 (manual)	±1.99000	±1.98990 to ±1.99010
20 (manual)	±19.9000	±19.8990 to ±19.9010
200 (manual)	±199.000	±198.990 to ±199.010
1000 (manual)	±1200.00 (max. input)	±1199.76 to ±1200.24
Set DMM to Auto Range and apply the input voltage shown and verify that the instrument autoranges as shown		
±0099.99 VDC	DMM Down Ranges from	1000 Range to 200 Range
±009.999 VDC	DMM Down Ranges from	200 Range to 20 Range
±00.9999 VDC	DMM Down Ranges from	20 Range to 2 Range
±0.09999 VDC	DMM Down Ranges from	2 Range to .2 Range
±.200000 VDC	DMM Up Ranges from	.2 Range to 2 Range
±2.00000 VDC	DMM Up Ranges from	2 Range to 20 Range
±20.0000 VDC	DMM Up Ranges from	20 Range to 200 Range
±200.000 VDC	DMM Up Ranges from	200 Range to 1000 Range
Set voltage standard to 0V and remove input cables		

Table 5.3 - ACV (Averaging) Calibration Check (90 Day, 23°C ± 5°C)

Input and Control Setting	
Function: ACV Range: .2, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper	Note: Guard (J105) must be strapped to SIG LO (J102). Note: Signals below 0.1% of full scale are not spec'd.

Signal Range	Signal Input	Frequency	Readout Performance Standard
2 (manual)	.000000	N/A	0.00000 to 0.00100
20 (manual)	.000000	N/A	00.0000 to 00.0100
200 (manual)	.000000	N/A	000.000 to 000.100
1000 (manual)	.000000	N/A	0000.00 to 0001.00
Remove the jumper and apply the following input voltages (RMS, Sine)			
2 (manual)	1.99000 VAC	30 Hz to 50 Hz	1.96940 to O/L, or (02.0160 on 20 RNG)
2 (manual)	1.99000 VAC	50 Hz to 100 Hz	1.98480 to 1.99520
2 (manual)	1.99000 VAC	100 Hz to 10 kHz	1.98790 to 1.99210
2 (manual)	1.99000 VAC	10 kHz to 20 kHz	1.98480 to 1.99520
2 (manual)	1.99000 VAC	20 kHz to 100 kHz	1.96940 to O/L, or (02.0160 on 20 RNG)
20 (manual)	19.9000 VAC	30 Hz to 50 Hz	19.6940 to O/L, or (020.160 on 200 RNG)
20 (manual)	19.9000 VAC	50 Hz to 100 Hz	19.8480 to 19.9520
20 (manual)	19.9000 VAC	100 Hz to 10 kHz	19.8790 to 19.9210
20 (manual)	19.9000 VAC	10 kHz to 20 kHz	19.8480 to 19.9520
20 (manual)	19.9000 VAC	20 kHz to 100 kHz	19.6940 to O/L, or (020.160 on 200 RNG)
200 (manual)	199.000 VAC	30 Hz to 50 Hz	196.940 to O/L, or (0199.90 on 1000 RNG)
200 (manual)	199.000 VAC	50 Hz to 100 Hz	198.480 to 199.520
200 (manual)	199.000 VAC	100 Hz to 10 kHz	198.790 to 199.210
200 (manual)	199.000 VAC	10 kHz to 20 kHz	198.480 to 199.520
200 (manual)	199.000 VAC	20 kHz to 100 kHz	196.940 to O/L, or (0199.90 on 1000 RNG)
1000 (manual)	0500.00 VAC	30 Hz to 100 Hz	0498.35 to 0501.65
1000 (manual)	0500.00 VAC	100 Hz to 10 kHz	0498.85 to 0501.15
1000 (manual)	0500.00 VAC	10 kHz to 20 kHz	0498.35 to 0501.65
1000 (manual)	1000.00 VAC (max. input)	30 Hz to 100 Hz	0994.60 to 1005.40
1000 (manual)	1000.00 VAC (max. input)	100 Hz to 10 kHz	0996.60 to 1003.40
1000 (manual)	1000.00 VAC (max. input)	10 kHz to 20 kHz	0994.60 to 1005.40
Set Voltage Standard to 0V and remove input cables			

Table 5.4 - ACV (True RMS) Calibration Check (90 Day, 23°C ± 5°C)

Input and Control Setting			
Function: ACV Range: 2, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper			Note: Guard (J105) must be strapped to SIG LO (J102). Note: Signals below 1.0% of full scale are not spec'd.
Signal Range	Signal Input	Frequency	Readout Performance Standard
2	.00000		0.00000 to 0.00300
20	.000000		00.0000 to 00.0300
200	.000000		000.000 to 000.300
1000	.000000		0000.00 to 0003.00
Remove the jumper and apply the following input voltages (Sine, RMS)			
2 (manual)	1.99000 VAC	30 Hz to 100 Hz	1.98000 to O/L, or (02.0360 on 20 RNG)
2 (manual)	1.99000 VAC	100 Hz to 5 kHz	1.98400 to 1.99600
2 (manual)	1.99000 VAC	5 kHz to 50 kHz	1.98200 to 1.99800
2 (manual)	1.99000 VAC	50 kHz to 100 kHz	1.97400 to O/L, or (02.0600 on 20 RNG)
2 (manual)	1.99000 VAC	100 kHz to 200 kHz	1.88500 to O/L, or (02.1400 on 20 RNG)
2 (manual)	1.99000 VAC	200 kHz to 300 kHz	1.78900 to O/L, or (02.2900 on 20 RNG)
20 (manual)	19.9000 VAC	30 Hz to 100 Hz	19.8000 to O/L, or (020.360 on 200 RNG)
20 (manual)	19.9000 VAC	100 Hz to 20 kHz	19.8600 to 19.9400
20 (manual)	19.9000 VAC	20 kHz to 50 kHz	19.8200 to 19.9800
20 (manual)	19.9000 VAC	50 kHz to 100 kHz	19.8000 to O/L, or (020.360 on 200 RNG)
20 (manual)	19.9000 VAC	100 kHz to 200 kHz	18.8500 to O/L, or (021.400 on 200 RNG)
20 (manual)	19.9000 VAC	200 kHz to 300 kHz	17.8900 to O/L, or (022.000 on 200 RNG)
200 (manual)	199.000 VAC	30 Hz to 100 Hz	198.000 to O/L, or (0203.60 on 1000 RNG)
200 (manual)	199.000 VAC	100 Hz to 20 kHz	198.600 to 199.400
200 (manual)	199.000 VAC	20 kHz to 50 kHz	198.200 to 199.800
200 (manual)	199.000 VAC	50 kHz to 100 kHz	198.000 to O/L, or (0203.60 on 1000 RNG)
200 (manual)	199.000 VAC	100 kHz to 200 kHz	188.500 to O/L, or (0214.00 on 1000 RNG)
200 (manual)	199.000 VAC	200 kHz to 300 kHz	178.900 to O/L, or (0220.00 on 1000 RNG)

Table 5.4 - ACV (True RMS) Calibration Check (90 Day, 23°C ± 5°C) continued

Signal Range	Signal Input	Frequency	Readout Performance Standard
1000 (manual)	1000.00 (max. input)	30 Hz to 100 Hz	0993.00 to 1007.00
1000 (manual)	1000.00 (max. input)	100 Hz to 20 kHz	0997.00 to 1003.00
1000 (manual)	0400.00 (max. input)	20 kHz to 50 kHz	0395.20 to 0404.80
1000 (manual)	0200.00 (max. input)	50 kHz to 100 kHz	0195.40 to 0204.60
1000 (manual)	0100.00 (max. input)	100 kHz to 200 kHz	0090.00 to 0110.00
1000 (manual)	0067.00 (max. input)	200 kHz to 300 kHz	0050.30 to 0083.70
Set Voltage Standard to 0V and remove input cables			

Table 5.5 - Kohms Calibration Check (90 Day, 23°C ± 5°C)

Input & Control Setting	
Function: KΩ Range: .2, Manual Input Terminals: J101 (Hi) and J103 (KΩ source) connected to J102 (Lo) and J104 (KΩ sink) with a copper jumper	Note: Guard (J105) must be strapped to SIG LO (J102).

Signal Range	Signal Input	Readout Performance Standard
All ranges	Short	.2 KΩ/.000006, 2 KΩ/0.00006, 20 KΩ/00.0006, 200 KΩ/000.006, 2 MΩ/0000.06, & 20 MΩ/00000.6
Remove the jumper and apply the following resistance inputs		
.2 KΩ (manual)	199.000Ω	.198980 to .199020
2 KΩ (manual)	1.99000 KΩ	1.98982 to 1.99018
20 KΩ (manual)	19.9000 KΩ	19.8982 to 19.9018
200 KΩ (manual)	199.000 KΩ	198.982 to 199.018
2000 KΩ (manual)	1.99000 MΩ	1989.80 to 1990.20
20000 KΩ (manual)	19.9000 MΩ	19895.4 to 19904.6
Auto	Short	Auto Ranges to .2 KΩ Range
Auto	Open	Auto Ranges to 20 MΩ Range, flashing 20000 (O/L)
Remove resistance standards and input cables		

Table 5.6 - kHz Calibration Check (90 Day, 23°C ± 5°C)

Function: kHz Range: 2000, Manual Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper		Note: Guard (J105 must be strapped to SIG LO (J102).
Frequency Range	Frequency Input @ 1V RMS	Readout Performance Standard
2000	200 Hz	0000.16 to 0000.24
2000	2 kHz	0001.96 to 0002.04
2000	20 kHz	0019.96 to 0020.04
2000	200 kHz	0199.95 to 0200.05
2000	2 MHz	1999.84 to 02000.5 (Up Range)
20,000	20 MHz	19998.4 to O/L
Remove input frequency and input cables		

NOTE

The DMM (for the Frequency function) upranges, in Autorange, between 2 MHz and 5 MHz.

NOTE

The DMM must be manually upranged for input frequencies above 5 MHz.

5.3 CALIBRATION ADJUSTMENTS.

5.3.1 Test setup and adjustment instructions are presented in this subsection. If performance of the calibration checks indicate the need for adjustment, perform the appropriate adjustment procedure. Like the calibration checks, the adjustment procedures are organized by instrument function. This section covers the calibration of the Dana Model 5100 Digital Multimeter and is designed to return the instrument to its published specification for indefinite periods of time. The procedure consists of applying known input levels and adjusting the appropriate component for the indicated value. A list of equipment required to perform the calibration procedure is provided in table 5.1.

5.3.2 Disassembly of the instrument case is as follows:

a. Place instrument on a flat level surface with the bail extended towards the back of the instrument.

b. Disconnect the power cable and remove the screws (see table 3.2) on the back panel.

c. Slide the instrument out of the case.

5.3.3 The following steps are performed prior to making any adjustments to the instrument.

a. Check the line voltage requirements stamped on the serial tag located on the back of the instrument and insure that the available power source is the same. Connect the instrument to the line and set the power switch to ON. Allow at least 30 minutes for the instrument to temperature stabilize.

b. Refer to the operating manuals provided with the test equipment to be used and provide appropriate warmup time.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

5.3.4 DC Voltage Sources.

5.3.4.1 Calibration of the 5100 to its published specifications requires the use of metrology standards and techniques, which are presented in the following paragraphs.

5.3.4.2 The 10V, 100V, and 1000V range sources are derived by the method illustrated in figure 5.1. The setup is as follows:

a. Disconnect standard cell bank and μVmeter leads and set the DC calibrator on the desired voltage range of 10, 100, or 1000.

b. Adjust the decade voltage divider for a ratio equal to Voltage of the standard cells/Desired decade voltage.

c. Connect the μVmeter and adjust the DC calibrator source for the amount required to achieve null.

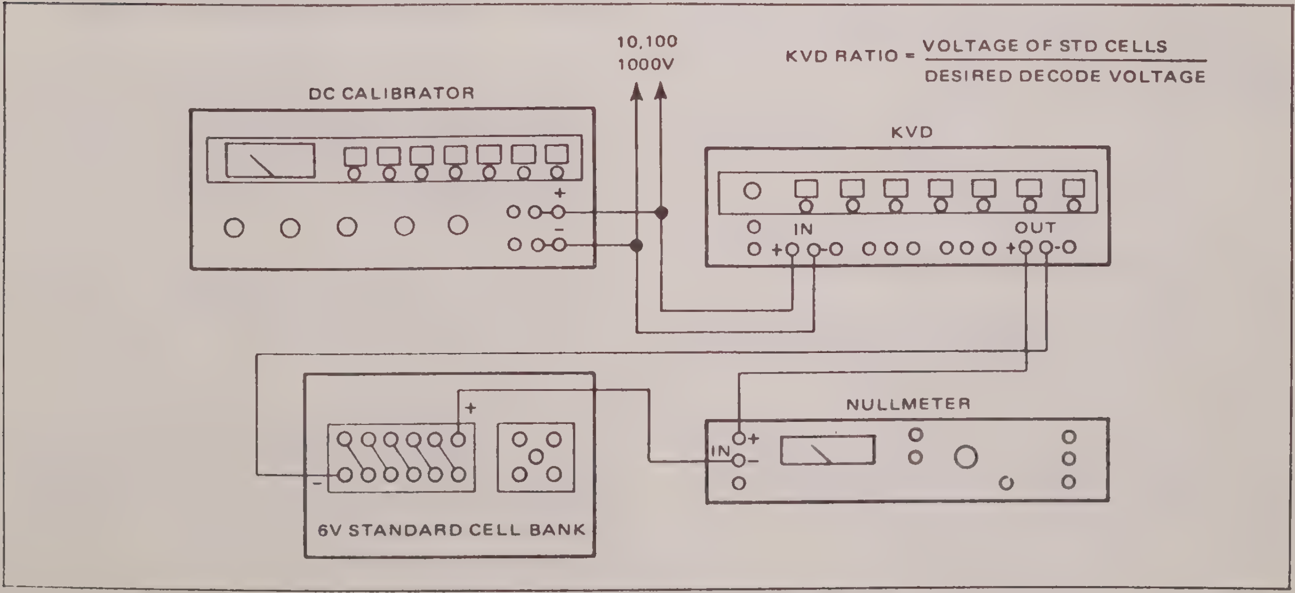


Figure 5.1 - 10V, 100V and 1000V Sources

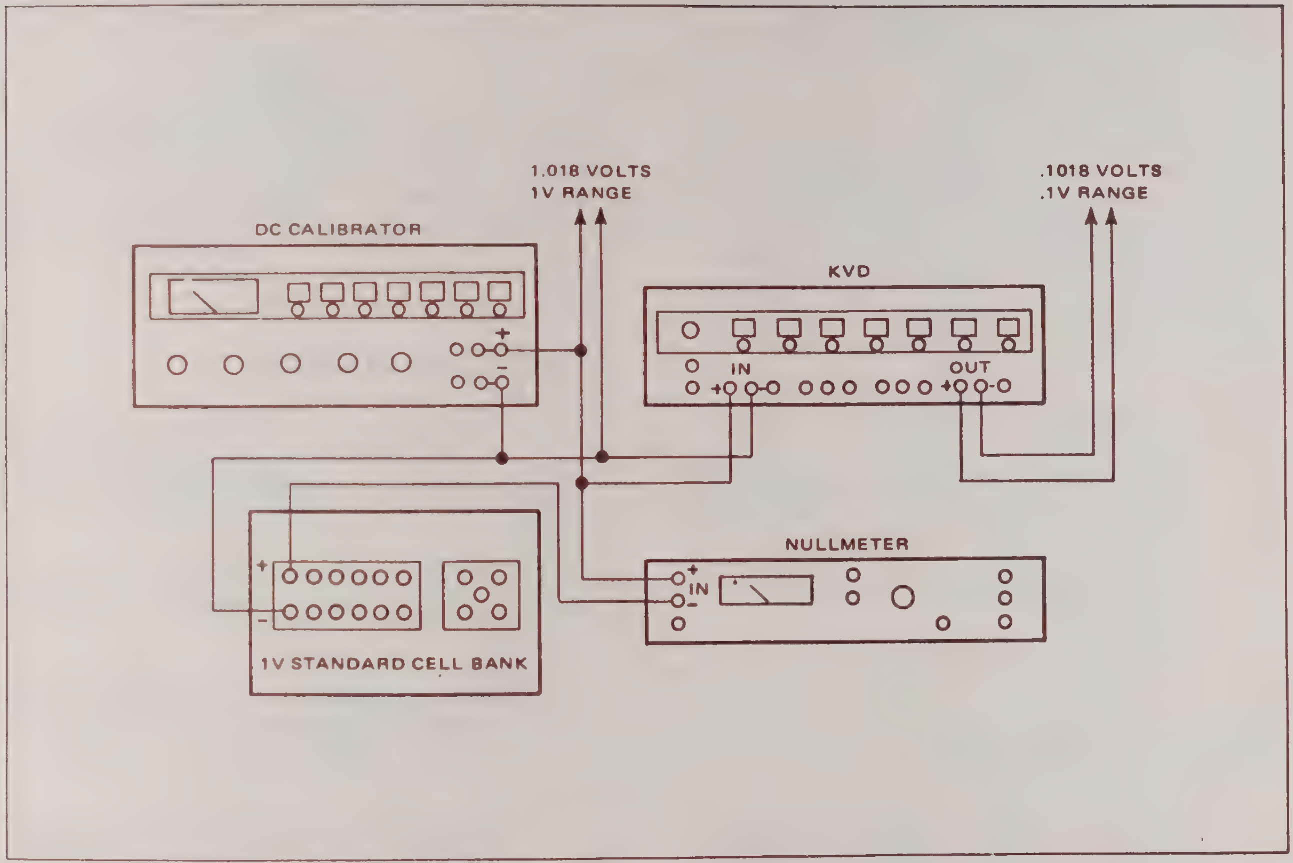


Figure 5.2 - 1V, .1V Sources

5.3.4.3 The 1 volt source is derived and equal in voltage to a single certified standard cell by the method illustrated in figure 5.2. The setup is as follows:

a. Disconnect the standard cell and µVmeter leads and set the DC calibrator for an output equal to the level of the certified cell.

b. Connect the µVmeter and adjust the DC calibrator source for the amount required to achieve null.

5.3.4.4 The .1 volt source is derived from the 1 volt source by use of a precision voltage divider in the method illustrated in figure 5.2.

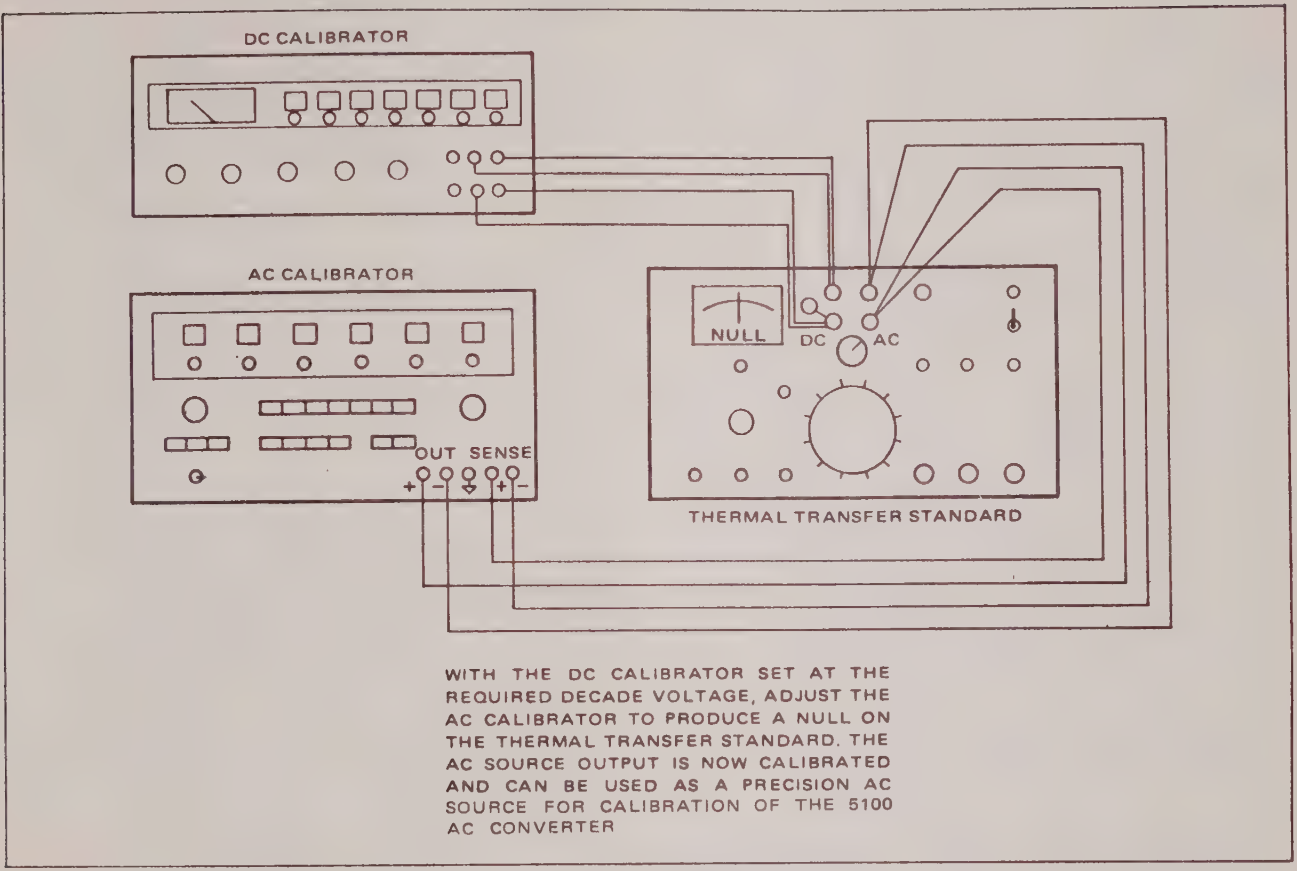
5.3.4.5 The divider is set to .1000000. The output of the divider is then a precise 1/10th of the 1 volt input and is used to calibrate the .1 DCV range of the DMM.

5.3.5 AC Voltage Source (Sinusoidal RMS).

5.3.5.1 The generation of accurate AC signals for calibrating the AC converter requires the use of a thermal transfer standard, a DC voltage standard, and a stable AC voltage source.

5.3.5.2 The test setup is shown in figure 5.3. Information on the use of the transfer standard can be obtained from the operator's manual.

5.3.5.3 The accuracy of the AC voltage source is equal to the sum of the transfer standard and DC voltage source accuracies.



WITH THE DC CALIBRATOR SET AT THE REQUIRED DECADE VOLTAGE, ADJUST THE AC CALIBRATOR TO PRODUCE A NULL ON THE THERMAL TRANSFER STANDARD. THE AC SOURCE OUTPUT IS NOW CALIBRATED AND CAN BE USED AS A PRECISION AC SOURCE FOR CALIBRATION OF THE 5100 AC CONVERTER

Figure 5.3 - AC Source

5.3.6 Familiarization.

5.3.6.1 Read all step-by-step procedures before starting calibration to verify that all required test equipment, tools, and miscellaneous hookup cables are available to perform the calibration procedure. Verify that all test equipment has been under power for the required amount of time prescribed by the manufacturer to attain full accuracy and/or stability.

5.3.7 Warmup.

5.3.7.1 Apply power to the 5100 and allow 1/2 hour of warmup time.

5.3.8 Calibration Points.

5.3.8.1 Calibration points are shown in figure 5.4.

5.3.8.2 Access to the calibration points is by removal of the instrument case. This procedure is performed as follows:

a. Set DMM power switch to OFF.

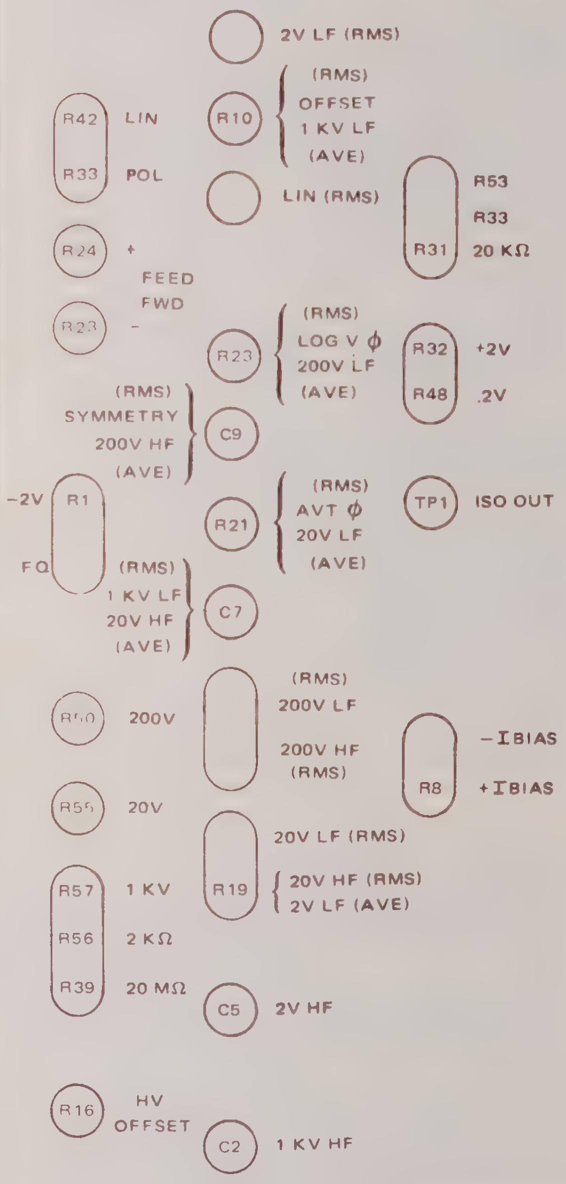
b. Remove line cord from DMM (J201).

c. Remove screws (2) from rear panel.

d. Slide DMM out of case.

e. Replace line cord to J201.

f. Set DMM power switch to ON.


2V LF (RMS)
R10
(RMS)
OFFSET
1 KV LF
(AVE)
R42
LIN
R33
POL
LIN (RMS)
R53
R33
R31
20 KΩ
R24
+
FEED
FWD
R23
-
R23
(RMS)
LOG V ϕ
200V LF
(AVE)
R32
+2V
R48
.2V
(RMS)
SYMMETRY
200V HF
(AVE)
C9
-2V
R1
FQ
R21
(RMS)
AVT ϕ
20V LF
(AVE)
TP1
ISO OUT
(RMS)
1 KV LF
20V HF
(AVE)
C7
R50
200V
(RMS)
200V LF
200V HF
(RMS)
R8
-IBIAS
+IBIAS
R55
20V
20V LF (RMS)
R57
1 KV
R19
20V HF (RMS)
2V LF (AVE)
R56
2 KΩ
R39
20 MΩ
C5
2V HF
R16
HV
OFFSET
C2
1 KV HF

DC CALIBRATION ⚠

(CONNECT MICROVOLTMETER TO ISO OUTPUT REF TO LO SENSE)

	INPUT	MODE	ADJUST
1.	SHORT	2V DC	FRONT PANEL "DC OFFSET"
2.	1 MΩ	2V DC	+IBIAS
	(REPEAT 1 & 2 AS REQUIRED)		
3	SHORT	.2V DC	-IBIAS
	(DISCONNECT METER USE DISPLAY)		
4.	SHORT	2V DC	POL (±)
5.	+100 µV	2V DC	+ FEED FWD (+10 DIGITS)
6.	-100 µV	2V DC	- FEED FWD (-10 DIGITS)
7.	+1V	2V DC	+2V
8.	+1.9V	2V DC	LIN
	(REPEAT 7 & 8 AS REQUIRED)		
9.	-1.9V	2V DC	-2V
10.	SHORT	.2V DC	FRONT PANEL OFFSET ZERO
11.	+.19	.2V DC	.2V
12.	SHORT	20V DC	HV OFFSET
13.	+1000V	1 KV DC	1 KV
14.	+190V	200V DC	200V
15.	+19V	20V DC	20V
16.	+1000V	1 KV DC	1 KV

(NOTE: IF READJUSTED, REPEAT 14 & 15)

4-WIRE OHMS ADJUSTMENT ⚠

	INPUT	MODE	ADJUST
1.	10 KΩ	20 KΩ	20 KΩ
2.	1 KΩ	2 KΩ	2 KΩ
3.	10 MΩ	20 MΩ	20 MΩ

MODEL 5100 DMM

⚠ REFER TO MANUAL FOR DETAILS

WARNING: GUARD VOLTAGE PRESENT ON COVER

Figure 5.4 - Calibration Points

5.3.9 Calibration Procedure.

5.3.9.1 This procedure is designed to produce the highest accuracy in the least number of steps, while minimizing interaction between adjustments. To insure optimum accuracy, no deviation from the order of adjustments in this procedure can be made.

5.3.9.2 ISOLATOR ZERO.

a. Connect a jumper to J101 (Hi) and J102 (Lo) input terminals. J105 (GUARD) is to be connected to J102 (Lo).

b. Set the DMM to the DCV function and 2 range (manual).

c. Connect a microvoltmeter "Hi" input lead to TP1, isolator output on the reference isolator PCB. A hole in the top cover, labeled "ISO OUT," provides access to the TP1 pin using an insulated minigator or capture type test clip. The microvoltmeter "Lo" input lead is connected to the J102/J105 input terminal (analog common).

d. Adjust the FRONT PANEL ZERO, R32, for zero ± 5 μV.

e. Replace the jumper with a 1 MΩ, 5%, 1/4W resistor.

f. Adjust R8, +I (current) Bias, on the Reference Isolator PCB for zero ± 5 μV.

g. Replace the 1 MΩ resistor with a jumper and repeat steps d, e, and f.

h. Remove the microvoltmeter test leads.

5.3.9.3 POLARITY ADJUSTMENT.

a. With the DMM in the DCV function and the input shorted, select the 2 volt range (manual).

b. Visually monitor the DMM polarity LED, and adjust R33, labeled "POL," on the Digitizer PCB for the center of polarity.

NOTE

The center of polarity is the mid-point of the hysteresis when the polarity indicator "bounces" plus and minus approximately 50% of the readings.

5.3.9.4 FEED FORWARD ADJUSTMENT.

a. With the DMM in the DCV function and 2 volt range (manual). Remove the jumper at the input and connect a DC voltage source set to +100 μV.

b. Adjust R24, labeled + FEED FWD, on the Digitizer PCB for a readout of +0.00010 on the display.

c. Reverse the polarity of the input signal (–100 μV). Adjust R23, labeled – FEED FWD, for a readout of –0.00010 on the display. Recheck the Feed Forward adjustments.

d. Apply a +1.00000 volt to the input terminals and adjust R32, labeled +2V, on the Reference Isolator PCB for a readout of +1.00000 on the display.

e. Increase the input voltage to +1.90000. Adjust R42, labeled LIN, on the Digitizer PCB for a readout of +1.90000 on the display.

f. Repeat steps d and e until each step is within ±1 digit of the required reading on the display.

g. Apply a –1.90000 volts to the input terminals and adjust R1, labeled –2V, on the Digitizer PCB for a readout of –1.90000 on the display.

h. Decrease the input voltage to –1.00000 and verify the readout on the display is –1.00000 ± 1 digit.

i. Check steps a through g and adjust, if necessary.

5.3.9.5 DCV RANGE ADJUSTMENTS.

a. Select the .2 range (manual). Remove the signal input cable, replace with a jumper at J101 and J102/J105, and adjust R32, FRONT PANEL ZERO, for a readout of .000000 ± 1 digit on the display, if necessary.

b. Remove the jumper, apply a +.190000 volt input, and adjust R48, labeled .2V, on the Reference Isolator PCB for a readout of +.190000 on the display..

c. Reverse the polarity input (–.190000 volts) and verify a readout of –.190000 ± 2 digits on the display.

d. Select the 2 volt range, replace the signal input with a jumper, and verify a readout of (±)

0.00000 on the display. Repeat steps a, b, and c, if the readout is not zeroes.

e. Select the 20 volt range, replace the signal input with a jumper and adjust R16, labeled HV OFFSET, on the Digitizer PCB for a readout of (±) 00.0000 on the display. Remove the input jumper.

f. Select the 1000 range (manual), apply a +1000.00 volts to the input terminals (J101 and J102/J105). Adjust R57, labeled 1 KV, on the Digitizer PCB for a readout of +1000.00 on the display.

g. Reduce the DC voltage standard to +190.000 volts at the input terminals and select the 200 volt range (manual). Adjust R50, labeled 200V, on the Digitizer PCB for a readout of +190.000 on the display.

h. Reduce the DC voltage standard to +19.0000 volts at the input terminals and select the 20 volt range (manual). Adjust R55, labeled 20V, on the Digitizer PCB for a readout of +19.0000 on the display.

i. Repeat steps f, g, and h and readjust, if necessary.

j. Reduce the voltage standard outputs and remove input cables.

5.3.9.6 4-WIRE KOHMS ADJUSTMENTS.

NOTE

Low sense line must be less than 1 ohm.

a. With the DMM in the DCV function, select the .2 volt range. Connect a jumper to the input terminals and adjust R32, FRONT PANEL ZERO, for a readout of (±) .000000 on the display, if necessary.

b. Connect the DMM as shown in the figure 5.5 test setup.

c. Select the Kohms function and the 20 Kohm range. Connect the DMM to a 10 Kohm resistance standard using a 4-wire, low leakage cable as shown in figure 5.5.

d. Adjust R31, labeled 20 KΩ, on the Reference Isolator for a readout equal to the resistance standard value.

e. Connect the DMM to a 1 Kohm resistance standard, select the 2 Kohm range, and adjust R56, labeled 2 KΩ, on the digitizer PCB for a readout equal to the resistance standard value.

f. Connect the DMM to a 100 ohm resistance standard, select the .2 Kohm range, and verify that the readout is equal to the value of the resistance standard, ± 6 digits.

g. Set the DMM to the 200 Kohm range, connect the DMM input to a 100 Kohm resistance standard, and verify that the readout is equal to the value of the resistance standard, ± 5 digits.

h. Set the DMM to the 2000 Kohm (2 MΩ) range, connect the DMM input to a 1 Mohm resistance standard, and verify that the readout is equal to the value of the resistance standard, ± 6 digits.

i. Set the DMM to the 20,000 Kohm (20 MΩ) range, connect the DMM input to a 10 Mohm resistance standard, select the measurement 3-pole filter, and adjust R39, labeled 20 MΩ, on the digitizer PCB for a readout of 10.0000 on the display.

j. Remove the input cables from the DMM and resistance standard and disable the measurement filter.

5.3.9.7 AC CONVERTER (Averaging).

a. Select the ACV function and the 1000 range. Connect the AC voltage standard source set to 1000V AC @ 1 kHz to the input terminals, J101 (Hi) and J102/J105 (Lo). Adjust R10, labeled 1 KV LF, on the AC converter for a readout of 1000.00 on the display.

b. Increase the frequency of the AC voltage standard to 20 kHz and adjust C2, labeled 1 KV HF, on the AC converter for a readout of 1000.00 on the display.

c. Reduce the output of the AC voltage standard to 1V AC @ 1 kHz, select the 2 volt range, and adjust R19, labeled 2V LF, on the AC converter for a readout of 1.00000 on the display.

d. Increase the frequency of the AC voltage standard to 20 kHz and adjust C5, labeled 2V HF, on the AC converter for a readout of 1.00000 on the display.

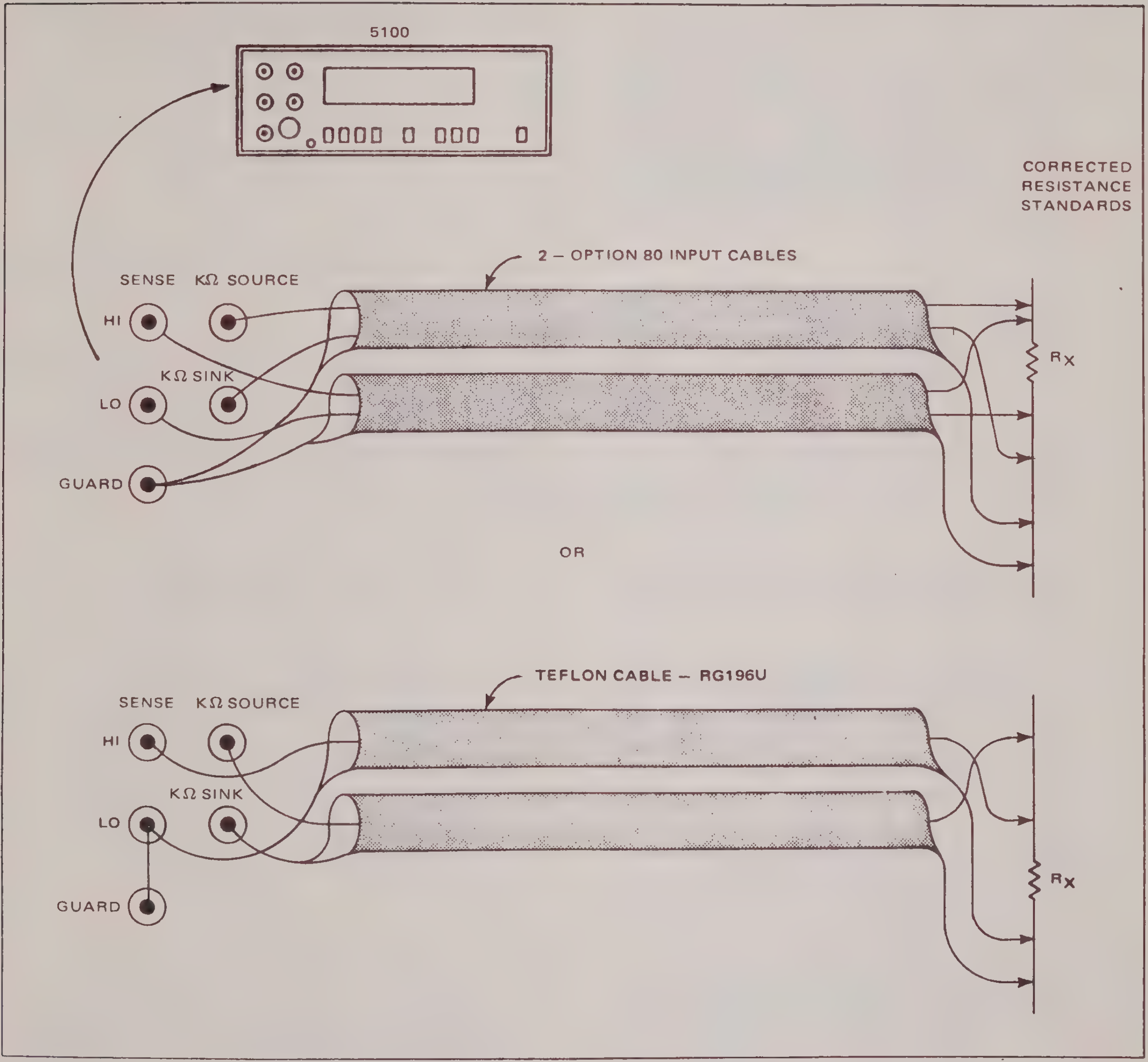

5100
CORRECTED RESISTANCE STANDARDS
2 — OPTION 80 INPUT CABLES
SENSE
KΩ SOURCE
HI
KΩ SINK
LO
GUARD
RX
OR
TEFLON CABLE — RG196U
SENSE
KΩ SOURCE
HI
KΩ SINK
LO
GUARD
RX

Figure 5.5 - Ohms Measurement Connection

e. Select the 20 volt range, increase the output of the AC voltage standard to 10.0000 volts @ 1 kHz, and adjust R21, labeled 20V LF, on the AC converter for a readout of 10.0000 on the display.

f. Increase the frequency of the AC voltage standard to 20 kHz and adjust C7, labeled 20V HF, on the AC converter for a readout of 10.0000 on the display.

g. Select the 200 volt range, increase the output of the AC voltage standard to 100.000 volts @ 1 kHz and adjust R23, labeled 200V LF, on the AC converter for a readout of 100.000 on the display.

h. Increase the frequency of the AC voltage standard to 20 kHz and adjust C9, labeled 200V HF, on the AC converter for a readout of 100.000 on the display.

5.3.9.8 AC CONVERTER (TRUE RMS).

a. Select the ACV function, autorange, and connect a jumper (short) to the input terminals J101 (Hi) and J102/J105 (Lo). The readout on the display must be less than 0.00300. A readout greater than 300 digits indicates that the AVT (Rectifier) Amp and Log Amp must be rezeroed. The zero procedure adjustments are listed in paragraph 5.3.9.9.

b. Remove the jumper from the input terminals and connect the output of an AC Voltage standard set to .1 VAC @ 1 kHz to J101 (Hi) and J102/J105 (Lo). Adjust R38 (OFFSET) for a reading on the display of 0.10000.

c. Increase the AC Voltage standard output to 1 VAC @ 1 kHz and adjust R51 (GAIN LABELED 2V LF) for a reading on the display of 1.00000.

d. Increase the AC Voltage standard output to 1.9 VAC @ 1 kHz and adjust R44 (LIN) for a reading on the display of 1.90000.

e. Temporarily remove the signal input from the AC Voltage standard. Connect a jumper (short) to the input terminals and verify the reading is less than 0.00300 (300 digits). Remove the jumper and reconnect the input terminals to the AC Voltage standard.

f. Manually select the 1000 range, increase the AC Voltage standard output to 1000 VAC @ 1 kHz and adjust R15 (1 KV LF) for a reading on the display of 1000.00.

g. Increase the frequency of the AC Voltage standard to 20 kHz and adjust C4 (1 KV HF) for a reading on the display of 1000.00. Select autorange.

h. Reduce the output of the AC Voltage standard to 1 VAC, increase the frequency to 40 kHz, and adjust C26 (2V HF) for a reading on the display of 1.00000.

i. Increase the output of the AC Voltage standard to 10 VAC, reduce the frequency to 1 kHz, and adjust R13 (20V LF) for a reading on the display of 10.0000.

j. Increase the frequency of the AC Voltage standard to 40 kHz, and adjust C9 (20V HF) for a reading on the display of 10.0000.

k. Increase the output of the AC Voltage standard to 100 VAC @ 1 kHz and adjust R14 (200V LF) for a reading on the display of 100.000.

l. Increase the frequency of the AC Voltage standard to 40 kHz and adjust C12 (200V HF) for a reading on the display of 100.000.

5.3.9.9 5100 TRUE RMS AC CONVERTER AMPLIFIER ZERO ADJUSTMENTS.

These adjustments are required to rezero the AVT (Rectifier) Amp and Log Amp. The adjustments are to be made with the GUARD and AC CONVERTER shields removed, the PCB jumper, W1, connecting the Scaling Amp to the AVT (Rectifier) Amp removed, and the PCB mounted on the AC Converter Extender PCB, P/N 403950, for access to test points.

a. Set R28, R32, R20, R38, R44, and R51 to the center of their adjustment spans and set R22 to its full counter-clockwise (CCW) position.

b. Connect a jumper (short) from TP2 (AVT AMP IN) to TP1 (Mecca ground), connect a jumper (short) from TP4 (LOG AMP OUT) to TP1 (Mecca ground), connect an oscilloscope (Hi) to TP5 (AVT AMP OUT) and (Lo) to TP1 (Mecca ground). Adjust R28 (AVT Voltage zero) for an equally displaced noise envelope about the DC reference on the oscilloscope.

NOTE

A X10 scope probe should be used with the Vertical input set to 50 mV/div. If a X1 probe is used (.5V/div) the (Hi) input lead must be dc-coupled with a 10 Kohm, 5% 1/4W, resistor to prevent loading and, possibly, oscillation.

c. Remove the jumper from TP4 to TP1, connect the oscilloscope (Hi) to TP3 (LOG AMP OUT) and adjust R32 (LOG AMP Voltage Zero) for approximately +1V DC (2 vertical divisions above the zero DC reference on the scope).

d. Adjust R22 (LOG AMP Current Zero) for approximately (minus) –.2V DC. Reduce the scopes Vertical input to .2V/div. and adjust one vertical division below the zero DC reference.

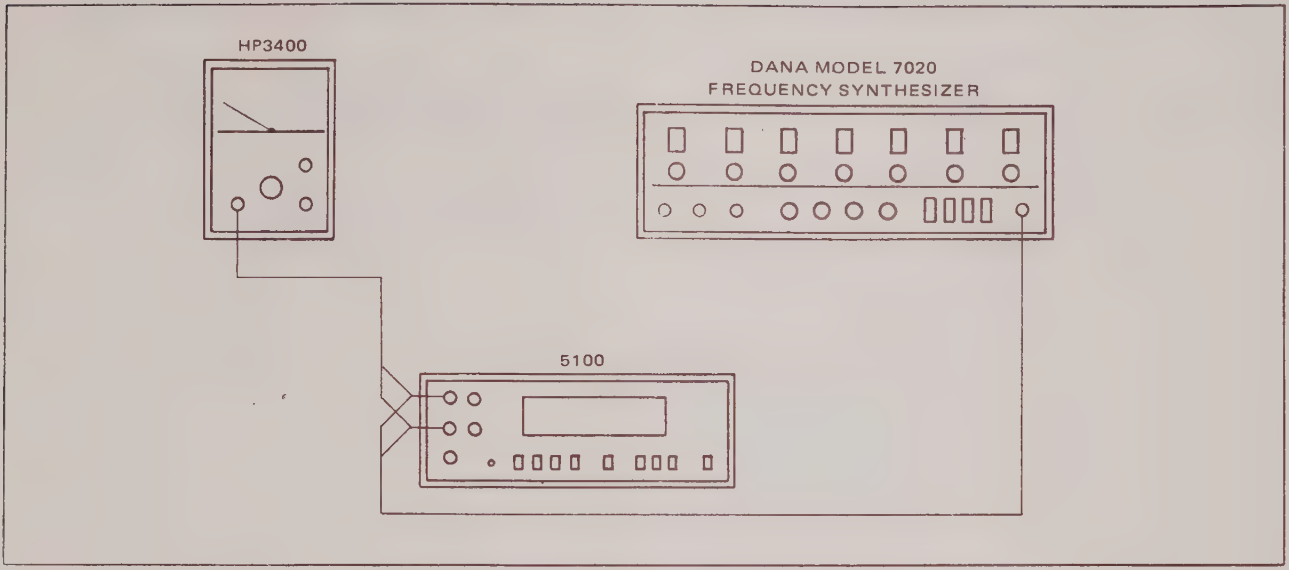


Figure 5.6 - kHz Calibration Connection, Part 1

e. Remove the jumpers (shorts) and the oscilloscope input leads. Connect the output of a DC Voltage standard, set to +1 VDC, to TP2 (Hi) and TP1 (Lo) and record the reading on the DMM display.

f. Reverse the polarity of the output from the DC Voltage standard and adjust R20 for value recorded in step e.

g. Repeat steps e and f until the readings are within 2 digits of the value recorded in step e.

h. Remove the leads from the DC Voltage standard.

i. Connect a jumper (short) from TP2 (AVT AMP IN) to TP1 (Mecca ground) and verify the reading on the DMM display is less than 0.00300 (300 digits).

j. Disable the Power switch (OFF), remove the assembly from the Extender PCB, replace the jumper (W1), replace the AC Converter shield, reinstall assembly in the DMM, replace the Guard shield, and enable the DMM Power switch (ON).

k. Proceed with the calibration procedure outlined in paragraph 5.3.9.8.

5.3.9.10 FREQUENCY.

a. Select the Frequency function and manually downrange to the 2000.00 Kohm (2 MHz) range.

b. Connect the output of a Dana Model 7020, Frequency Synthesizer (or equivalent), to the input (J101, Hi and J102/J105, Lo) of the DMM under calibration and to the input of an HP3400, true RMS Voltmeter (or equivalent), as shown in figure 5.6.

c. Adjust the output of the 7020 Synthesizer for a frequency of 1 kHz at approximately 250 mV RMS (25 dB attenuation) on the HP3400 Voltmeter.

d. Remove the DMM Guard shield and connect an oscilloscope X10 probe (to prevent loading) input (Hi) to U5-13 (Frequency Signal Conditioner Out) referenced to TP3 (DIGITAL COMMON) on the main PCB Assembly.

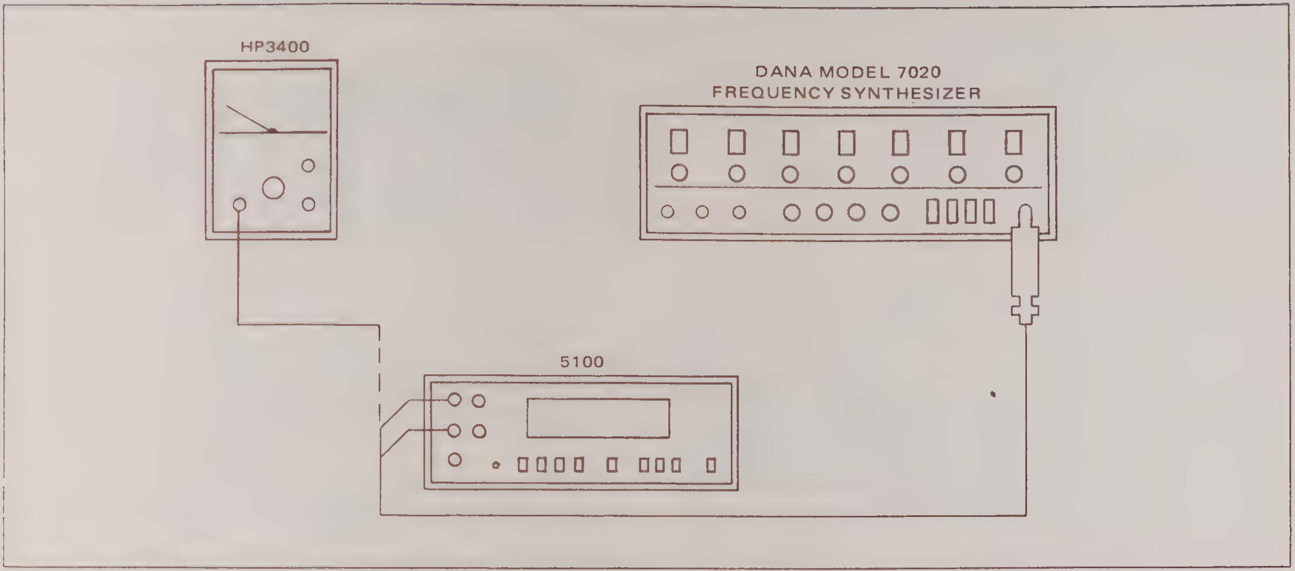


Figure 5.7 - kHz Calibration Connection, Part 2

e. Adjust R34, main PCB assembly, for a symmetrical squarewave on the oscilloscope.

f. Remove the oscilloscope probe, decrease the output amplitude of the synthesizer, and readjust R34 for a reading on the display of 0001.00.

g. Decrease the synthesizer output and, again, fine tune R34 for the correct reading on the display.

NOTE

This is a sensitivity adjustment and should be repeated until the adjustment of R34 no longer affects the reading on the display (approximately 200 mV RMS).

h. Verify that the DMM reads input signals from 10 Hz to 10 MHz with a sensitivity of less than 300 mV RMS.

i. Connect the DMM input to the output of a Frequency Doubler, HP10515A (50Ω load), connected to the output of the synthesizer, set to 9.5 MHz, as shown in figure 5.7.

j. Adjust the output of the synthesizer for maximum output (0 dB) amplitude at a frequency of 19 MHz.

NOTE

The DMM (for the Frequency function) upranges, in Autorange, between 2 MHz and 5 MHz.

NOTE

The DMM must be manually upranged for input frequencies above 5 MHz.

k. Verify that the reading on the display is approximately 19000.0 kHz (19 MHz). Adjust R2, FQ on the Digitizer PCB assembly, for a reading on the display of 19000.0 kHz. Replace the DMM Guard shield.

l. Decrease the synthesizer output until the reading on the display starts to break up, remove the input cable to the DMM, and connect to the input of the HP3400, RMS Voltmeter (or equivalent). Verify that the amplitude of the synthesizer output signal is less than 300 mV RMS.

5.4 TROUBLESHOOTING PERFORMANCE TESTS.

5.4.1 This section contains Unit and Subassembly performance tests. The unit performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the unit test is designed to isolate the malfunction to a functional area of the board.

The unit performance tests are organized by instrument function such as AC volts, DC volts or Kohms. A "singlethread" diagram is provided for each of the unit performance tests. These diagrams show the primary signal path through the instrument for the individual function of the instrument.

5.4.2 The subassembly performance tests are designed to isolate a malfunction to a component or small group of components on a printed circuit board.

These tests are organized by subassembly such as the display PCB or the AC converter board.

5.4.3 Both the unit and subassembly performance tests present test setup instructions, step by step instructions for monitoring the circuit under test and performance standards in the form of voltage levels or oscilloscope waveforms. In addition the tests are fully illustrated by either the "singlethread" diagrams or schematics which illustrate the test point location within the circuit under test. For ease in locating the physical test point within the instrument, pictorial drawings are provided on pages facing the schematic.

5.4.4 Test points called out in the performance tests may be actual physical test points provided as convenience test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares or diamonds. These "flags" also appear on the corresponding schematic and on the pictorial drawing in the Drawing section of this manual.

5.4.5 Note that the test points are numbered sequentially so as to start at the input of a circuit and progress to the output. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags 1 appearing on the assembly drawing and schematics in the Drawing Section (6). These black square test point flags indicate voltage measurement points. Similarly the alphabetic test points refer to black diamond shaped flags A appearing on the assembly drawings and schematics. The Alphabetic diamond flags indicate oscilloscope test points.

5.4.6 To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

5.4.7 Unit Performance Tests.

5.4.7.1 Tables 5.7 through 5.10 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to 5%.

5.4.7.2 The performance tests presented in this section are:

DC Volts Unit Performance Test	Table 5.7
AC Volts (Averaging & True RMS) Unit Performance Test	Table 5.8
Kohms Unit Performance Test	Table 5.9
kHz Unit Performance Test	Table 5.10

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

Table 5.7 - DCV Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .2 (manual) Input Terminals: J10 (Hi) and J102 (Lo) connected to a DC voltage standard set to ±0.19900V					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Use of DC active filter, S6, optional. NOTE: Guard (J105) to be strapped to Sig Lo (J102).
	DC Voltage Input	S1-B-2	1	Figure 5.9	±0.199000V DC ± Tol.
	Isolator Input	E26	2	Figure 5.9	±0.199000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.9	±1.99000V DC ± Tol.
Range: 2 (manual) Set DC voltage standard to ±1.99000V	DC Voltage Input	S1-B-2	1	Figure 5.9	±1.99000V DC ± Tol.
	Isolator Input	E26	2	Figure 5.9	±1.9900V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.9	±1.99000V DC ± Tol.
Range: 20 (manual) Set DC voltage standard to ±19.9000V	DC Voltage and HV Buffer Input	S2-B-2	4	Figure 5.9	±19.9000V DC ± Tol.
	Attenuator Input	S2-A-2	5	Figure 5.9	±19.9000V DC ± Tol.
	Attenuator and Isolator Input	E26	2	Figure 5.9	±1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.9	±1.99000V DC ± Tol.
Range: 200 (manual) Set DC voltage standard to ±199.000V	DC Voltage and HV Buffer Input	S2-B-2	4	Figure 5.9	±199.000V DC ± Tol.
	Attenuator Input	S2-A-2	5	Figure 5.9	±199.000V DC ± Tol.

Table 5.7 - DCV Unit Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Attenuator Output and Isolator Output	E26	2	Figure 5.9	±1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.9	±1.99000V DC ± Tol.
Range: 1000 (manual) Set DC voltage standard to ±1000.00V	DC Voltage Input and 9 MΩ Divider Resistor	S3-B-2	6	Figure 5.9	±1000.00V DC ± Tol.
	Attenuator Input	S2-A-2	5	Figure 5.9	±100.000V DC ± Tol.
	Attenuator Output and Isolator Input	E26	2	Figure 5.9	±1.00000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.9	±1.00000V DC ± Tol.
Reduce DC voltage standard to 0V					

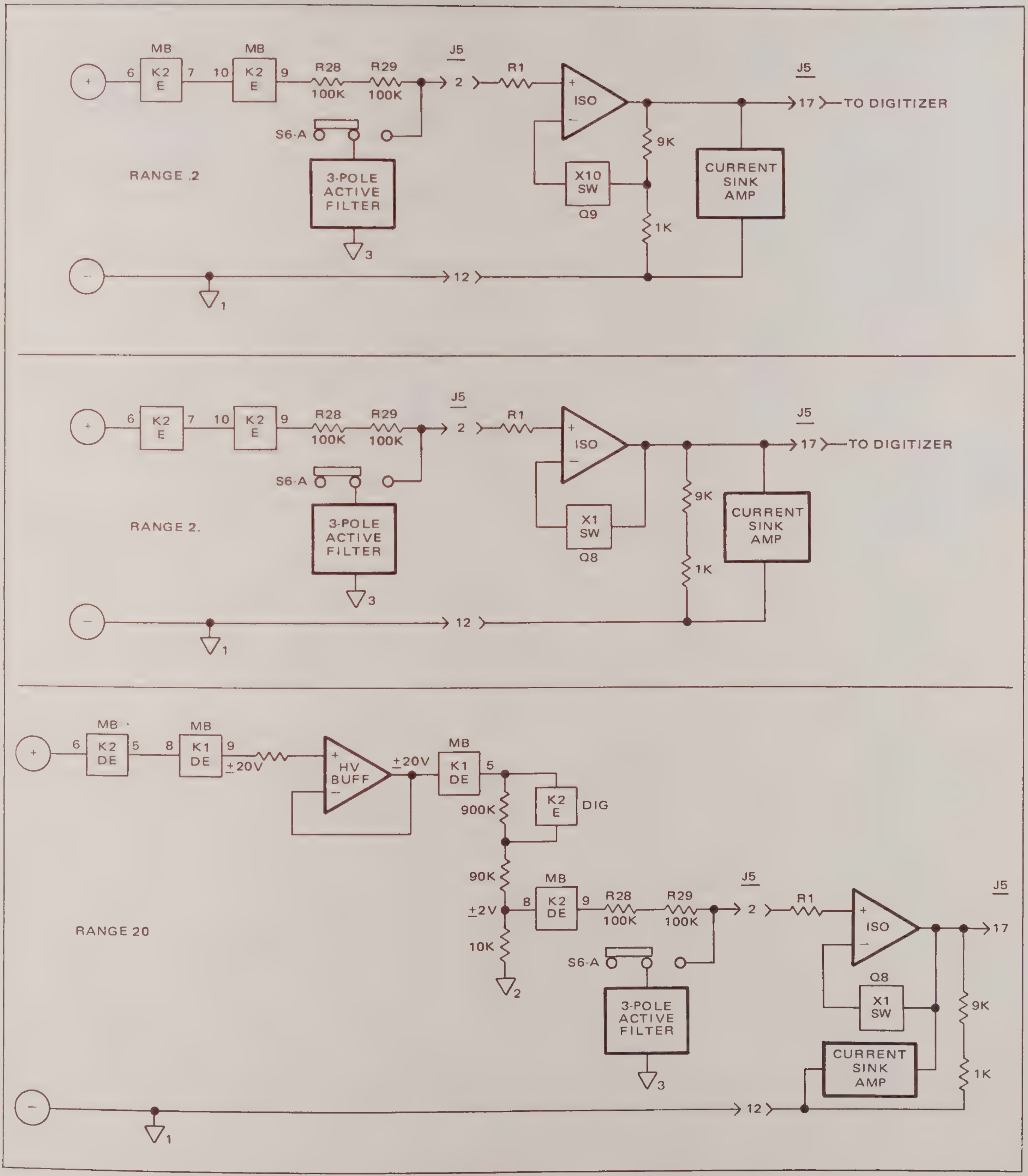

MB
K2
E
6
7
10
MB
K2
E
9
R28
100K
R29
100K
J5
2
R1
ISO
J5
17
TO DIGITIZER
S6-A
9K
3-POLE
ACTIVE
FILTER
X10
SW
Q9
CURRENT
SINK
AMP
1K
3
RANGE .2
12
1
K2
E
R28
100K
R29
100K
J5
2
R1
ISO
J5
17
TO DIGITIZER
S6-A
9K
3-POLE
ACTIVE
FILTER
X1
SW
Q8
CURRENT
SINK
AMP
1K
RANGE 2.
12
MB
K2
DE
5
8
MB
K1
DE
9
±20V
HV
BUFF
±20V
MB
K1
DE
5
900K
K2
E
DIG
90K
MB
K2
DE
8
9
±2V
R28
100K
R29
100K
J5
2
R1
ISO
J5
17
10K
S6-A
Q8
X1
SW
9K
3-POLE
ACTIVE
FILTER
CURRENT
SINK
AMP
1K
RANGE 20
12
2
3
1

Figure 5.8 - DCV Simplified Schematic, .2, 2, 20 Ranges

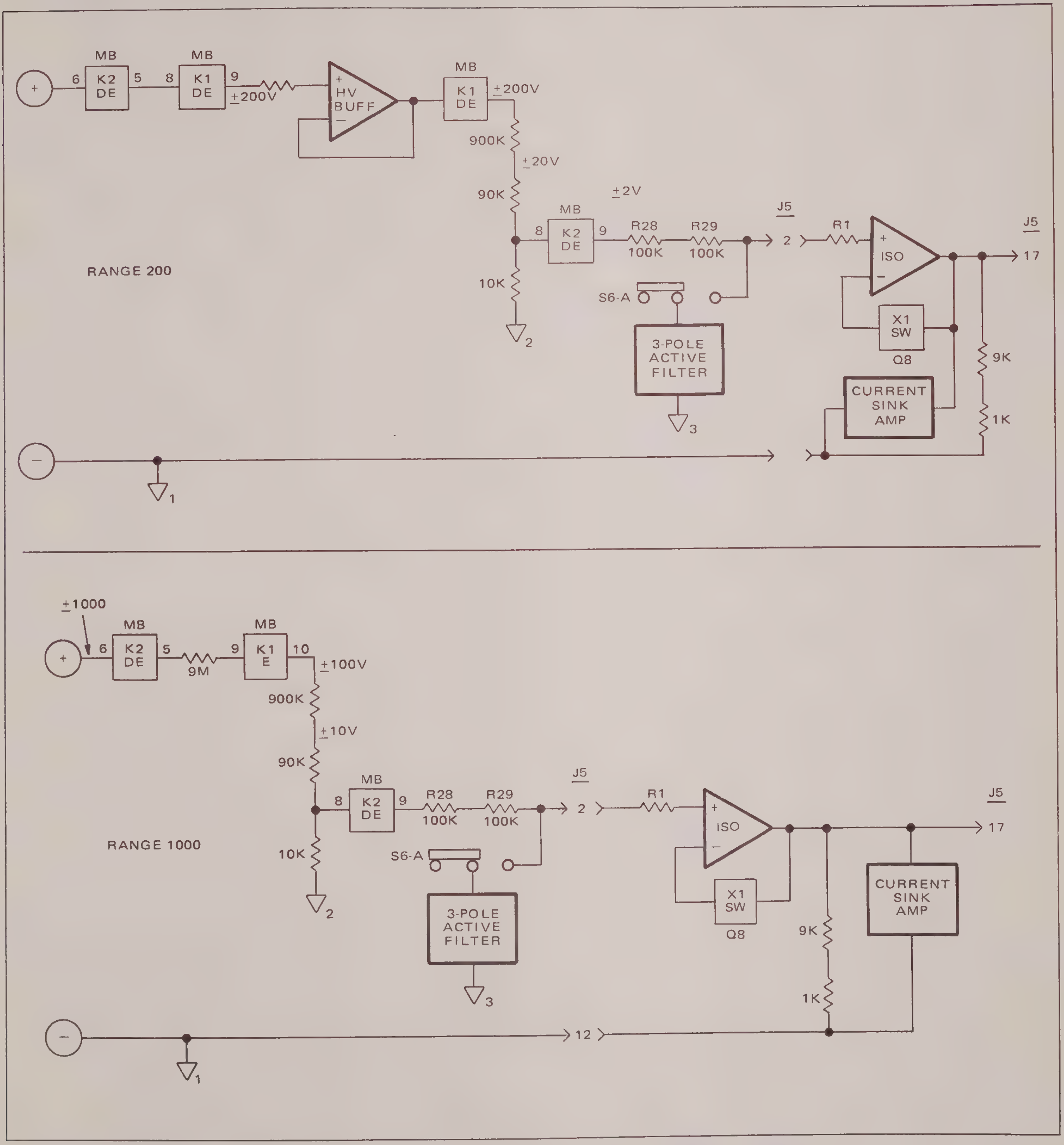
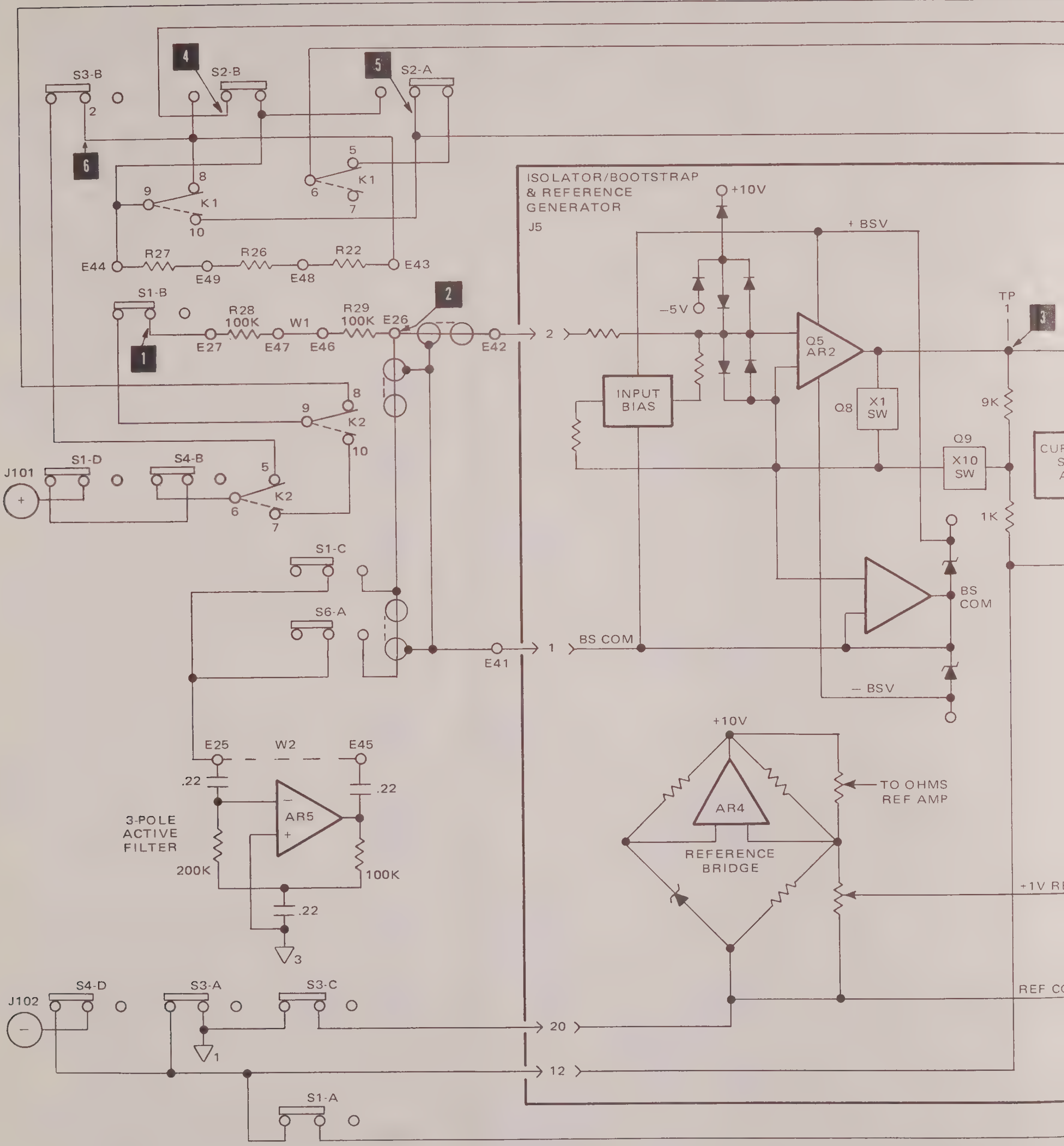

MB
K2
DE
6
5
MB
K1
DE
8
9
±200V
HV
BUFF
+
−
MB
K1
DE
±200V
900K
±20V
90K
±2V
MB
K2
DE
8
9
R28
100K
R29
100K
J5
2
R1
ISO
J5
17
RANGE 200
10K
2
S6-A
3-POLE
ACTIVE
FILTER
3
X1
SW
Q8
9K
CURRENT
SINK
AMP
1K
1
±1000
MB
K2
DE
6
5
9M
MB
K1
E
9
10
±100V
900K
±10V
90K
MB
K2
DE
8
9
R28
100K
R29
100K
J5
2
R1
ISO
J5
17
RANGE 1000
10K
2
S6-A
3-POLE
ACTIVE
FILTER
3
X1
SW
Q8
9K
CURRENT
SINK
AMP
1K
12
1

Figure 5.8 - DCV Simplified Schematic, 200, 1000 Volt Ranges continued


S3-B
2
6
4
S2-B
5
S2-A
8
9
K1
10
5
K1
6
7
E44
R27
E49
R26
E48
R22
E43
S1-B
R28
100K
W1
R29
100K
E26
2
E27
E47
E46
E42
1
8
9
K2
10
J101
S1-D
S4-B
5
K2
6
7
S1-C
S6-A
E41
E25
W2
E45
.22
.22
3-POLE
ACTIVE
FILTER
AR5
200K
100K
.22
3
J102
S4-D
S3-A
S3-C
1
S1-A
ISOLATOR/BOOTSTRAP
& REFERENCE
GENERATOR
J5
+10V
+ BSV
–5V
INPUT
BIAS
Q5
AR2
Q8
X1
SW
TP
1
3
9K
Q9
X10
SW
CUR
S
A
1K
BS
COM
BS COM
– BSV
+10V
TO OHMS
REF AMP
AR4
REFERENCE
BRIDGE
+1V R
REF C
2
1
20
12

	MAIN PCB RLYS		DIGITIZER RLYS			ISO GAIN
	K1	K2	K1	K2	K3	
.2		▨				X10
2		▨				X1
20				▨		X1
200						X1
1000	▨					X1

EN

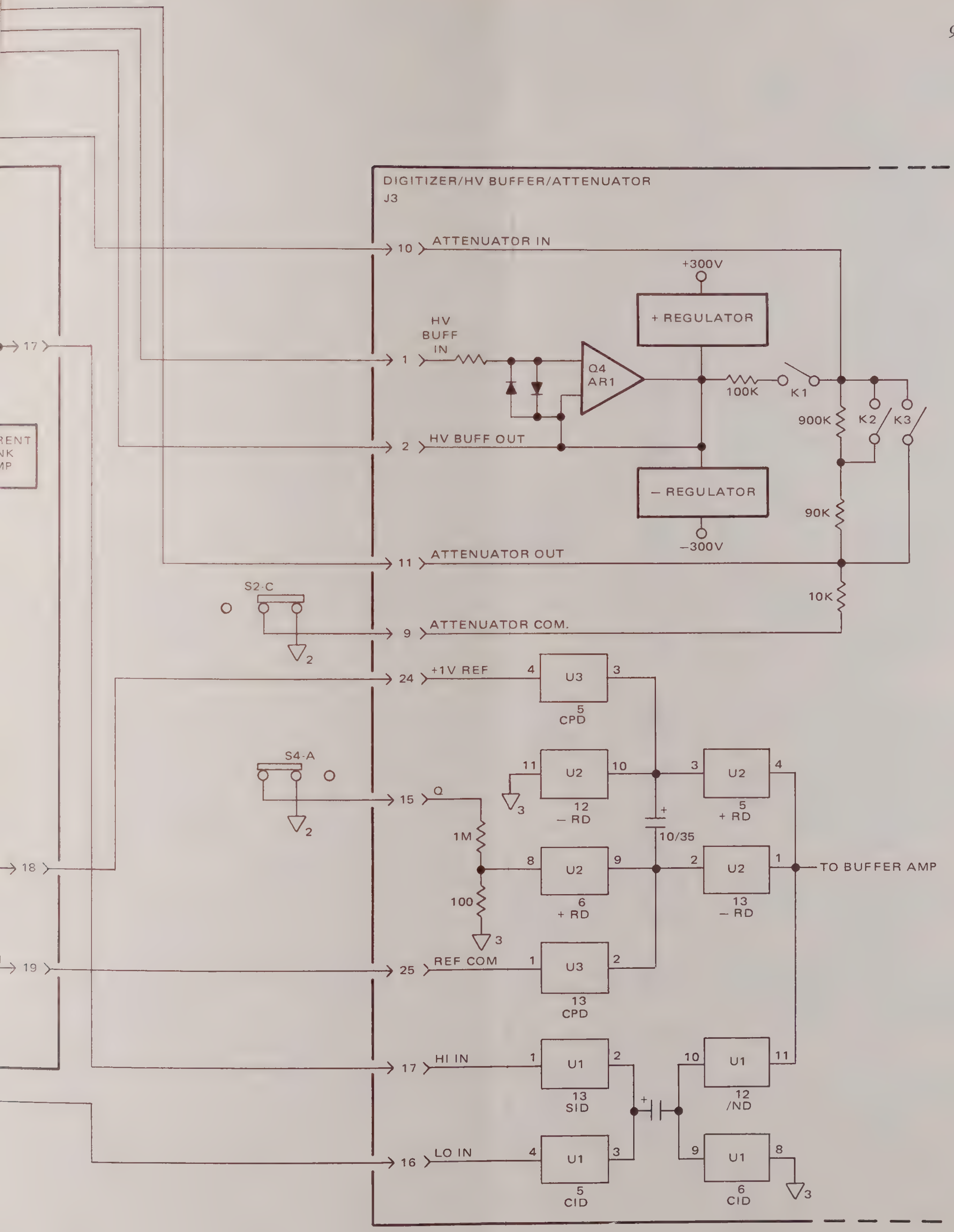
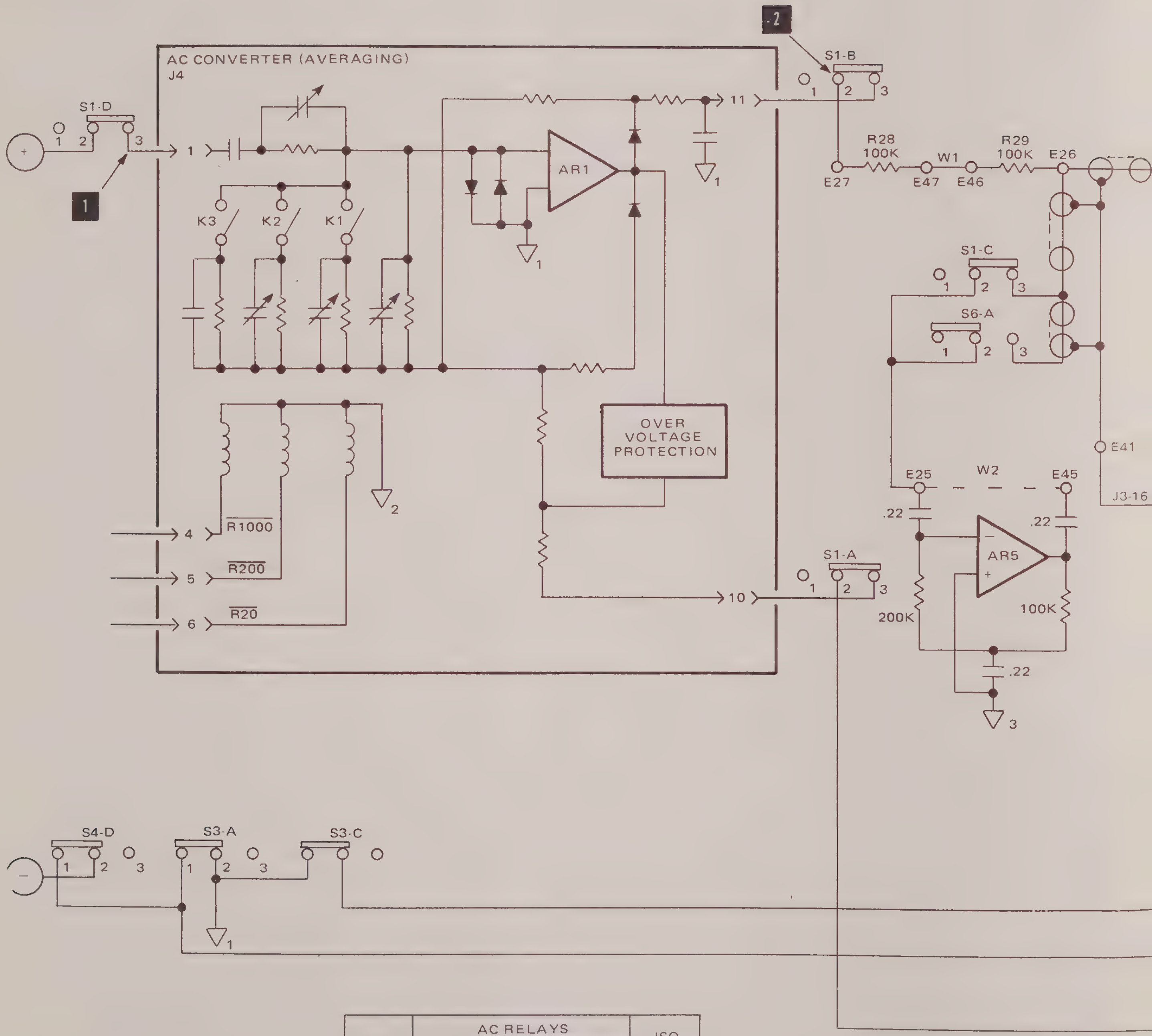

DIGITIZER/HV BUFFER/ATTENUATOR
J3
10
ATTENUATOR IN
+300V
+ REGULATOR
HV
BUFF
IN
1
Q4
AR1
100K
K1
900K
K2
K3
2
HV BUFF OUT
– REGULATOR
90K
–300V
11
ATTENUATOR OUT
10K
S2-C
2
9
ATTENUATOR COM.
24
+1V REF
4
U3
3
5
CPD
S4-A
11
U2
10
3
U2
4
3
12
– RD
5
+ RD
15
Q
10/35
2
1M
8
U2
9
2
U2
1
TO BUFFER AMP
100
6
+ RD
13
– RD
3
25
REF COM
1
U3
2
13
CPD
17
HI IN
1
U1
2
10
U1
11
13
SID
12
/ND
16
LO IN
4
U1
3
9
U1
8
5
CID
6
CID
3
17
18
19
RENT
NK
MP
GIZED

Figure 5.9 - DCV Single Thread Diagram

Table 5.8 - ACV Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: 2 (manual) Input Terminals: J101 (Hi) and J102 (Lo) connected to an AC voltage standard set to 1.99000V @ 10 kHz					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Frequency of input signal optional NOTE: Guard (J105) to be strapped to Sig Lo (J102)
	AC Signal Input	S1-D-3	1	Figure 5.10/5.11	1.9900V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2	Figure 5.10/5.11	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.10/5.11	+1.99000V DC ± Tol.
Range: 20 (manual) Set AC voltage standard to 19.9000V @ 10 kHz	AC Signal Input	S1-D-3	1	Figure 5.10/5.11	19.9000V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2	Figure 5.10/5.11	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.10/5.11	+1.99000V DC ± Tol.
Range: 200 (manual) Set AC voltage standard to 199.000V @ 10 kHz	AC Signal Input	S1-D-3	1	Figure 5.10/5.11	199.000V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2	Figure 5.10/5.11	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.10/5.11	+1.99000V DC ± Tol.
Range: 1000 (manual) Set AC voltage standard to 1000V @ 10 kHz	AC Signal Input	S1-D-3	1	Figure 5.10/5.11	1000.00V AC ± Tol.
	AC Converter Output and Isolator Input	S1-B-2	2	Figure 5.10/5.11	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.10/5.11	+1.99000V DC ± Tol.
Reduce AC voltage standard to 0V					


AC CONVERTER (AVERAGING)
J4
S1-D
1
2
3
1
+
AR1
K3
K2
K1
1
1
11
2
S1-B
1
2
3
R28
100K
W1
R29
100K
E26
E27
E47
E46
S1-C
1
2
3
S6-A
1
2
3
OVER VOLTAGE PROTECTION
2
4
R1000
5
R200
6
R20
10
S1-A
1
2
3
E41
E25
W2
E45
J3-16
.22
.22
AR5
−
+
200K
100K
.22
3
S4-D
1
2
3
S3-A
1
2
3
S3-C
−
1

RNG	AC RELAYS			ISO GAIN
	K1	K2	K3	
2				X1
20	▨			X1
200		▨		X1
1000			▨	X1

ENERGIZED ▨

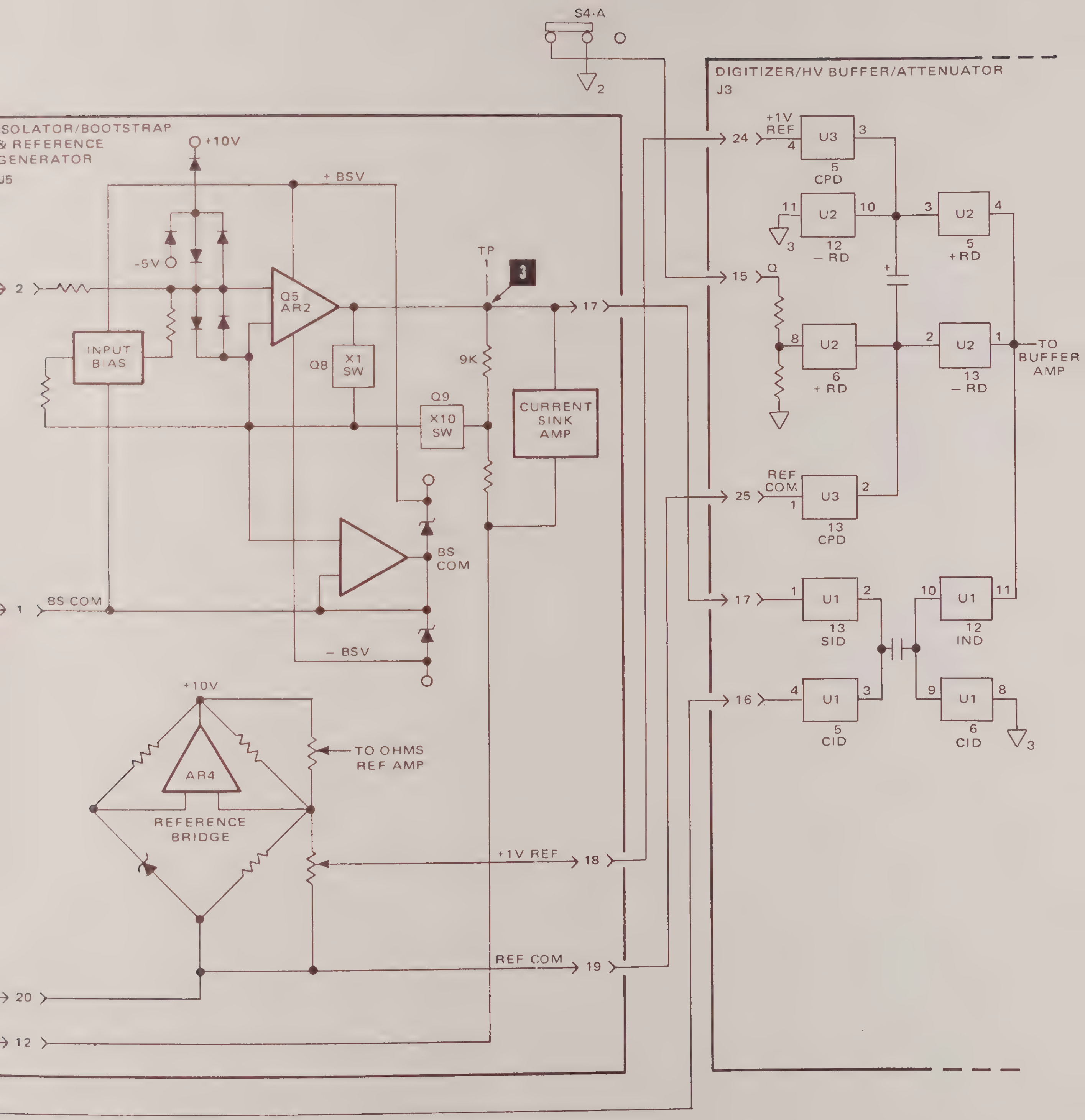
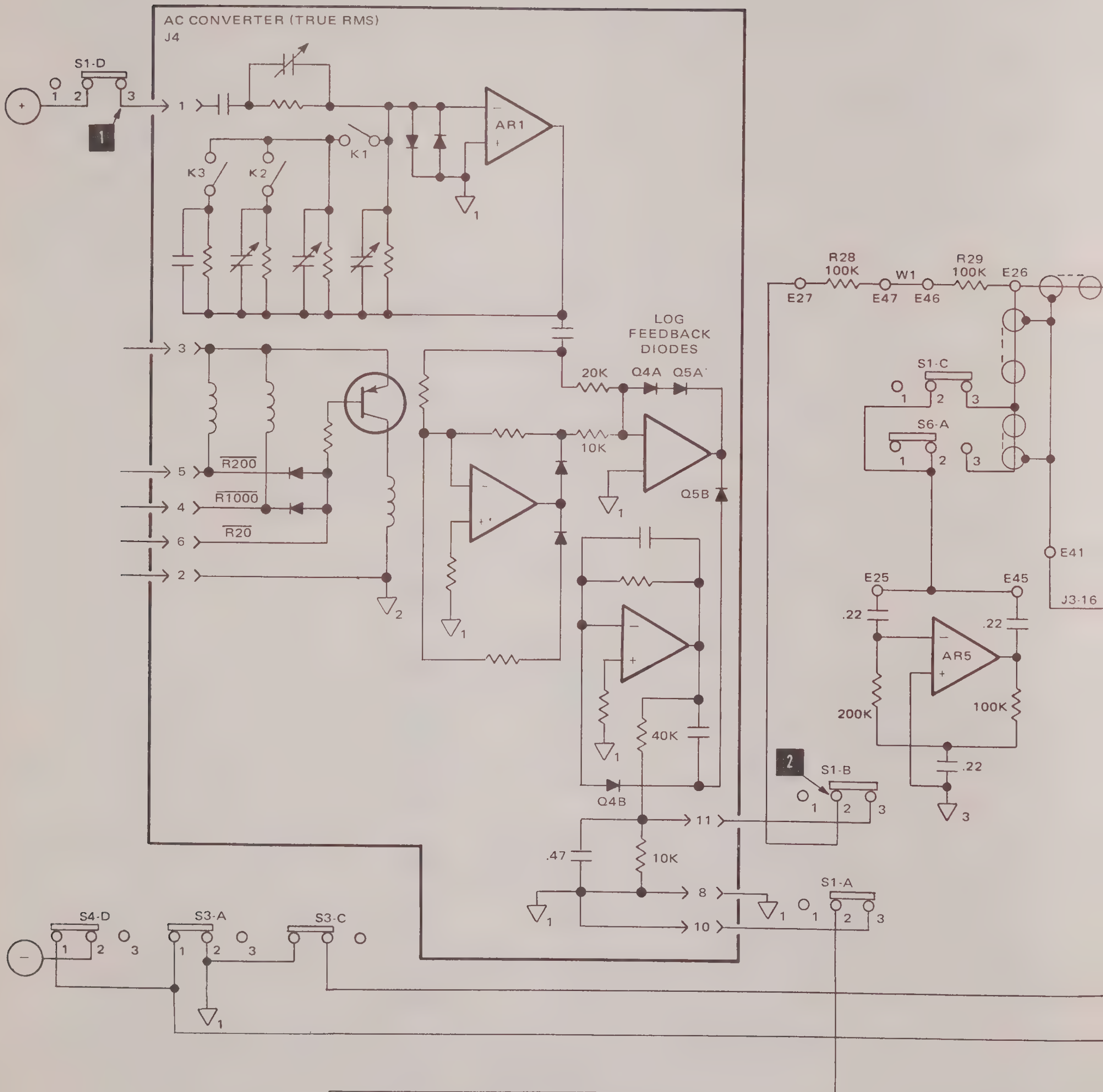

S4-A
2
DIGITIZER/HV BUFFER/ATTENUATOR
J3
SOLATOR/BOOTSTRAP
& REFERENCE
GENERATOR
J5
+10V
+ BSV
-5V
2
INPUT BIAS
Q5
AR2
TP
1
3
17
9K
Q8
X1
SW
Q9
X10
SW
CURRENT
SINK
AMP
BS
COM
BS COM
1
– BSV
+10V
AR4
TO OHMS
REF AMP
REFERENCE
BRIDGE
+1V REF
18
REF COM
19
20
12
24
+1V
REF
4
U3
3
5
CPD
11
U2
10
3
12
– RD
3
U2
4
5
+ RD
15
Q
+
8
U2
6
+ RD
2
U2
1
13
– RD
TO
BUFFER
AMP
25
REF
COM
1
U3
2
13
CPD
17
1
U1
2
13
SID
10
U1
11
12
IND
16
4
U1
3
5
CID
9
U1
8
6
CID
3

Figure 5.10 - ACV (Averaging) Single Thread Diagram


AC CONVERTER (TRUE RMS)
J4
S1-D
1
2
3
1
AR1
K1
K3
K2
1
3
5
4
6
2
R200
R1000
R20
2
1
LOG
FEEDBACK
DIODES
20K
Q4A
Q5A
10K
Q5B
1
1
40K
Q4B
11
.47
10K
8
10
1
R28
100K
W1
R29
100K
E26
E27
E47
E46
S1-C
1
2
3
S6-A
1
2
3
E41
E25
E45
J3-16
.22
.22
AR5
200K
100K
.22
3
2
S1-B
1
2
3
S1-A
1
2
3
1
S4-D
1
2
3
S3-A
1
2
3
S3-C
1

RNG	AC RELAYS			ISO GAIN
	K1	K2	K3	
2				X1
20	▨			X1
200	▨	▨		X1
1000	▨		▨	X1

ENERGIZED ▨

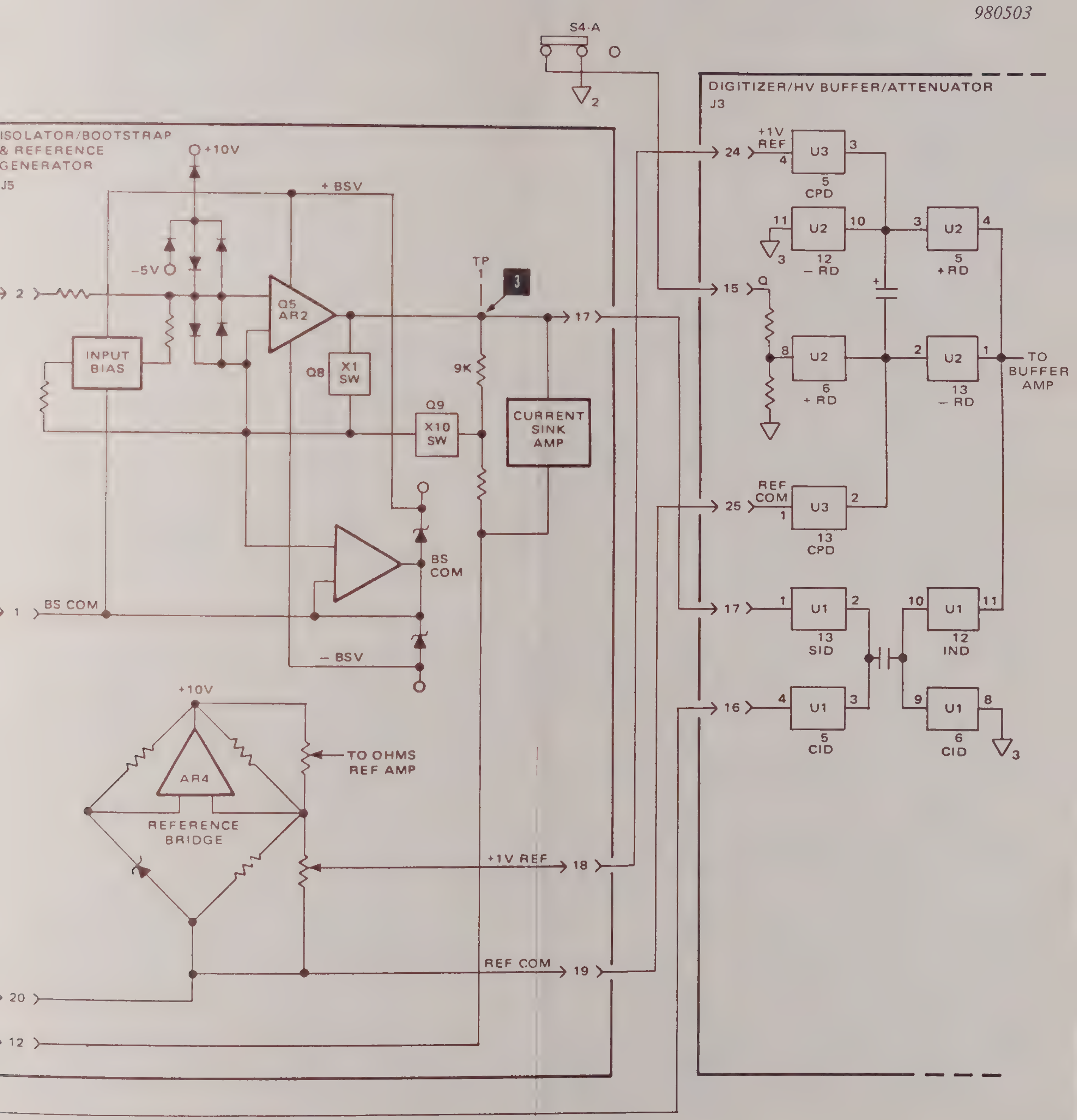

980503
S4-A
2
DIGITIZER/HV BUFFER/ATTENUATOR
J3
ISOLATOR/BOOTSTRAP
& REFERENCE
GENERATOR
J5
+10V
+ BSV
-5V
2
Q5
AR2
TP
1
3
17
INPUT
BIAS
Q8
X1
SW
9K
Q9
X10
SW
CURRENT
SINK
AMP
BS
COM
1
BS COM
- BSV
+10V
AR4
REFERENCE
BRIDGE
TO OHMS
REF AMP
+1V REF
18
REF COM
19
20
12
24
+1V
REF
4
U3
3
5
CPD
11
U2
10
3
12
- RD
3
U2
4
5
+ RD
15
Q
8
U2
6
+ RD
2
U2
1
13
- RD
TO
BUFFER
AMP
25
REF
COM
1
U3
2
13
CPD
17
1
U1
2
13
SID
10
U1
11
12
IND
16
4
U1
3
5
CID
9
U1
8
6
CID
3

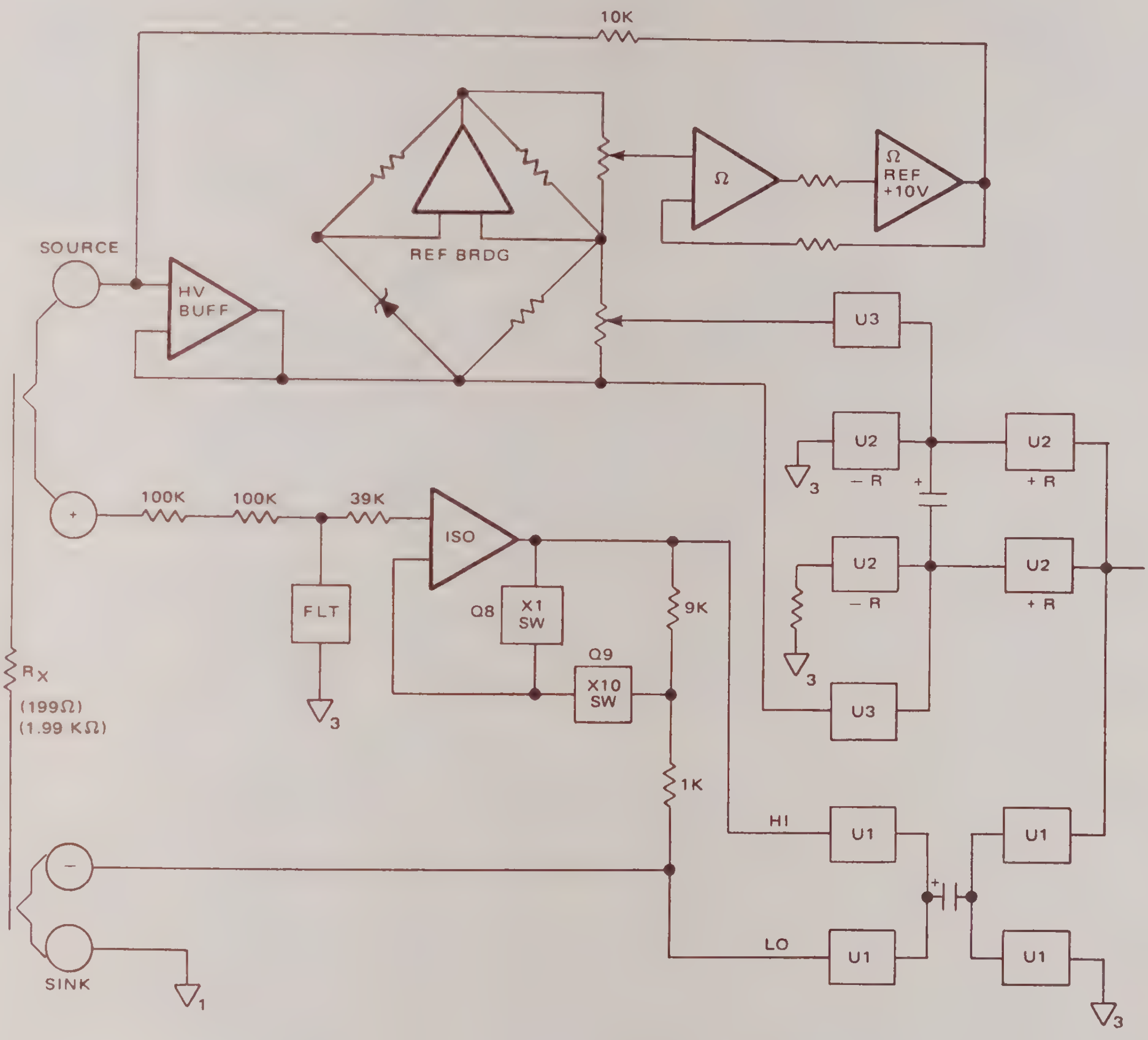
Figure 5.11 - ACV (True RMS) Single Thread Diagram

Table 5.9 - KΩ Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: KΩ Range: .2 (manual) Input Terminals: J101 (Hi)/J103 (Ω Source) and J102 (Lo)/J104 (Ω -Sink) connected to a resistance standard set to 199.00Ω					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Guard (J105) to be strapped to Sig Lo (J102) NOTE: Use of the DC active filter, S6, is optional
	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+10.1900V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+0.19900V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.
Range: 2 (manual) Set resistance standard to 1.99 KΩ	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+11.990V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.
Range: 20 (manual) Set resistance standard to 19.9 KΩ	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+11.990V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.
Range: 200 (manual) Set resistance standard to 199 KΩ	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+11.990V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.

Table 5.9 - KΩ Unit Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Range: 2000 (manual) Set resistance standard to 1.99 MΩ	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+11.990V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.
Range: 20,000 (manual) Set resistance standard to 19.9 MΩ	KΩ Reference Voltage	S2-C-1	1	Figure 5.16	+11.990V DC ± Tol.
	Isolator Input	S1-B-2	2	Figure 5.16	+1.99000V DC ± Tol.
	Isolator Output	TP1, Reference-Isolator Assy.	3	Figure 5.16	+1.99000V DC ± Tol.


10K
Ω
REF +10V
REF BRDG
SOURCE
HV BUFF
U3
U2
– R
+ R
+
3
100K
100K
39K
ISO
Q8
X1 SW
Q9
X10 SW
9K
1K
FLT
RX
(199Ω)
(1.99 KΩ)
HI
LO
U1
SINK
1

RNG	ISO GAIN
.2 KΩ	X10
2 KΩ	X1

SOURCE CURRENT EQUALS 1 mA

Figure 5.12 - KΩ Simplified Schematic, .2, 2 KΩ Ranges

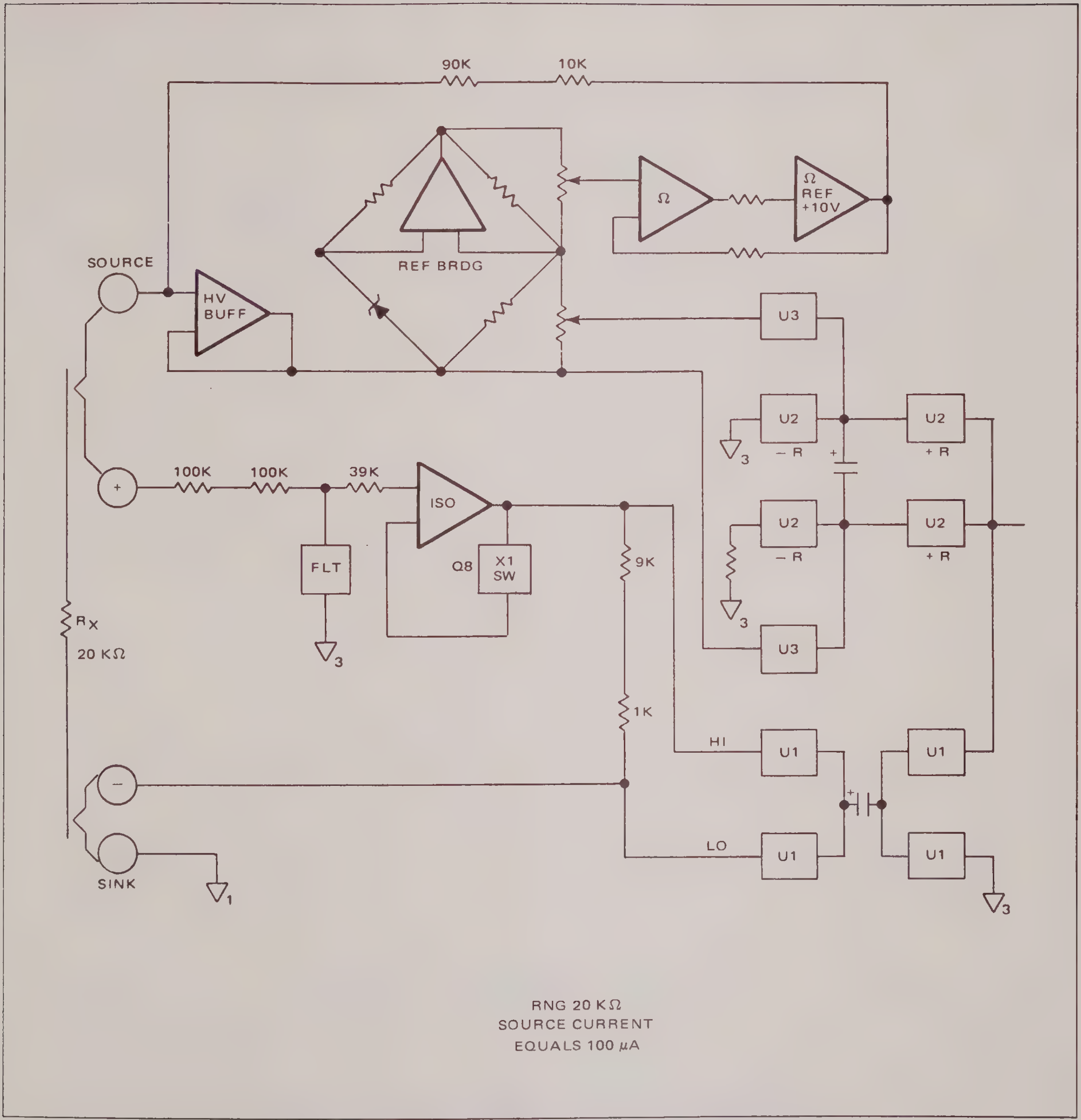

90K
10K
Ω
Ω
REF
+10V
REF BRDG
SOURCE
HV
BUFF
U3
U2
– R
U2
+ R
U2
– R
U2
+ R
U3
100K
100K
39K
ISO
FLT
Q8
X1
SW
9K
1K
R X
20 KΩ
HI
LO
U1
U1
U1
U1
SINK
RNG 20 KΩ
SOURCE CURRENT
EQUALS 100 μA

Figure 5.13 - KΩ Simplified Schematic, 20 KΩ Range

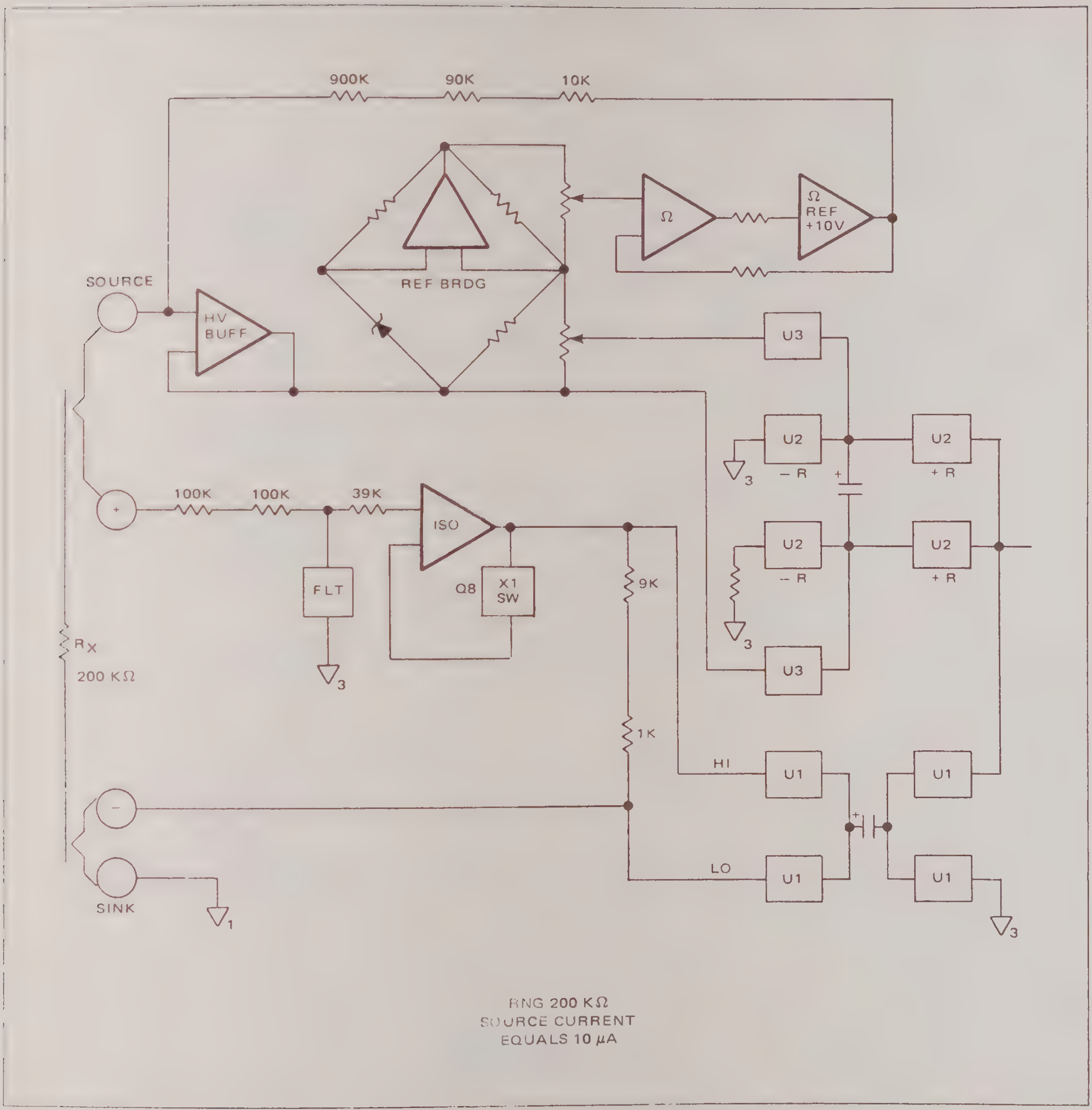

900K
90K
10K
Ω
Ω
REF
+10V
REF BRDG
SOURCE
HV
BUFF
U3
U2
– R
+
U2
+ R
3
+
100K
100K
39K
ISO
FLT
Q8
X1
SW
9K
U2
– R
U2
+ R
3
U3
R_X
200 KΩ
3
1K
HI
U1
U1
+
–
LO
U1
U1
SINK
1
3
RNG 200 KΩ
SOURCE CURRENT
EQUALS 10 μA

Figure 5.14 - KΩ Simplified Schematic, 200 KΩ Range

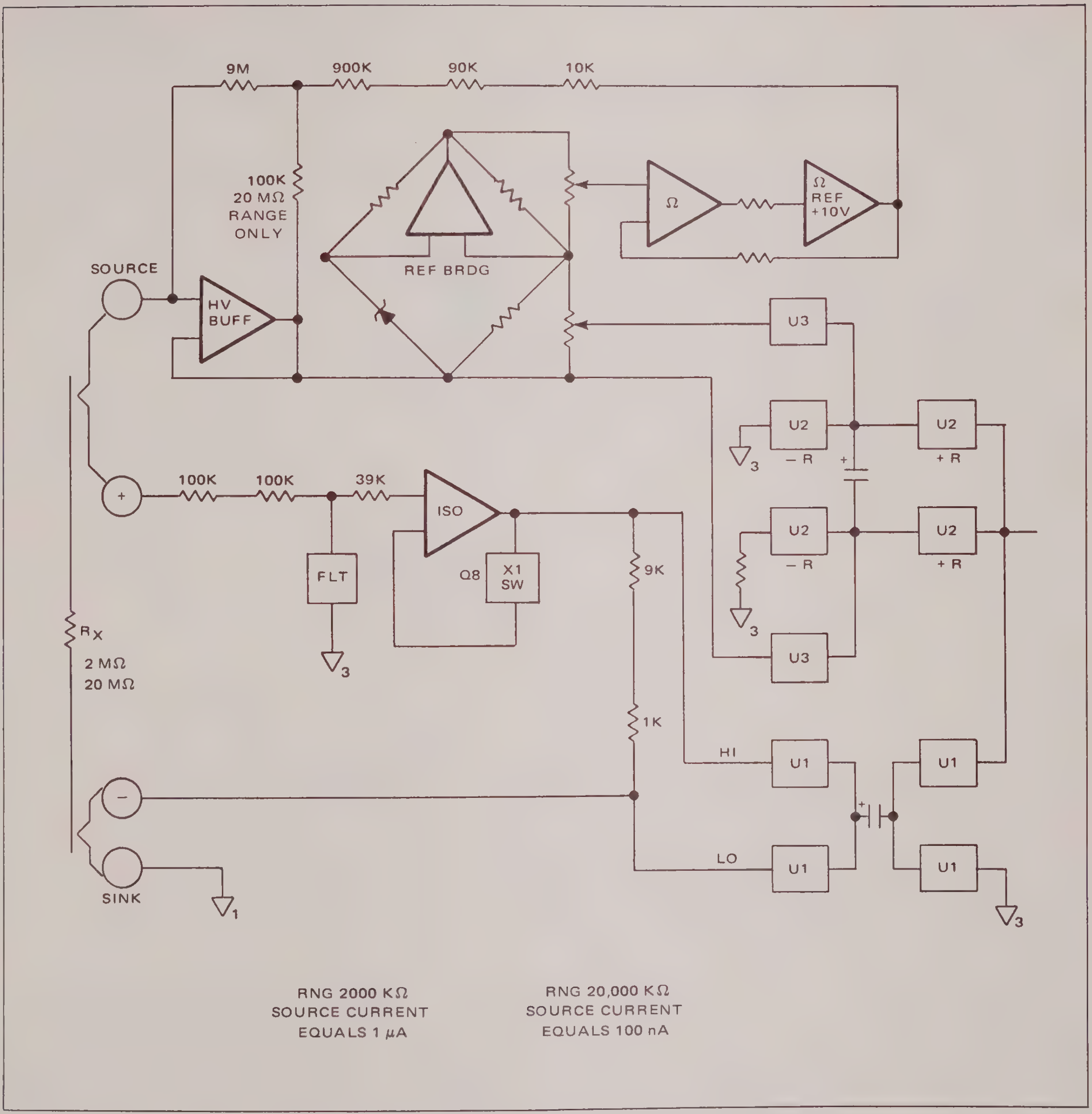
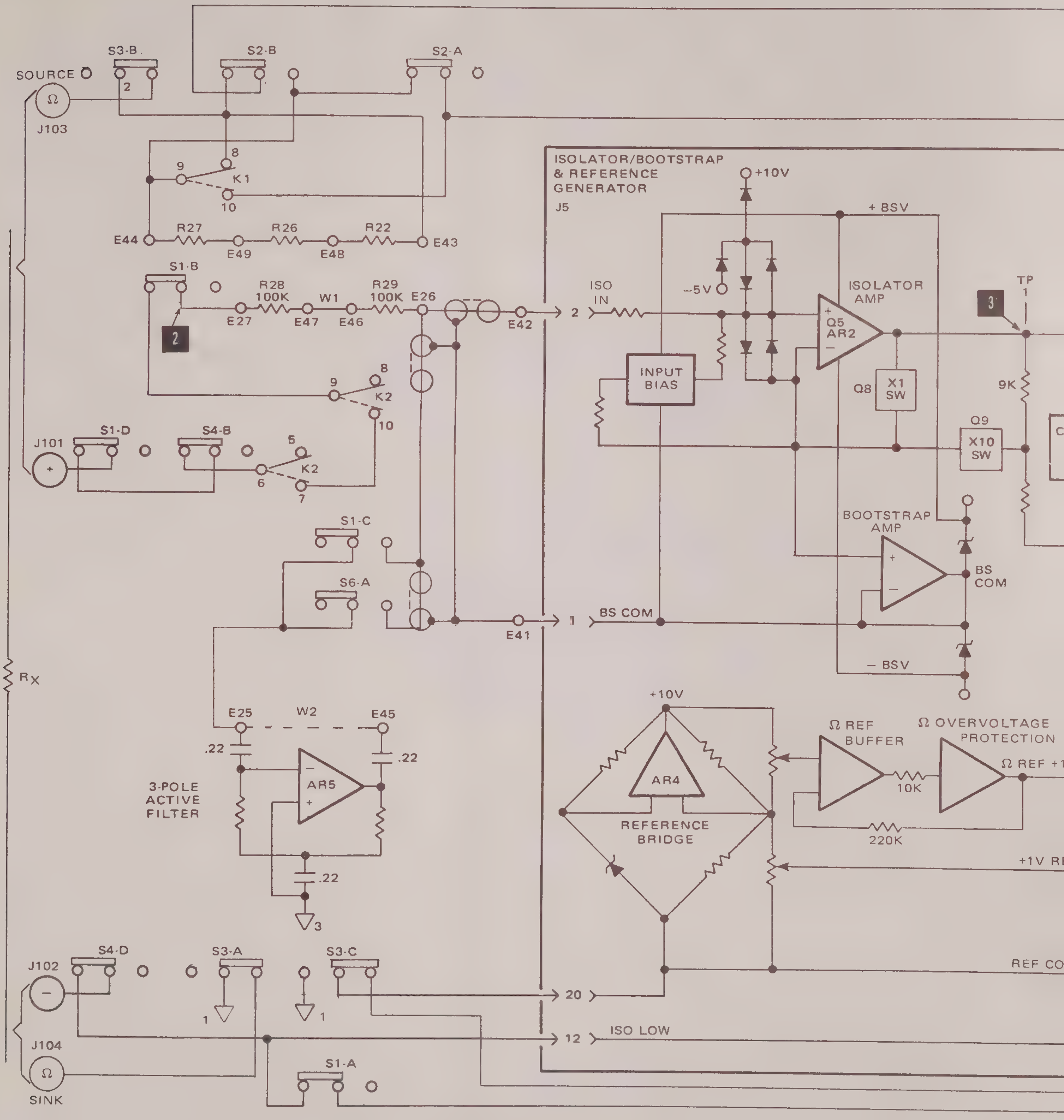

9M
900K
90K
10K
100K
20 MΩ
RANGE
ONLY
Ω
Ω
REF
+10V
REF BRDG
SOURCE
HV
BUFF
U3
U2
– R
+
U2
+ R
100K
100K
39K
ISO
U2
– R
U2
+ R
FLT
Q8
X1
SW
9K
3
3
3
U3
RX
2 MΩ
20 MΩ
1K
HI
U1
U1
+
LO
U1
U1
SINK
1
3
+
–
RNG 2000 KΩ
SOURCE CURRENT
EQUALS 1 μA
RNG 20,000 KΩ
SOURCE CURRENT
EQUALS 100 nA

Figure 5.15 - KΩ Simplified Schematic, 2000, 20,000 KΩ Ranges


SOURCE
J103
S3-B
S2-B
S2-A
K1
8
9
10
R27
R26
R22
E44
E49
E48
E43
S1-B
R28
100K
W1
R29
100K
E26
E27
E47
E46
E42
2
3
K2
J101
S1-D
S4-B
5
6
7
S1-C
S6-A
E41
RX
E25
W2
E45
.22
3-POLE
ACTIVE
FILTER
AR5
J102
S4-D
S3-A
S3-C
1
J104
SINK
S1-A
ISOLATOR/BOOTSTRAP
& REFERENCE
GENERATOR
J5
+10V
+ BSV
−5V
ISO
IN
INPUT
BIAS
ISOLATOR
AMP
Q5
AR2
Q8
X1
SW
TP
1
9K
Q9
X10
SW
BOOTSTRAP
AMP
BS
COM
BS COM
− BSV
AR4
REFERENCE
BRIDGE
Ω REF
BUFFER
10K
220K
Ω OVERVOLTAGE
PROTECTION
Ω REF +1
+1V RE
REF CO
20
12
ISO LOW

	MAIN PCB RLYS		DIGITIZER RLYS			ISO GAIN
	K1	K2	K1	K2	K3	
.2K (200Ω)		▨			▨	X10
2K		▨			▨	X1
20K		▨		▨		X1
200K		▨				X1
2,000K (2 MΩ)	▨	▨				X1
20,000K (20 MΩ)	▨	▨	▨			X1

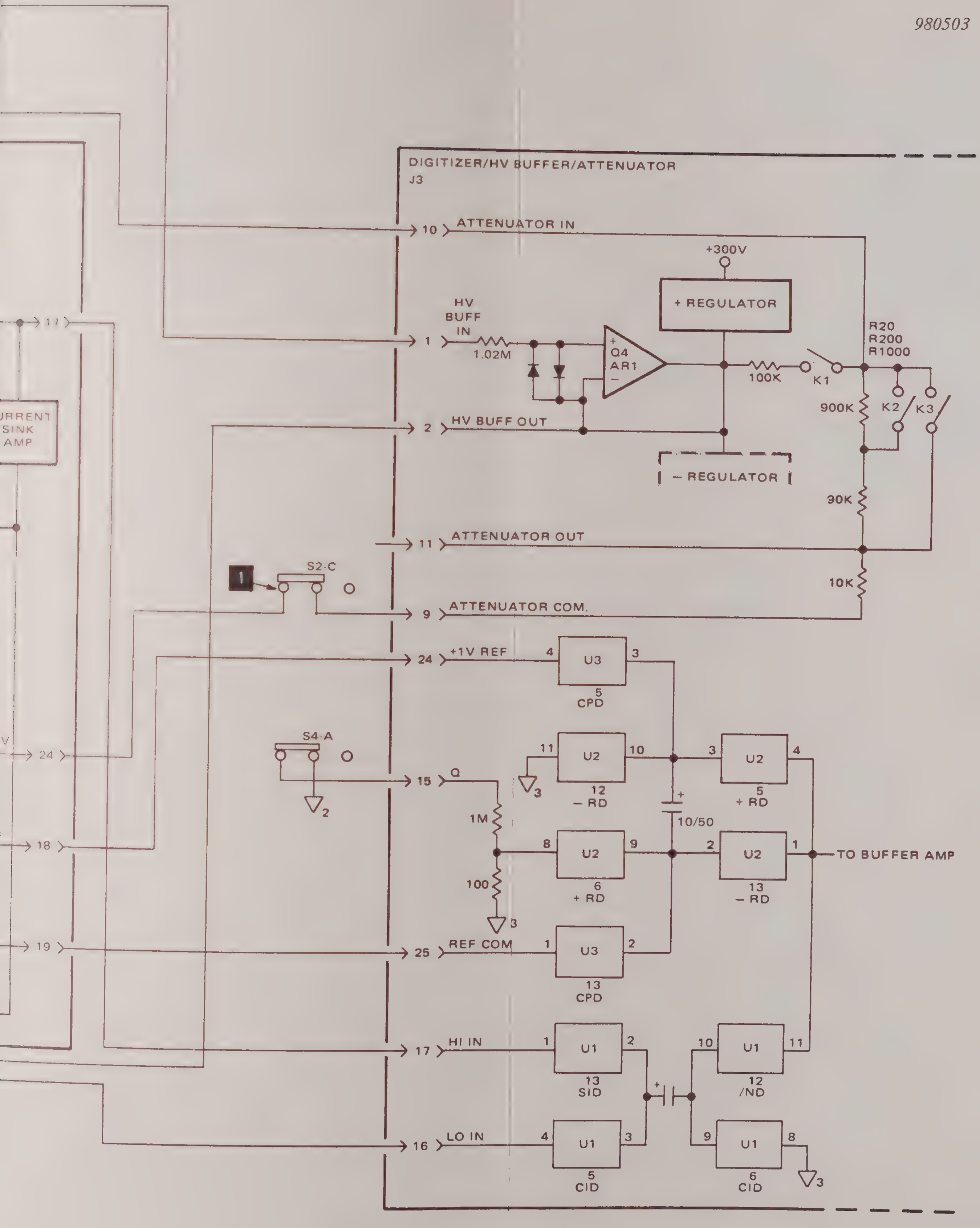

DIGITIZER/HV BUFFER/ATTENUATOR
J3
10
ATTENUATOR IN
+300V
+ REGULATOR
HV
BUFF
IN
1
1.02M
Q4
AR1
100K
K1
R20
R200
R1000
900K
K2
K3
2
HV BUFF OUT
– REGULATOR
90K
11
ATTENUATOR OUT
10K
1
S2-C
9
ATTENUATOR COM.
24
+1V REF
U3
CPD
S4-A
15
Q
U2
– RD
+ RD
1M
10/50
TO BUFFER AMP
100
25
REF COM
17
HI IN
U1
SID
/ND
16
LO IN
CID
URRENT
SINK
AMP
17
24
18
19
RGIZED

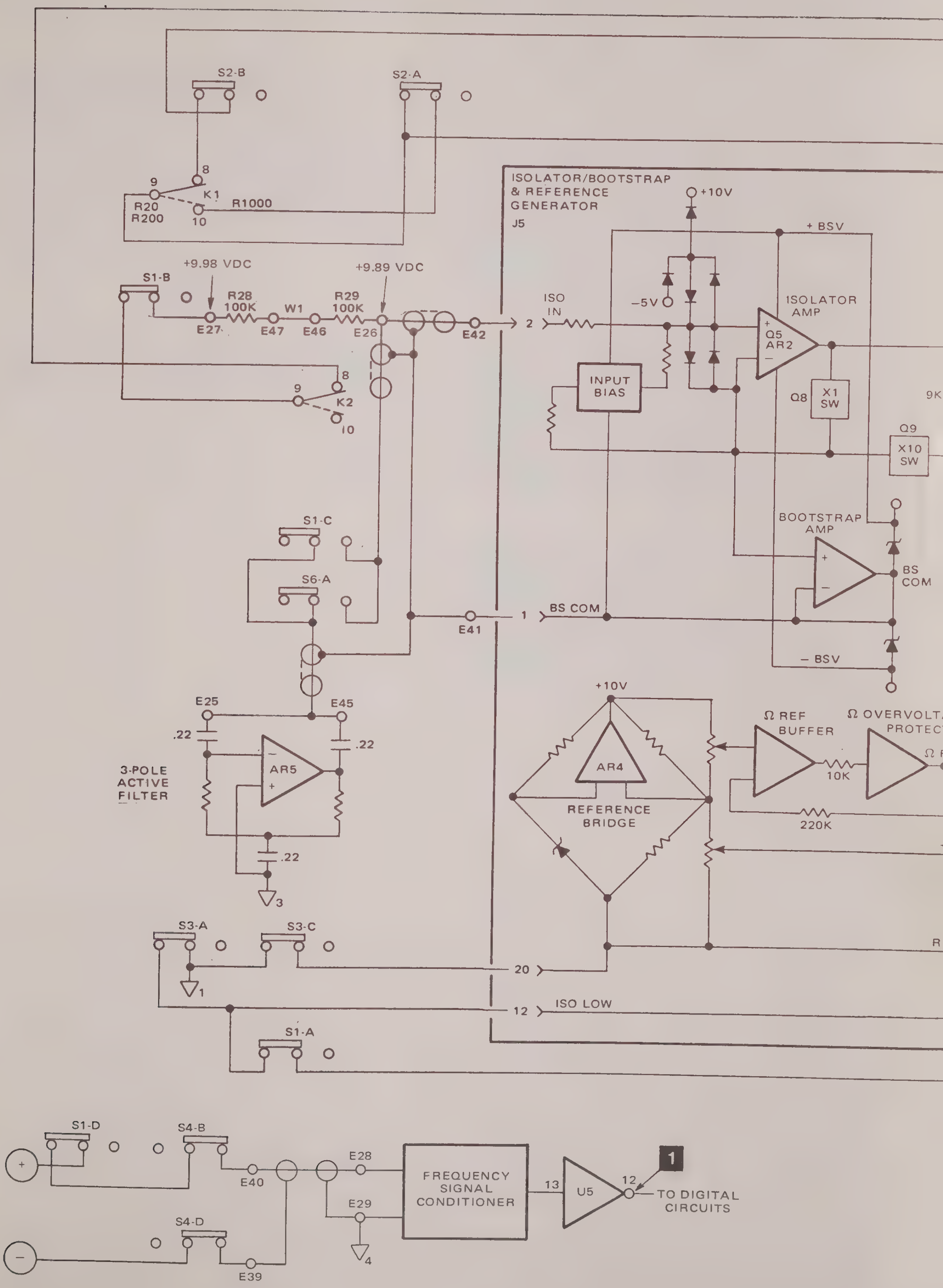
Figure 5.16 - KΩ Single Thread Diagram

Table 5.10 - kHz Unit Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: kHz Range: 2000 (manual) Input Terminals: J101 (Hi) and J102 (Lo) are connected to a frequency standard set to 200 Hz @ .5V RMS – sine variable to 20 MHz					NOTE: All analog measurements are referneced to TP4 (MECCA) NOTE: Frequency measurements (scope or counter) are referenced to TP3 (Digital Common)
	Signal Conditioned Frequency Output to Digital Measurement Circuits	U5-12	1	Figure 5.17	Output is non-sinusoidal from Digital Common (REF) to +4.25V DC, Frequency same as Input

The configuration of the analog circuits in the kHz function is:

1. The KΩ Ref voltage is connected to the attenuator common, voltage is: +10V DC
2. The Attenuator output is connected to the isolator input, voltage is: +9.98V DC
3. The Attenuator input is connected to the HV Buffer Input
4. The Isolator output voltage is: +10.02V DC


S2-B
S2-A
8
9
K1
R20
R200
10
R1000
+9.98 VDC
+9.89 VDC
S1-B
R28
100K
W1
R29
100K
E27
E47
E46
E26
E42
8
9
K2
10
ISOLATOR/BOOTSTRAP
& REFERENCE
GENERATOR
J5
+10V
+ BSV
ISO
IN
2
−5V
ISOLATOR
AMP
Q5
AR2
INPUT
BIAS
Q8
X1
SW
9K
Q9
X10
SW
BOOTSTRAP
AMP
BS
COM
S1-C
S6-A
1
BS COM
E41
− BSV
E25
E45
.22
.22
AR5
3-POLE
ACTIVE
FILTER
.22
3
+10V
Ω REF
BUFFER
Ω OVERVOLT
PROTECT
AR4
REFERENCE
BRIDGE
10K
220K
S3-A
S3-C
20
1
12
ISO LOW
S1-A
S1-D
S4-B
+
E40
E28
E29
FREQUENCY
SIGNAL
CONDITIONER
13
U5
12
1
TO DIGITAL
CIRCUITS
4
S4-D
−
E39

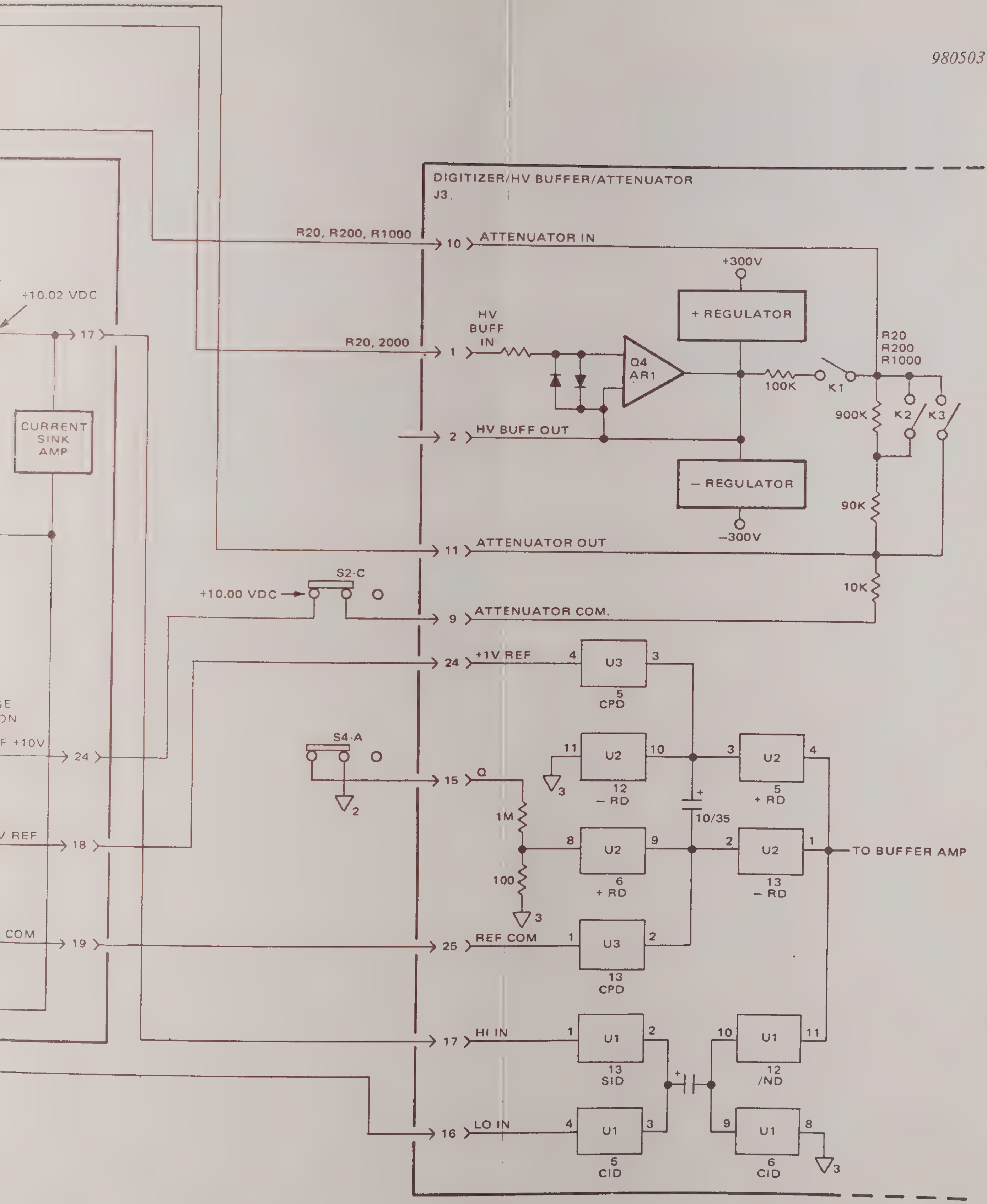

DIGITIZER/HV BUFFER/ATTENUATOR
J3.
R20, R200, R1000
10
ATTENUATOR IN
+300V
+ REGULATOR
+10.02 VDC
17
HV
BUFF
IN
R20, 2000
1
Q4
AR1
100K
K1
R20
R200
R1000
900K
K2
K3
CURRENT
SINK
AMP
2
HV BUFF OUT
− REGULATOR
90K
−300V
11
ATTENUATOR OUT
S2-C
+10.00 VDC
10K
9
ATTENUATOR COM.
24
+1V REF
4
U3
3
5
CPD
F +10V
24
S4-A
11
U2
10
3
U2
4
15
Q
3
12
− RD
5
+ RD
2
1M
10/35
V REF
18
8
U2
9
2
U2
1
TO BUFFER AMP
100
6
+ RD
13
− RD
3
COM
19
25
REF COM
1
U3
2
13
CPD
17
HI IN
1
U1
2
10
U1
11
13
SID
12
/ND
16
LO IN
4
U1
3
9
U1
8
5
CID
6
CID
3

Figure 5.17 - kHz Single Thread Diagram

5.4.8 Subassembly Performance Tests.

5.4.8.1 Subassembly performance tests are designed to isolate a malfunction to a small group of components or a single functional group of components. Once the trouble is narrowed down to a small area the technician should resort to conventional troubleshooting techniques such as checking individual components such as resistors, capacitors, semiconductors and applying heat and cold to individual components. Each of the subassembly performance tests is accompanied by performance standards for each step of the test. These performance standards are in the form of static DC voltages or waveform pictures.

5.4.8.2 In the case of the main printed circuit board, the largest and most complex of the PCBs, several performance tests have been provided. These tests are segregated because the main PCB contains a number of separate functional circuits such as the clock, isolator, range control and null detector. Separate performance tests are provided for each of the remaining smaller boards.

5.4.8.3 The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements. Troubleshooting, unlike calibration, may be done with any equipment that is accurate to 5%.

5.4.8.4 Note that the test points in the performance test tables refer to the performance standard or waveforms in the test and to the test point shown on the assembly drawings and schematic drawings in Section 6 of this manual. The presentation of assembly drawings in the troubleshooting section and again in the drawing section of the manual is redundant but it provides the necessary continuity and makes the technicians troubleshooting job easier.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal AC primary circuits when instrument is connected to the AC line.

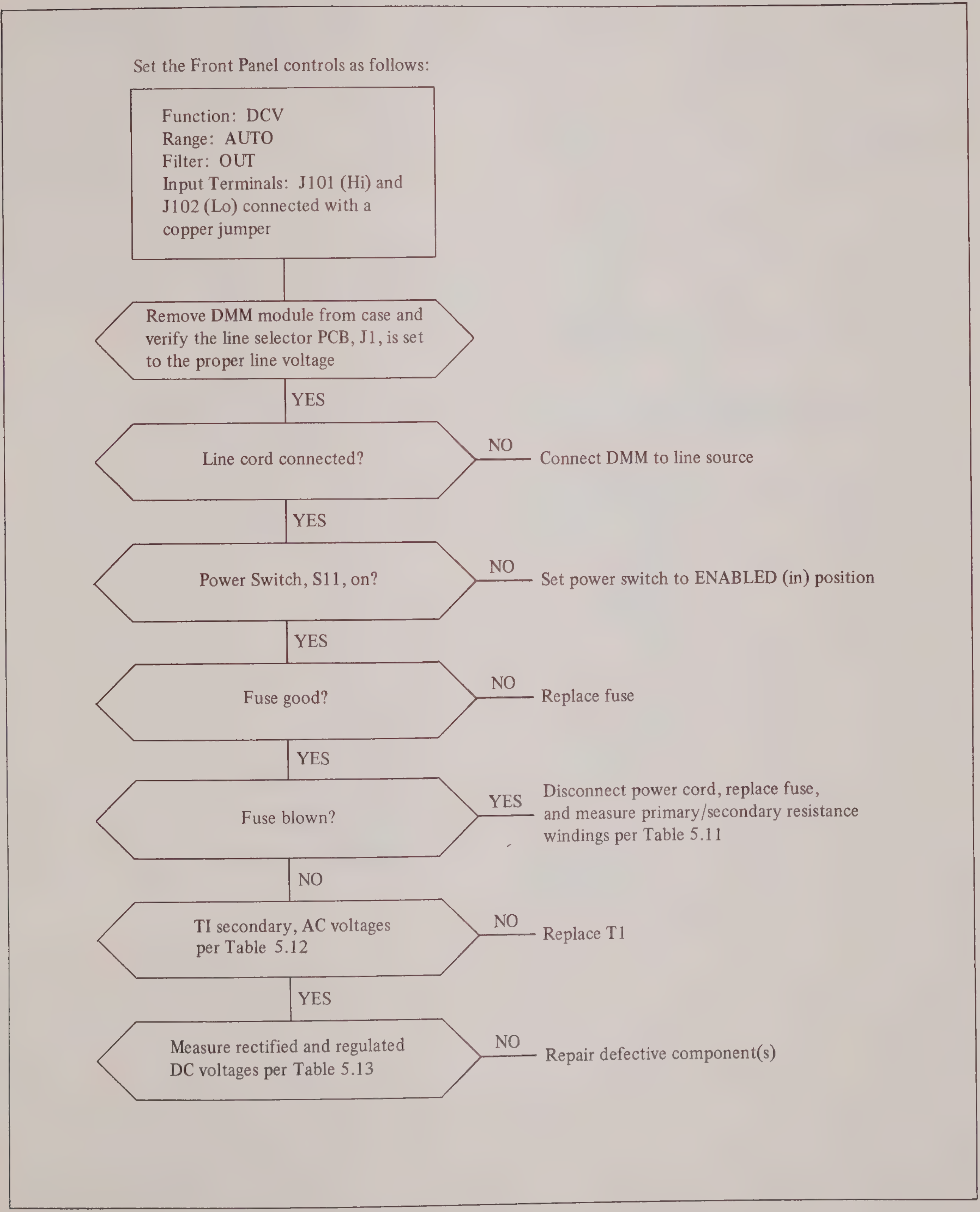

Set the Front Panel controls as follows:
Function: DCV
Range: AUTO
Filter: OUT
Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper
Remove DMM module from case and verify the line selector PCB, J1, is set to the proper line voltage
YES
Line cord connected?
NO
Connect DMM to line source
YES
Power Switch, S11, on?
NO
Set power switch to ENABLED (in) position
YES
Fuse good?
NO
Replace fuse
YES
Fuse blown?
YES
Disconnect power cord, replace fuse, and measure primary/secondary resistance windings per Table 5.11
NO
TI secondary, AC voltages per Table 5.12
NO
Replace T1
YES
Measure rectified and regulated DC voltages per Table 5.13
NO
Repair defective component(s)

Figure 5.18 - Main PCB, Power Supply Subassembly Performance Test

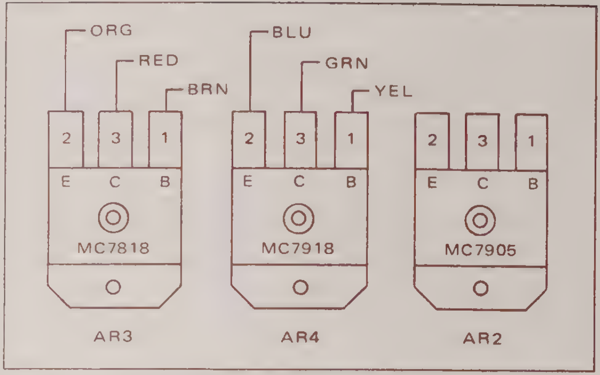


Figure 5.19 - Voltage Regulator Pin Assignments

Table 5.11 - Primary Resistance of T1

Primary Resistance of T1	
J1 Line Select Setting	J201 Line (L) to Neutral (N)
100 VAC	19Ω ± 1Ω
120 VAC	20Ω ± 1Ω
220 VAC	62Ω ± 3Ω
240 VAC	67Ω ± 3Ω

Secondary Resistances of T1		
From	To	Measurement
T1-6	T1-7	2.75Ω ± .5Ω
T1-10	T1-11	495Ω ± 10Ω
T1-12	T1-13	0.65Ω ± 0.15Ω
T1-13	T1-14	0.65Ω ± 0.15Ω
T1-12	T1-14	1.3Ω ± 0.3Ω
T1-15	T1-16	65Ω ± 1Ω

Table 5.12 - Secondary AC Voltages of T1

Secondary AC Voltages of T1		
From	To	Measurement
T1-6	T1-7	9.5 VAC ± 5%
T1-10	T1-11	205 VAC ± 5%
T1-12	T1-13	7.4 VAC ± 5%
T1-13	T1-14	7.4 VAC ± 5%
T1-12	T1-14	14.75 VAC ± 5%
T1-15	T1-16	37 VAC ± 5%

Table 5.13 - DC Voltages Referenced to Mecca (TP4)

DC Voltages Referenced to MECCA (TP4)		
Ref Desig	Measurement	P-P Ripple
E34	+255V ± 5V	6V
E35	−255V ± 5V	6V
AR2-3(C)	−7.5V ± 0.3V	700 mV
AR2-2(E)	−5.0V ± 0.25V	15 mV
AR4-3(C)	−22V ± 1V	400 mV
AR4-2(E)	−18V ± 0.5V	10 mV
AR3-1(B)	+22V ± 1V	400 mV
AR3-2(E)	+18V ± 0.5V	10 mV
CR15 (Cathode)	+10V ± 0.5V	5 mV
CR16 (Anode)	−18V ± 1V	20 mV
Q6 (Emitter)	−17V ± 1V	20 mV

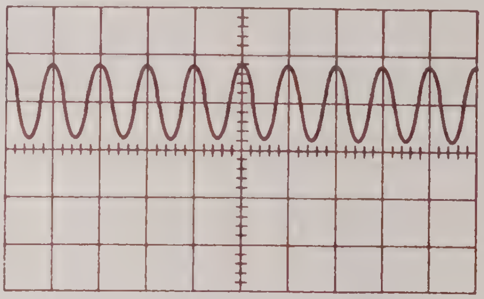
Table 5.14 - Main PCB, Oscillator/Clock & MUX Oscillator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP3 (DIG COM).
	Oscillator Output	U1-10/13	A	Figure 5.20	Waveform 1
	Clock Output	U1-2	B	Figure 5.20	Waveform 2
	MUX Osc.	U1-9	C	Figure 5.20	Waveform 3
	MUX Osc.	U1-8/5	D	Figure 5.20	Waveform 4
	MUX Osc.	U1-6/3	E	Figure 5.20	Waveform 5
	MUX Osc. Output	U1-4	F	Figure 5.20	Waveform 6

Waveforms for Table 5.14

1
(NO.)

U1-10/13
OSC OUT
1 MHz ± 1%



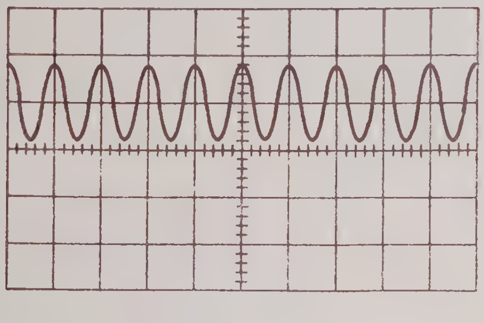
2.0V
(V/DIV)

1 μS
(S/DIV)

REF: DIGITAL COMMON
DC COUPLED

2
(NO.)

U1-2
CLOCK OUT
1 MHz ± 1%



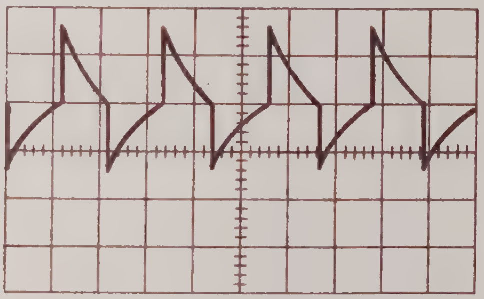
2.0V
(V/DIV)

1 μS
(S/DIV)

REF: DIGITAL COMMON
DC COUPLED

3
(NO.)

U1-9
MUX OSC
500 Hz ± 10%



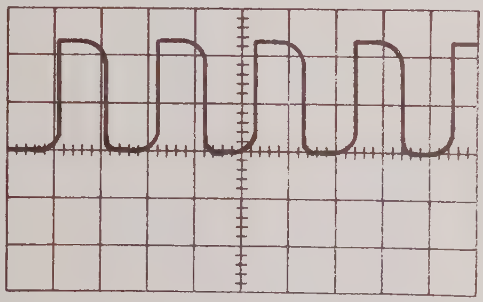
2.0V
(V/DIV)

1 mS
(S/DIV)

REF: DIGITAL COMMON
DC COUPLED

4
(NO.)

U1-8/5
MUX OSC
500 Hz ± 5%



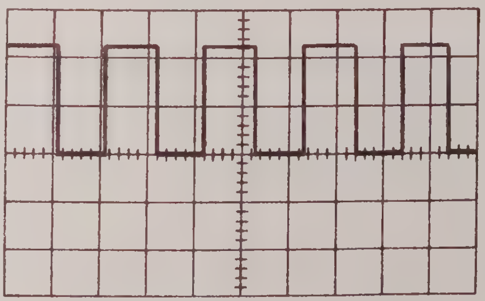
2.0V
(V/DIV)

1 mS
(S/DIV)

REF: DIGITAL COMMON
DC COUPLED

5
(NO.)

U1-6/3
MUX OSC
500 Hz ± 5%



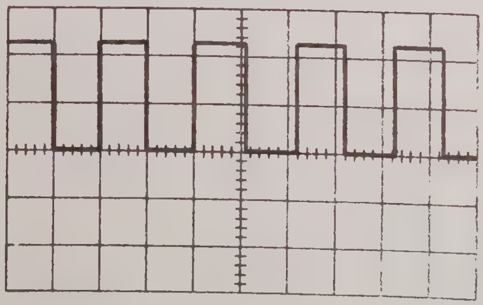
2.0V
(V/DIV)

1 mS
(S/DIV)

REF: DIGITAL COMMON
DC COUPLED

6
(NO.)

U1-4
MUX OSC OUT
500 Hz ± 5%



2.0V
(V/DIV)

1 mS
(S/DIV)

REF; DIGITAL COMMON
DC COUPLED

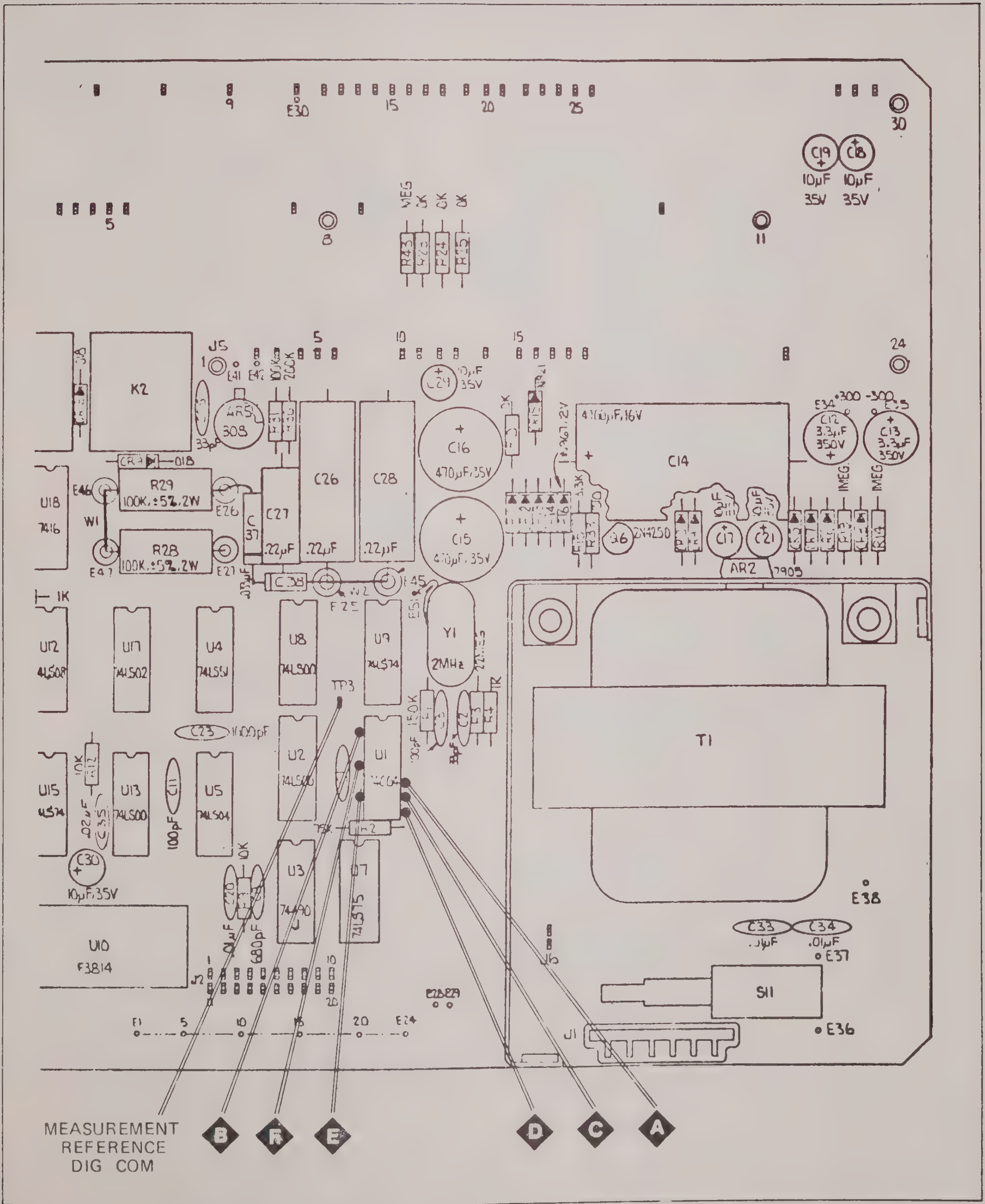

9
E30
15
20
25
30
C19
C8
10µF
35V
5
8
11
MEG
R43
R24
R25
5
10
15
24
J5
E41
E42
K2
AR5
308
33pF
CR
C16
470µF,35V
C15
470µF,35V
C14
4700µF,16V
E34
+300 -300
C12
3.3µF
350V
C13
3.3µF
350V
C24
10µF
35V
C26
C28
C27
.22µF
C37
U18
7416
E46
W1
E47
R29
100K,±5%,2W
R28
100K,±5%,2W
E26
E27
C38
W2
E45
E51
Q6
2N4250
C17
C21
AR2
7905
IMEG
R14
1K
U12
74LS08
U17
74LS02
U4
74LS51
U8
74LS00
U9
74LS74
Y1
2MHz
TP3
C23
1000pF
U15
74LS74
U13
74LS00
C11
100pF
U5
74LS04
U2
74LS00
U1
74C04
R12
10K
C35
.02µF
C30
10µF,35V
U3
7490
U7
74LS75
10K
680pF
.01µF
T1
U10
F3814
J2
1
10
20
E28
E29
E38
C33
C34
.01µF
E37
J6
S11
E36
J1
F1
5
10
15
20
E24
MEASUREMENT
REFERENCE
DIG COM
B
F
E
D
C
A

Figure 5.20 - Main PCB, Oscillator/Clock & MUX Oscillator Test Point Locations

Table 5.15 - Main PCB, Range/Function & Relay Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper	ROM Inputs/Outputs	U21	1	Figure 5.24	NOTE: All measurements are referenced to TP3 (DIG COM)
Range: 2	ROM Inputs/Outputs	U21			
Range: 20	ROM Inputs/Outputs	U21			
Range: 200	ROM Inputs/Outputs	U21			
Range: 1200	ROM Inputs/Outputs	U21			
Function: ACV	ROM Inputs/Outputs	U21	1	Figure 5.24	
Range: 200	ROM Inputs/Outputs	U21			
Range: 20	ROM Inputs/Outputs	U21			
Range: 2	ROM Inputs/Outputs	U21			
Function: KΩ	ROM Inputs/Outputs	U21	1	Figure 5.24	
Range: .2	ROM Inputs/Outputs	U21			
Range: 2	ROM Inputs/Outputs	U21			
Range: 20	ROM Inputs/Outputs	U21			
Range: 200	ROM Inputs/Outputs	U21			
Range: 2000	ROM Inputs/Outputs	U21			
Range: 20,000	ROM Inputs/Outputs	U21			
Function: kHz	ROM Inputs/Outputs	U21	1	Figure 5.24	
Range: 2000	ROM Inputs/Outputs	U21			

		MAIN PCB		DIGITIZER PCB			AC CONV. PCB			ISOLATOR GAIN	
FUNCTION	RANGE	K1	K2	K1	K2	K3	K1	K2	K3	X1	X10
DCV	.2		▨								▨
	2		▨							▨	
	20				▨					▨	
	200									▨	
	1000	▨								▨	
ACV	2									▨	
	20				▨		▨			▨	
	200							▨		▨	
	1000								▨	▨	
KΩ	.2		▨			▨					▨
	2		▨			▨				▨	
	20		▨		▨					▨	
	200		▨							▨	
	2000	▨	▨							▨	
	20,000	▨	▨	▨						▨	
kHz	2000										
	20,000			▨							

▨

Figure 5.21 - Range Relay Status Chart

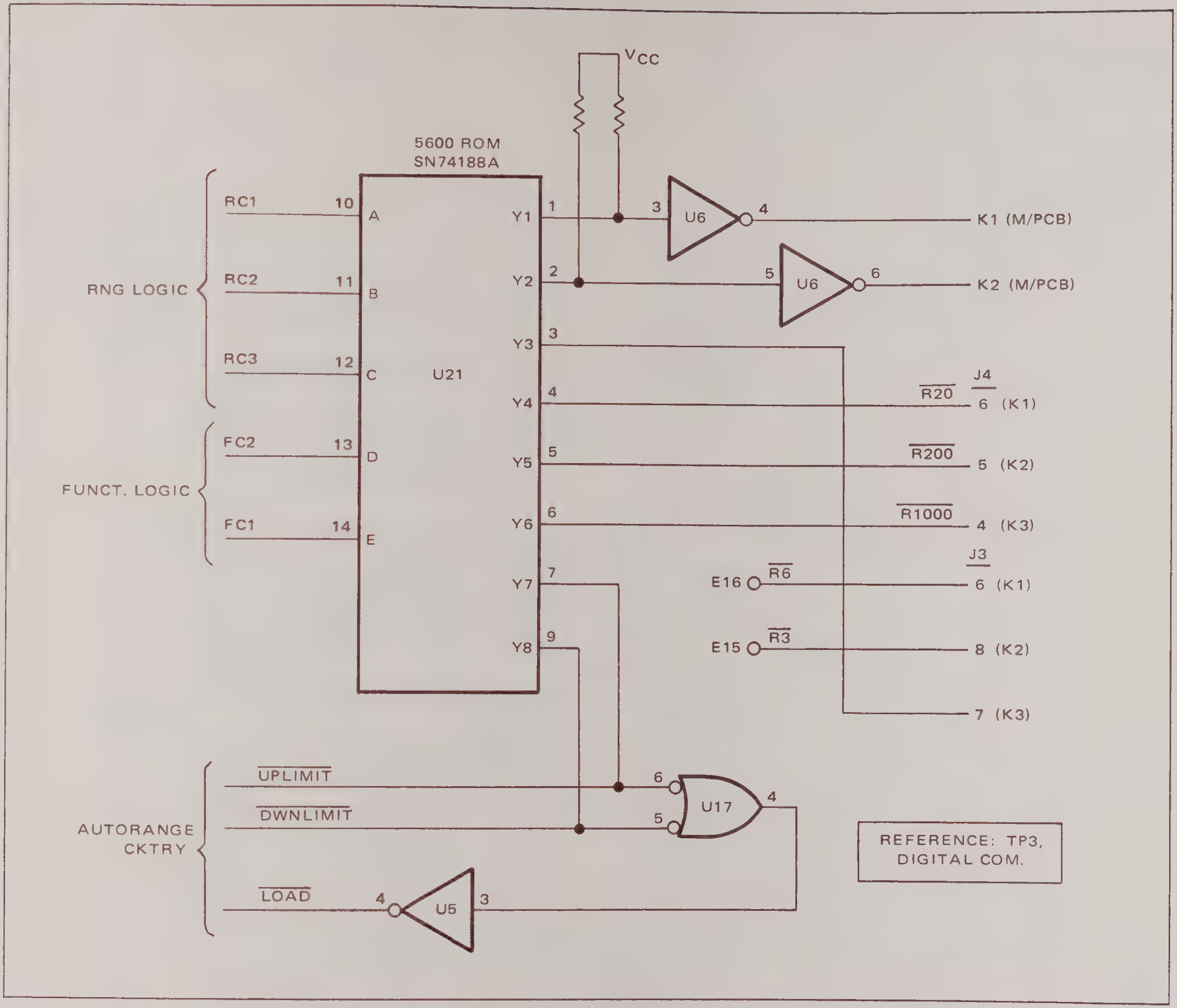

VCC
5600 ROM
SN74188A
U21
RNG LOGIC
RC1
RC2
RC3
FUNCT. LOGIC
FC2
FC1
10
11
12
13
14
A
B
C
D
E
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
1
2
3
4
5
6
7
9
U6
K1 (M/PCB)
K2 (M/PCB)
J4
R20
6 (K1)
R200
5 (K2)
R1000
4 (K3)
J3
E16
R6
6 (K1)
E15
R3
8 (K2)
7 (K3)
AUTORANGE CKTRY
UPLIMIT
DWNLIMIT
LOAD
U17
U5
REFERENCE: TP3, DIGITAL COM.

Figure 5.22 - Range & Function ROM Simplified Schematic

STATEMENTS

1. Inputs A(RC1), B(RC2), and C(RC3) are from the UP/DOWN range counter to code range information. High levels (3.6V, REF: DIG COM) decode range.
2. Inputs D(FC2) and E(FC1) are from function logic/switches to code function information. Low levels (0.15V, REF: DIG COM) decode function.
3. Outputs Y1 and Y2 are inverted to drive K1 and K2 on the main PCB for signal distribution for DCV and KΩ ranges. High outputs enable relays.
4. Outputs Y3, E16 ($\overline{\text{R6}}$, Display Decimal Code), and E15 ($\overline{\text{R3}}$, Display Decimal Code) drive K3, K1, and K2 respectively on the digitizer PCB to configure the HV buffer and/or attenuator for DCV and KΩ ranges. Low outputs enable relays.
5. Outputs Y4, Y5, and Y6 code range attenuation for the AC converter relays. Low outputs enable relays.
6. Outputs Y7 and Y8 decode $\overline{\text{UP LIMIT}}$ and $\overline{\text{DOWN LIMIT}}$ information for autoranging processes. Low outputs are range limits. If both outputs are low (power-up or illegal range), the up/down counter, U20, is set from range code 6 (hard-wired input code) when the $\overline{\text{load}}$ input goes low to protect signal input circuitry.

ROM IN

ROM OUT

DCV

TYPICAL FOR ALL INPUTS	U21 PIN		.2	2	20	200	1200
RC1	A	10	L	▓	L	▓	L
RC2	B	11	▓	▓	L	L	▓
RC3	C	12	L	L	▓	▓	▓
FC2	D	13	H	H	H	H	H
FC1	E	14	H	H	H	H	H

TRUE STATE		LOGIC LEVEL
▓	= HIGH =	H
░	= LOW =	L

TYPICAL FOR ALL TABLES

U21 PIN		.2	2	20	200	1200	TYPICAL FOR ALL OUTPUTS
Y1	1	L	L	L	L	▓	K1 — M/PCB
Y2	2	▓	▓	L	L	L	K2 — M/PCB
Y3	3	H	H	H	H	H	K3 — DIG
Y4	4	H	H	H	H	H	K1 — AC
Y5	5	H	H	H	H	H	K2 — AC
Y6	6	H	H	H	H	H	K3 — AC
Y7	7	H	H	H	H	░	$\overline{\text{UPLIMIT}}$
Y8	9	░	H	H	H	H	$\overline{\text{DWNLIMIT}}$
E16		H	H	H	H	H	K1 — DIG
E15		H	H	░	H	H	K2 — DIG

a

ACV

U21 PIN			2	20	200	1000
A	10		▓	L	▓	L
B	11	*	▓	L	L	▓
C	12		L	▓	▓	▓
D	13		H	H	H	H
E	14		░	░	░	░

U21 PIN			2	20	200	1000
Y1	1		L	L	L	L
Y2	2	*	L	L	L	L
Y3	3		H	H	H	H
Y4	4		H	░	H	H
Y5	5		H	H	░	H
Y6	6		H	H	H	░
Y7	7		H	H	H	░
Y8	9		░	H	H	H
E16			H	H	H	H
E15			H	░	H	H

b

KΩ

U21 PIN		.2	2	20	200	2,000	20,000
A	10	L	▓	L	▓	L	▓
B	11	▓	▓	L	L	▓	▓
C	12	L	L	▓	▓	▓	▓
D	13	░	░	░	░	░	░
E	14	H	H	H	H	H	H

U21 PIN		.2	2	20	200	2,000	20,000
Y1	1	L	L	L	L	▓	▓
Y2	2	▓	▓	▓	▓	▓	▓
Y3	3	░	░	H	H	H	H
Y4	4	H	H	H	H	H	H
Y5	5	H	H	H	H	H	H
Y6	6	H	H	H	H	H	H
Y7	7	H	H	H	H	H	░
Y8	9	░	H	H	H	H	H
E16		H	H	H	H	H	░
E15		H	H	░	H	H	H

c

kHz

U21 PIN			2,000	20,000
A	10			▓
B	11	*	▓	▓
C	12		▓	▓
D	13		░	░
E	14		░	░

U21 PIN			2,000	20,000
Y1	1			
Y2	2	*		
Y3	3			
Y4	4			
Y5	5			
Y6	6			
Y7	7			░
Y8	9		░	
E16				░
E15				

d

* THESE RANGES DO NOT EXIST

Figure 5.23 - Relay Logic Level Performance Standard

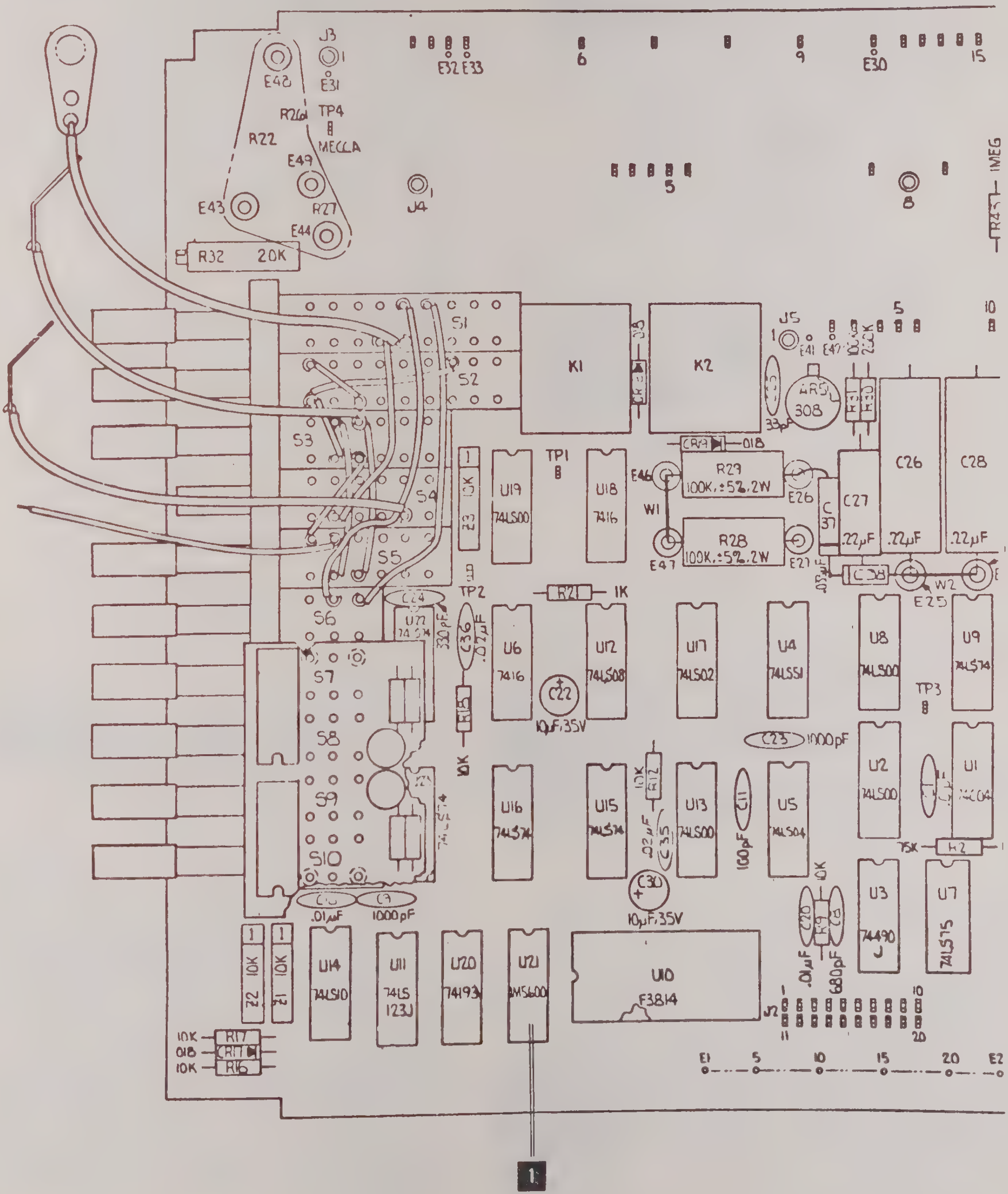

J3
E42
E31
E32 E33
6
9
E30
15
R26
TP4
MECCA
R22
E49
E43
R27
J4
5
8
IMEG
R43
E44
R32 20K
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
K1
K2
CR3
J5
E41
E47
ARS1
308
33pF
10
CR19
018
TP1
U19
74LS00
U18
7416
E46
R29
100K,±5%,2W
E26
C37
C27
.22μF
C26
.22μF
C28
.22μF
W1
E47
R28
100K,±5%,2W
E27
C38
W2
E25
10K
R23
TP2
R21
1K
C24
U22
74LS74
330pF
C36
.02μF
U6
7416
U12
74LS08
U17
74LS02
U4
74LS51
U8
74LS00
U9
74LS74
TP3
R15
C22
10μF,35V
C23
1000pF
10K
R12
U16
74LS74
U15
74LS74
C35
.02μF
U13
74LS00
C11
100pF
U5
74LS04
U2
74LS00
U1
74C04
75K
R2
C30
10μF,35V
C10
.01μF
C9
1000pF
U3
74490
U7
74LS75
C20
.01μF
R9
C21
680pF
U14
74LS10
U11
74LS
123J
U20
74193
U21
MM5600
U10
F3814
R22 10K
R21 10K
J2
1
10
11
20
10K R17
018 CR17
10K R16
E1
5
10
15
20
E2
1

Figure 5.24 - Main PCB, Range/Function & Relay Logic Test Point Locations

Table 5.16 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP3 (DIG COM) NOTE: External trigger oscilloscope at TP1 (SID)
	Counter Output Q_{e1}	U10-18/U13-5	G	Figure 5.25	Waveform 1
	Counter Output Q_{e2}	U10-16/U13-4	H	Figure 5.25	Waveform 2
	$\overline{\text{Signal Integrate}}$	U13-6	I	Figure 5.25	Waveform 3
	$\overline{\text{Reset}}$	U13-11	J	Figure 5.25	Waveform 4
Remove jumper and connect to a DC standard set at +.100000V (half-scale)	$\overline{\text{Null Detect}}$	TP2	K	Figure 5.25	Waveform 5_1
Reverse Signal Polarity	$\overline{\text{Null Detect}}$	TP2	K	Figure 5.25	Waveform 5_2
Reverse Signal Polarity	+ND F/F Output	U14-1	L	Figure 5.25	Waveform 6
	–ND F/F Output	U14-2	M	Figure 5.25	Waveform 7
	Internal Reset	U14-12	N	Figure 5.25	Waveform 8
	Signal Integrate	U13-3	O	Figure 5.25	Waveform 9
	Reference Integrate Enable	U17-13	P	Figure 5.25	Waveform 10
	– Reference Switch Drive	U18-6	Q	Figure 5.25	Waveform 11
	Freq/10 Switch Output	U4-6	R	Figure 5.25	Waveform 12
	Prescale Counter "A" Output	U3-3	S	Figure 5.25	Waveform 13
	Prescale Counter "D" Output	U3-7	T	Figure 5.25	Waveform 14
	Counter Control F/F "D" Input	U9-2	U	Figure 5.25	Waveform 15

Table 5.16 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Counter Control F/F Clock Input	U9-3	V	Figure 5.25	Waveform 16
	Counter Control F/F Q Output	U9-6	W	Figure 5.25	Waveform 17
	One-Shot "A" Q Output	U11-4	X	Figure 5.25	Waveform 18
	One-Shot "B" Q Output	U11-12	Y	Figure 5.25	Waveform 19
Remove DC standard voltage input					
Function: kHz Range: 2000 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected to a copper jumper	Sig Cond Bias Voltage	R8	2	Figure 5.25	NOTE: External trigger for frequency (kHz) scope measurements is at U13-6 (SIG INT) +3.3 to +3.4V DC
	Q1 Drain Bias Voltage	CR20 (Cathode)	3	Figure 5.25	+2.7 to +2.8V DC
	Q1 Source Bias Voltage	R7	4	Figure 5.25	+0.48 to +0.55V DC
	Sig Cond Divider Bias Voltage	R7	5	Figure 5.25	−1.40 to −1.50V DC
	Q2 Emitter Bias Voltage	R42	6	Figure 5.25	+3.5 to +3.6V DC
	Q2 Collector Bias Voltage	R34	7	Figure 5.25	+1.6 to +1.7V DC
	Q3 Collector Bias Voltage	R35	8	Figure 5.25	+3.8 to +3.9V DC
	Q4 Collector Bias Voltage	R39	9	Figure 5.25	+4.2 to +4.3V DC
	Q3/Q4 Emitter Bias Voltage	R38	10	Figure 5.25	+1.4 to +1.5V DC
	Q4 Base Bias Voltage	R36	11	Figure 5.25	+1.9 to +2.0V DC
	Q5 Collector/DC Output Voltage	R40	12	Figure 5.25	+2.5 to +2.6V DC

Table 5.16 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Remove jumper. Connect DMM inputs to frequency (function) generator set to 1V RMS output @ 1 MHz	Sig Cond Output	U5-12	Z	Figure 5.25	Waveform 20
	Clock Gate Enable	U2-12	a	Figure 5.25	Waveform 21
	Clock Gate Output	U2-11	b	Figure 5.25	Waveform 22
	Prescale Counter "D" Output	U3-7/U4-1	T	Figure 5.25	Waveform 23
	Sample Gate Enable	U4-8	c	Figure 5.25	Waveform 24
	Sample Gate Output	U2-6	d	Figure 5.25	Waveform 25
	Freq/10 Switch Output	U4-6	R	Figure 5.25	Waveform 26
	Prescale Counter "A" Output	U3-3	S	Figure 5.25	Waveform 27
	Counter Control F/F "D" Input	U9-2	U	Figure 5.25	Waveform 28
	Counter Control F/F Clock Input	U9-3	V	Figure 5.25	Waveform 29
	LSD Counter Gate Output	U2-8	e	Figure 5.25	Waveform 30
	LSD Counter Output	U3-9	f	Figure 5.25	Waveform 31
	Counter Control F/F "Q" Output	U9-6	W	Figure 5.25	Waveform 32
	Counter Gate Enable	U12-11	g	Figure 5.25	Waveform 33
	One-Shot "A" Q Output	U11-4	X	Figure 5.25	Waveform 34
	One-Shot "B" Q Output	U11-12	Y	Figure 5.25	Waveform 35
	Q_{e1} Counter Output	U10-18	G	Figure 5.25	Waveform 36
	Q_{e2} Counter Output	U10-16	H	Figure 5.25	Waveform 37

Table 5.16 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test continued

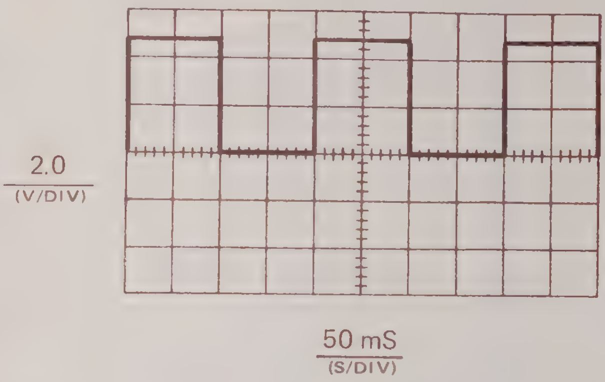
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Signal Integrate Output (EXT Trig)	U13-6	I	Figure 5.25	Waveform 38
	ND (Null Detect) Output	U6-1/TP2	K	Figure 5.25	Waveform 39
	+ ND F/F Output	U14-1	L	Figure 5.25	Waveform 40
	– ND F/F Output	U14-2	M	Figure 5.25	Waveform 41
	Reset	U13-11	J	Figure 5.25	Waveform 42
	Internal Reset	U14-12	N	Figure 5.25	Waveform 43
	Reference Integrate Enable	U17-13	P	Figure 5.25	Waveform 44
	– Reference Switch Drive	U18-6	Q	Figure 5.25	Waveform 45
Range: 20,000 (manual)	Clock Gate Enable	U12-12	a	Figure 5.25	Waveform 46
	Clock Gate Output	U2-11	b	Figure 5.25	Waveform 47
	Prescale Counter "D" Output	U3-7/U4-1	T	Figure 5.25	Waveform 48
	Sample Gate Enable	U4-8	c	Figure 5.25	Waveform 49
	Sample Gate Output	U2-6	d	Figure 5.25	Waveform 50
	Freq/10 Switch Output	U4-6	R	Figure 5.25	Waveform 51
	Prescale Counter "A" Output	U3-3	S	Figure 5.25	Waveform 52
	Counter Control F/F "D" Input	U9-2	U	Figure 5.25	Waveform 53
	Counter Control F/F Clock Input	U9-3	V	Figure 5.25	Waveform 54
	LSD Counter Gate Output	U2-8	e	Figure 5.25	Waveform 55

Table 5.16 - Main PCB, Counter & Timing/Control Logic Subassembly Performance Test continued

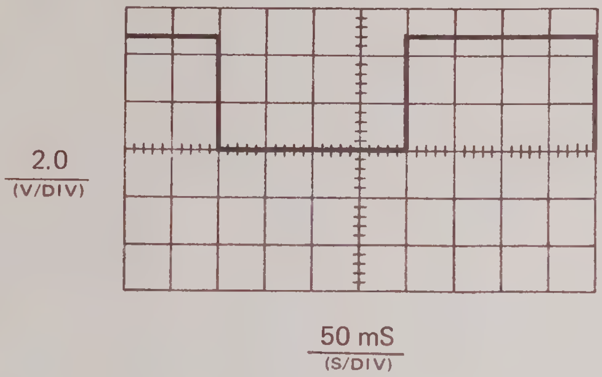
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	LSD Counter Output	U3-9	f	Figure 5.25	Waveform 56
	Counter Control F/F "Q" Output	U9-6	W	Figure 5.25	Waveform 57
	Counter Gate Enable	U12-11	g	Figure 5.25	Waveform 58
	One-Shot "A" $\bar{Q}$ Output	U11-4	X	Figure 5.25	Waveform 59
	One-Shot "B" $\bar{Q}$ Output	U11-12	Y	Figure 5.25	Waveform 60
	Q_{e1} Counter Output	U10-18	G	Figure 5.25	Waveform 61
	Q_{e2} Counter Output	U10-16	H	Figure 5.25	Waveform 62
	$\overline{\text{Signal Integrate}}$ Output (EXT Trig)	U13-6	I	Figure 5.25	Waveform 63
	$\overline{\text{ND}}$ $\overline{\text{(Null Detector)}}$ Output	U6-1/TP2	K	Figure 5.25	Waveform 64
	+ ND F/F Output	U14-1	L	Figure 5.25	Waveform 65
	– ND F/F Output	U14-2	M	Figure 5.25	Waveform 66
	$\overline{\text{Reset}}$	U13-11	J	Figure 5.25	Waveform 67
	Internal Reset	U14-12	N	Figure 5.25	Waveform 68
	Reference Integrate Enable	U17-13	P	Figure 5.25	Waveform 69
	– Reference Switch Drive	U18-6	Q	Figure 5.25	Waveform 70

Waveforms for Table 5.16

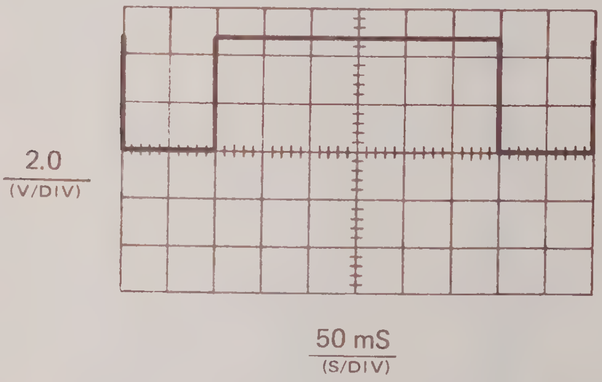
1 (NO.) Q_{e1} U10-18



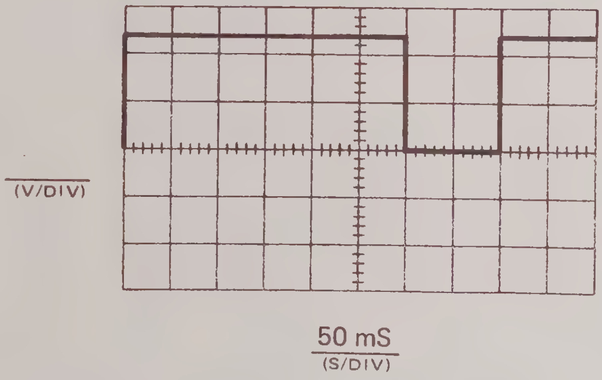
2 (NO.) Q_{e2} U10-16



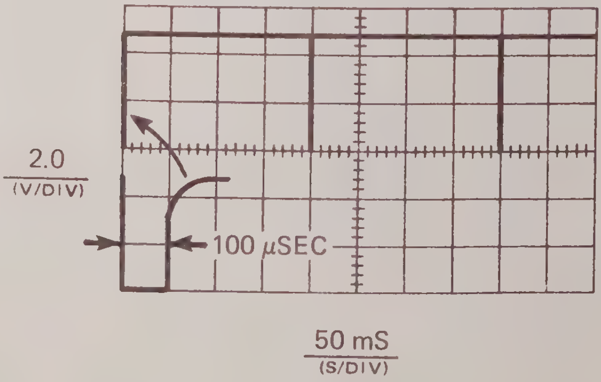
3 (NO.) $\overline{\text{SIGNAL INTEGRATE}}$ U13-6



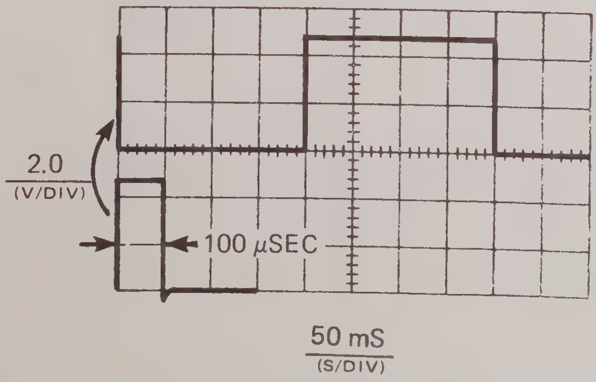
4 (NO.) $\overline{\text{RESET}}$ U13-11



5_1 (NO.) $\overline{\text{NULL DETECT}}$ (+ POL) TP2



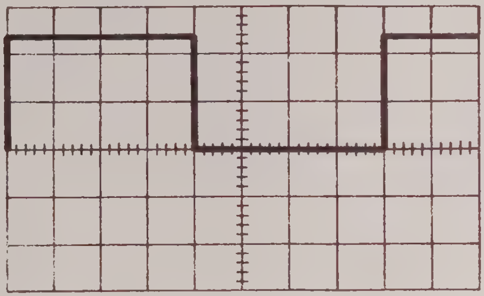
5_2 (NO.) NULL DETECT (– POL) TP2



Waveforms for Table 5.16 continued

6
(NO.)

+ ND F/F OUTPUT
U14-1

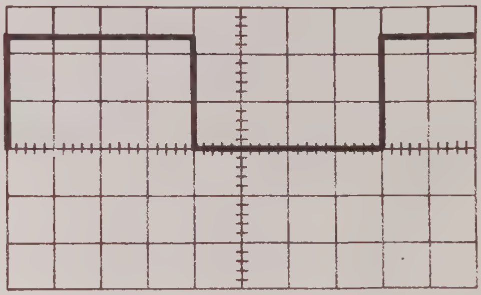


2.0
(V/DIV)

50 mS
(S/DIV)

7
(NO.)

– ND F/F OUTPUT
U14-2

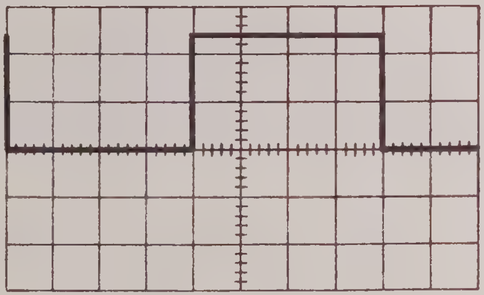


2.0
(V/DIV)

50 mS
(S/DIV)

8
(NO.)

INTERNAL RESET
U14-12

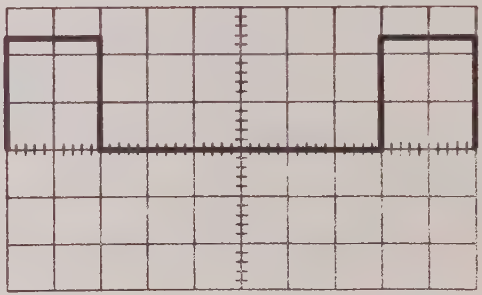


2.0
(V/DIV)

50 mS
(S/DIV)

9
(NO.)

SIGNAL INTEGRATE
U13-3

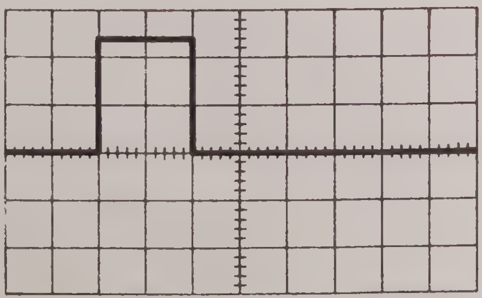


2.0
(V/DIV)

50 mS
(S/DIV)

10
(NO.)

REFERENCE INTEGRATE ENABLE
U17-13

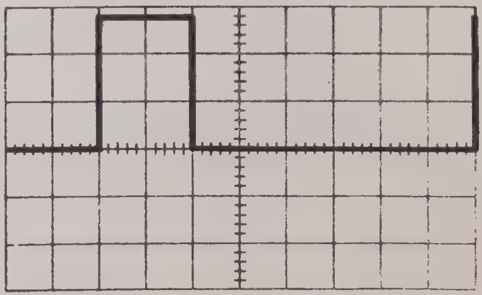


2.0
(V/DIV)

50 mS
(S/DIV)

11
(NO.)

– REFERENCE SWITCH DRIVE
U18-6



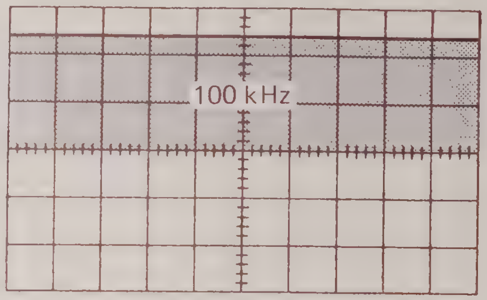
5.0
(V/DIV)

50 mS
(S/DIV)

Waveforms for Table 5.16 continued

12
(NO.)

FREQ/10 SWITCH OUTPUT
U4-6

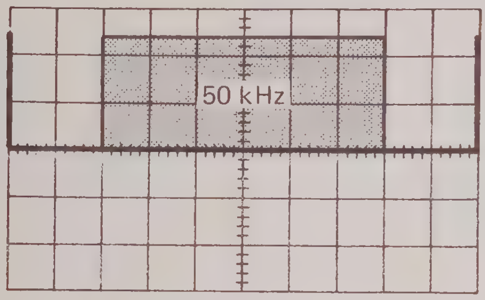


2.0
(V/DIV)

50 mS
(S/DIV)

13
(NO.)

PRESCALE COUNTER "A" OUTPUT
U3-3

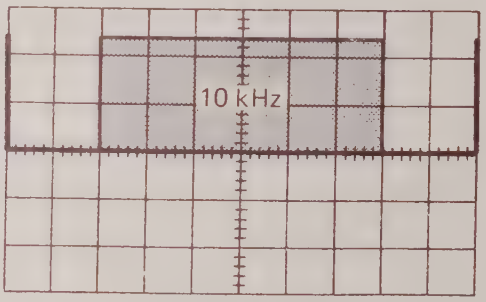


2.0
(V/DIV)

50 mS
(S/DIV)

14
(NO.)

PRESCALE COUNTER "D" OUTPUT
U3-7

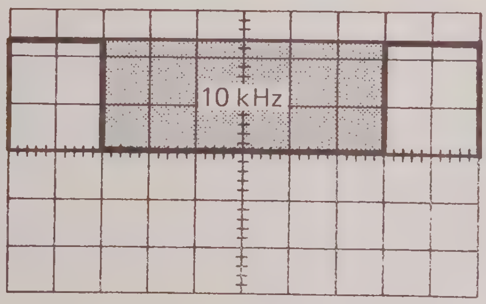


2.0
(V/DIV)

50 mS
(S/DIV)

15
(NO.)

COUNTER CONTROL F/F "D" INPUT
U9-2

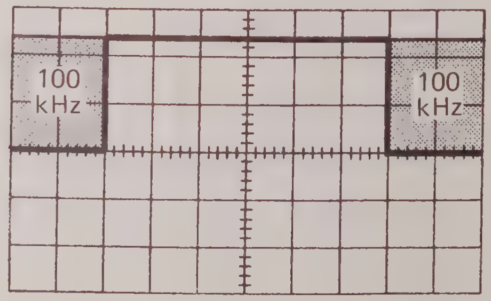


(V/DIV)

50 mS
(S/DIV)

16
(NO.)

COUNTER CONTROL F/F CLOCK INPUT
U9-3

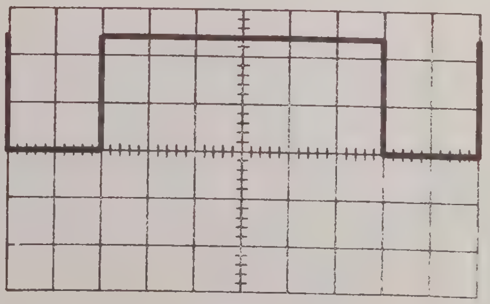


2.0
(V/DIV)

50 mS
(S/DIV)

17
(NO.)

COUNTER CONTROL F/F $\overline{Q}$ OUTPUT
U9-6

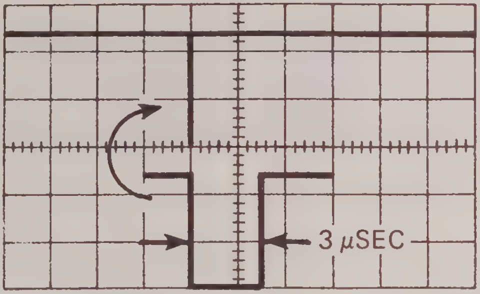


2.0
(V/DIV)

50 mS
(S/DIV)

18
(NO.)

ONE-SHOT "A" $\overline{Q}$ OUTPUT
U11-4

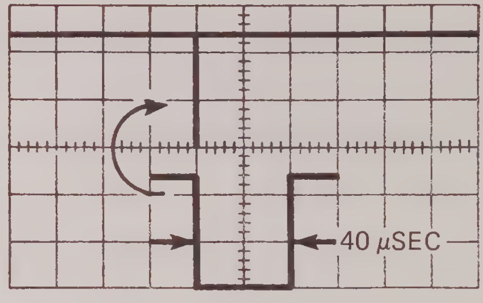


2.0
(V/DIV)

50 mS
(S/DIV)

19
(NO.)

ONE-SHOT "B" $\overline{Q}$ OUTPUT
U11-12

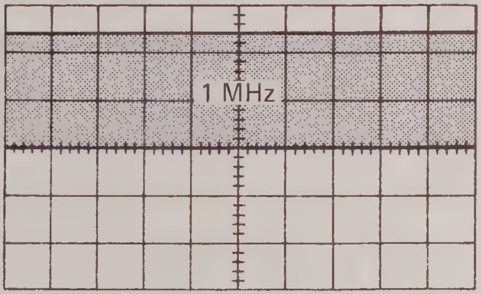


2.0
(V/DIV)

50 mS
(S/DIV)

20
(NO.)

SIGNAL CONDITIONER OUTPUT
U5-12

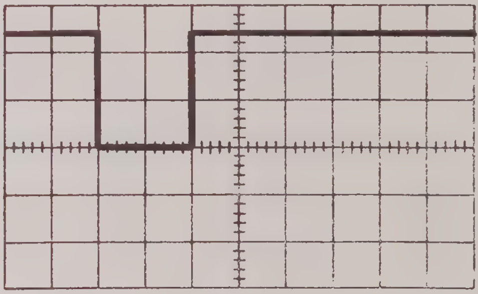


2.0
(V/DIV)

50 mS
(S/DIV)

21
(NO.)

CLOCK GATE ENABLE
U2-12

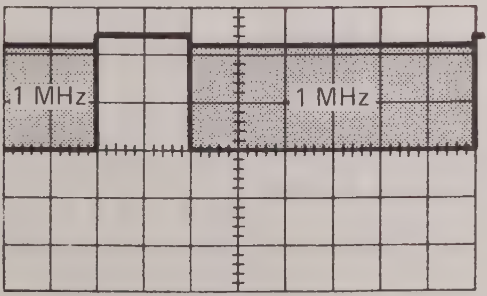


2.0
(V/DIV)

50 mS
(S/DIV)

22
(NO.)

CLOCK GATE OUTPUT
U2-11

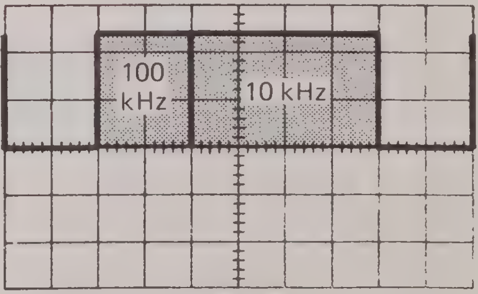


2.0
(V/DIV)

50 mS
(S/DIV)

23
(NO.)

PRESCALE COUNTER "D" OUTPUT
U3-7/U4-1

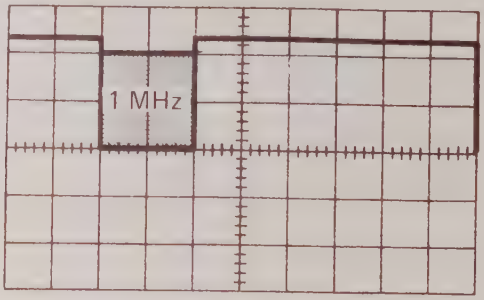


2.0
(V/DIV)

50 mS
(S/DIV)

Waveforms for Table 5.16 continued

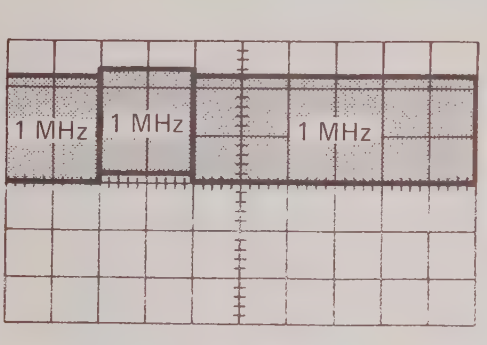
24 (NO.) SAMPLE GATE ENABLE
U4-8



2.0 (V/DIV)

50 mS (S/DIV)

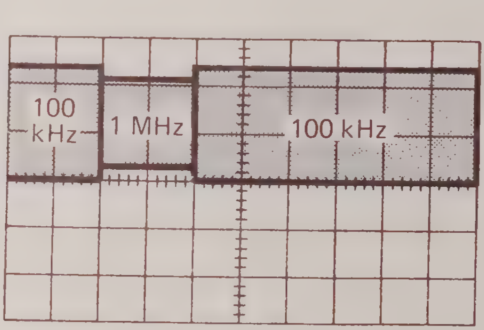
25 (NO.) SAMPLE GATE OUTPUT
U2-6



2.0 (V/DIV)

50 mS (S/DIV)

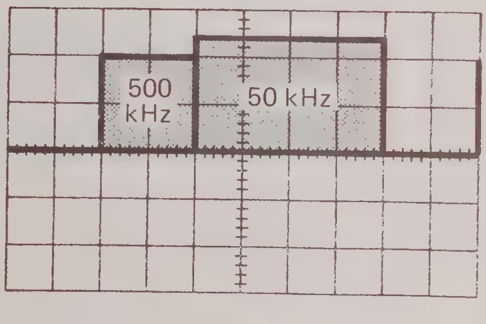
26 (NO.) FREQ/10 SWITCH OUTPUT
U4-6



2.0 (V/DIV)

50 mS (S/DIV)

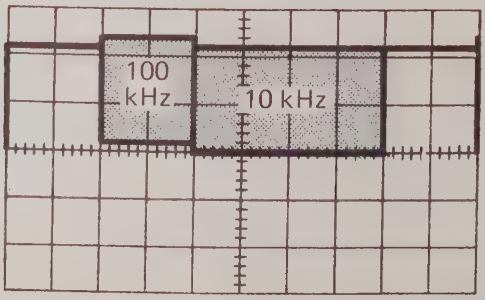
27 (NO.) PRESCALE COUNTER "A" OUTPUT
U3-3



2.0 (V/DIV)

50 mS (S/DIV)

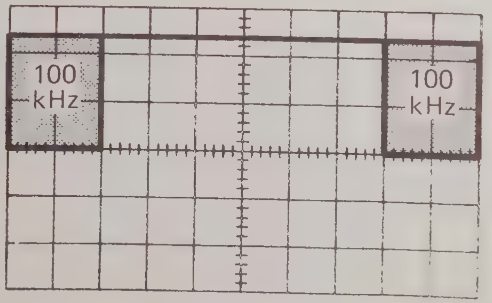
28 (NO.) COUNTER CONTROL F/F "D" INPUT
U9-2



2.0 (V/DIV)

50 mS (S/DIV)

29 (NO.) COUNTER CONTROL F/F CLOCK INPUT
U9-3

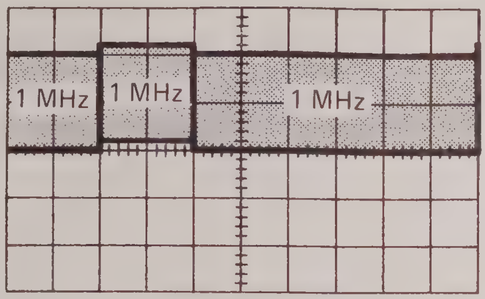


2.0 (V/DIV)

50 mS (S/DIV)

30
(NO.)

LSD COUNTER GATE OUTPUT
U2-8

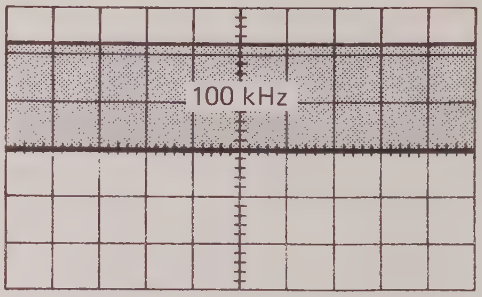


2.0
(V/DIV)

50 mS
(S/DIV)

31
(NO.)

LSD COUNTER OUTPUT
U3-9

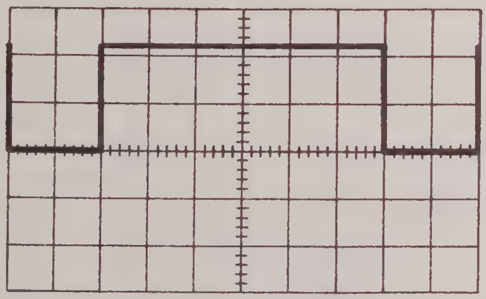


2.0
(V/DIV)

50 mS
(S/DIV)

32
(NO.)

COUNTER CONTROL F/F $\bar{Q}$ OUTPUT
U9-6

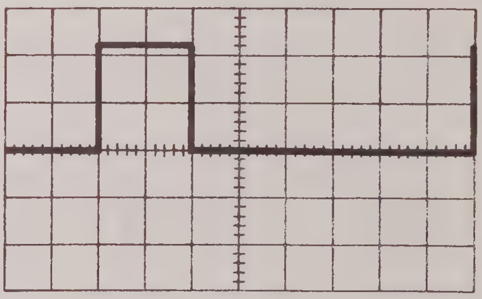


2.0
(V/DIV)

50 mS
(S/DIV)

33
(NO.)

COUNTER GATE ENABLE
U12-11

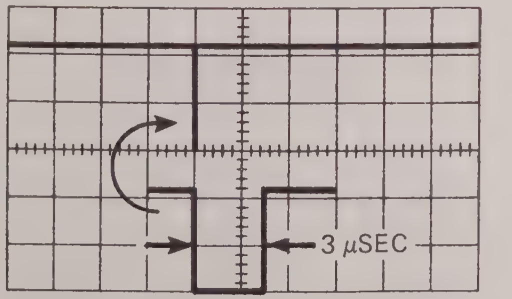


2.0
(V/DIV)

50 mS
(S/DIV)

34
(NO.)

ONE-SHOT "A" OUTPUT ($\bar{Q}$)
U11-4

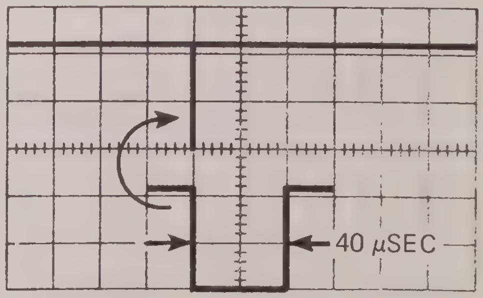


2.0
(V/DIV)

50 mS
(S/DIV)

35
(NO.)

ONE-SHOT "B" OUTPUT ($\bar{Q}$)
U11-12

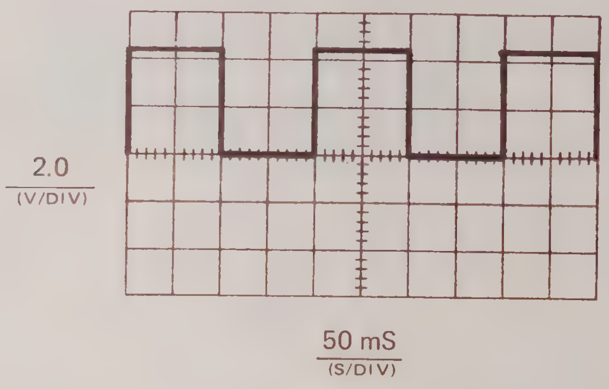


2.0
(V/DIV)

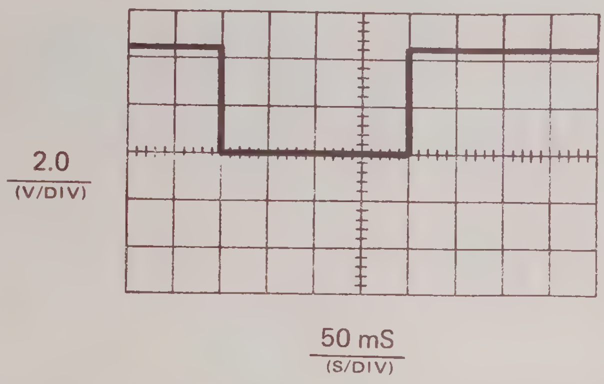
50 mS
(S/DIV)

Waveforms for Table 5.16 continued

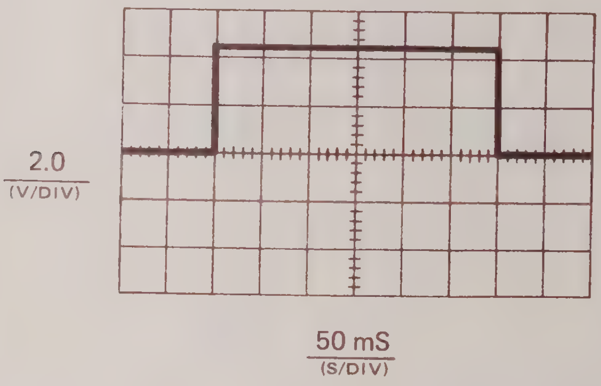
36 (NO.) Q_{e1} COUNTER OUTPUT
U10-18



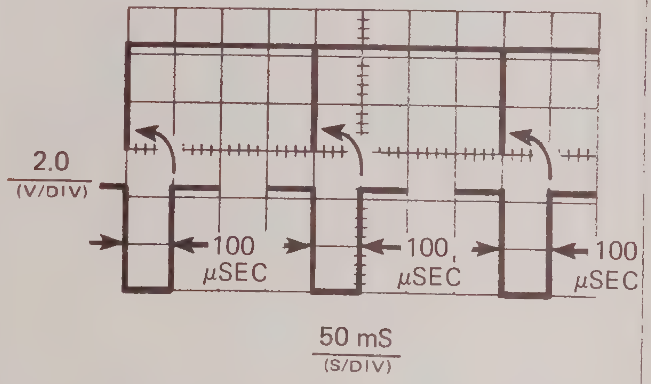
37 (NO.) Q_{e2} COUNTER OUTPUT
U10-16



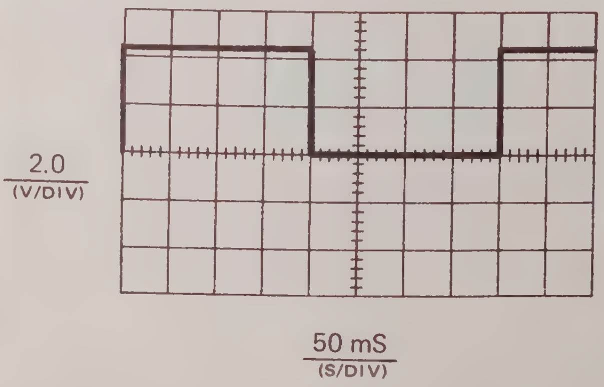
38 (NO.) $\overline{\text{SIGNAL INTEGRATE}}$
U13-6 (EXT TRIG)



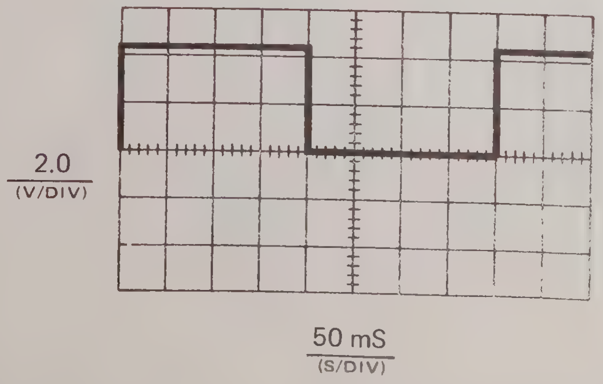
39 (NO.) $\overline{\text{ND}}$ (NULL DETECT)
U6-1/TP2



40 (NO.) + ND F/F OUTPUT
U14-1

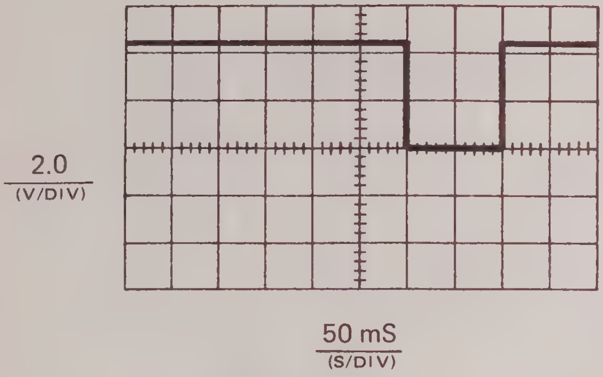


41 (NO.) – ND F/F OUTPUT
U14-2



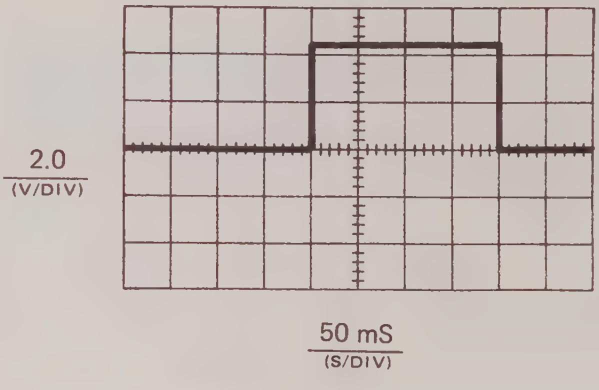
42 (NO.) $\overline{\text{RESET}}$

U13-11



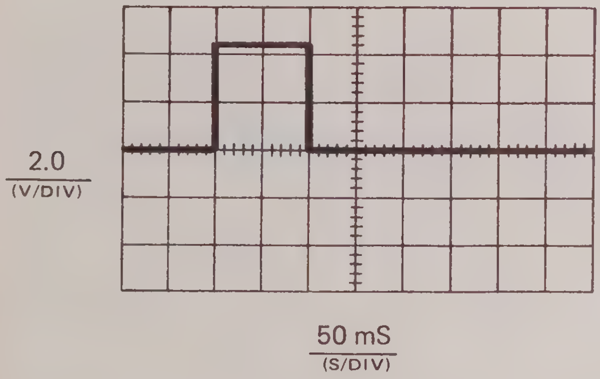
43 (NO.) INTERNAL RESET

U14-12



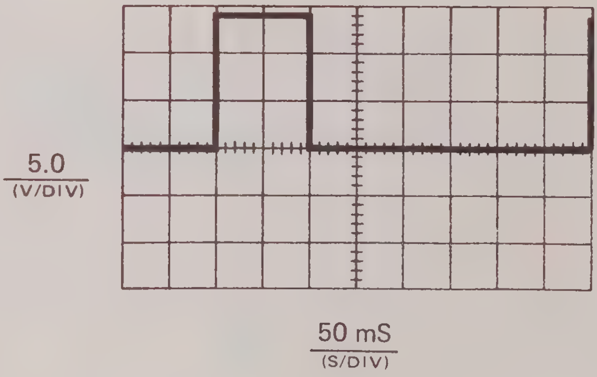
44 (NO.) REFERENCE INTEGRATE ENABLE

U17-13



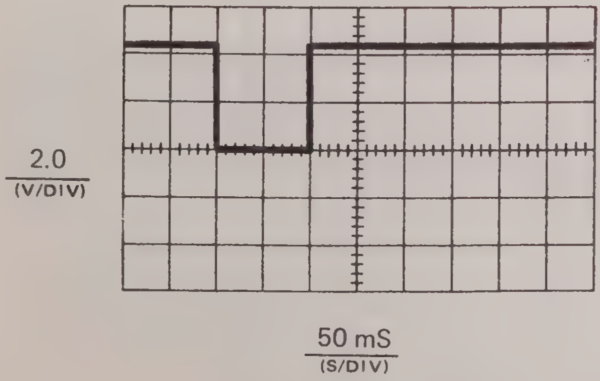
45 (NO.) – REFERENCE SWITCH DRIVE

U18-6



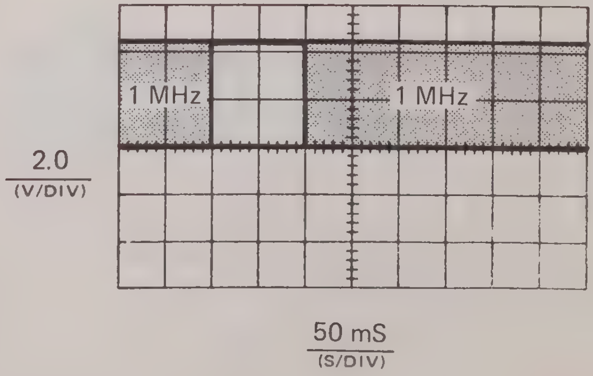
46 (NO.) CLOCK GATE ENABLE

U2-12



47 (NO.) CLOCK GATE OUTPUT

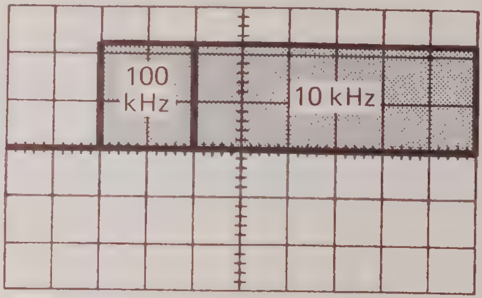
U2-11



Waveforms for Table 5.16 continued

48
(NO.)

PRESCALE COUNTER "D" OUTPUT
U3-7/U4-1

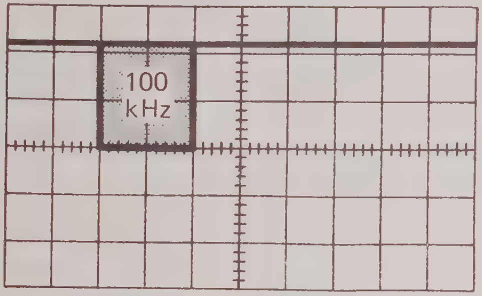


2.0
(V/DIV)

50 mS
(S/DIV)

49
(NO.)

SAMPLE GATE ENABLE
U4-8

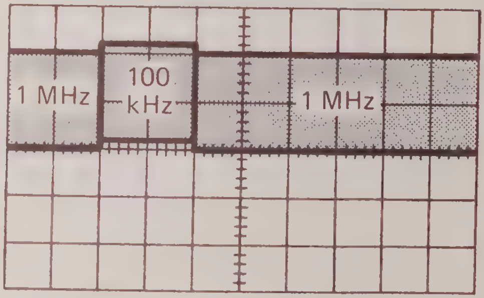


2.0
(V/DIV)

50 mS
(S/DIV)

50
(NO.)

SAMPLE GATE OUTPUT
U2-6

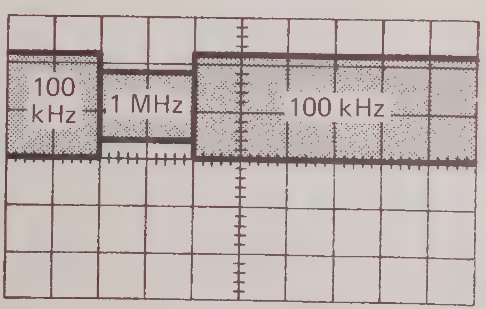


2.0
(V/DIV)

50 mS
(S/DIV)

51
(NO.)

FREQ/10 SWITCH OUTPUT
U4-6

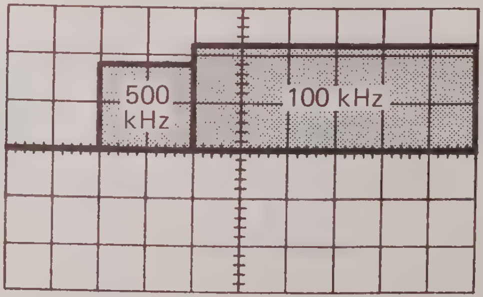


2.0
(V/DIV)

50 mS
(S/DIV)

52
(NO.)

PRESCALE COUNTER "A" OUTPUT
U3-3

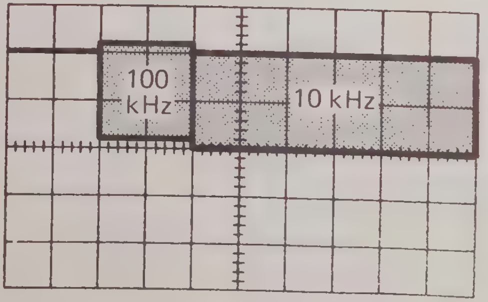


2.0
(V/DIV)

50 mS
(S/DIV)

53
(NO.)

COUNTER CONTROL F/F "D" INPUT
U9-2

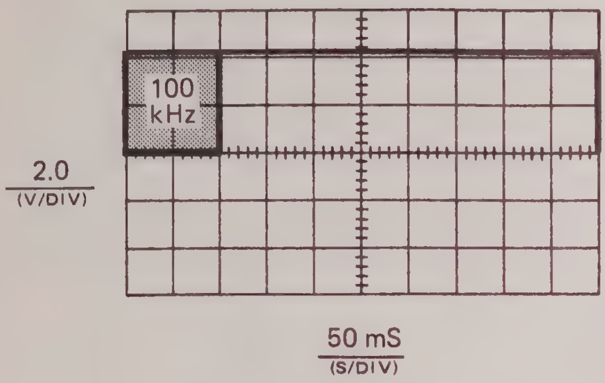


2.0
(V/DIV)

50 mS
(S/DIV)

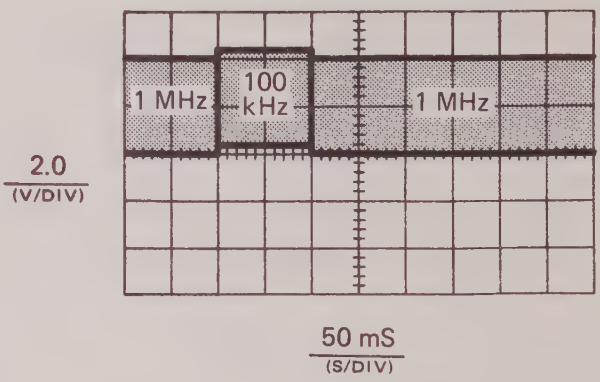
54
(NO.)

COUNTER CONTROL F/F CLOCK INPUT
U9-3



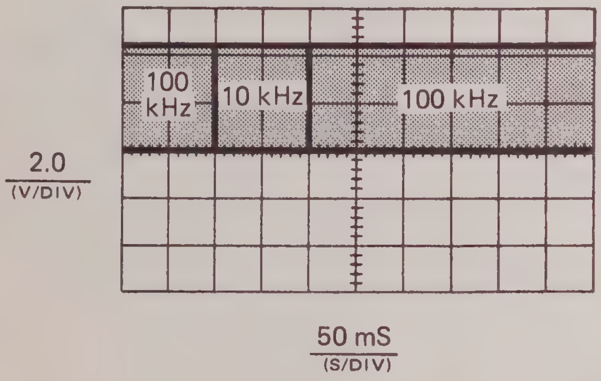
55
(NO.)

LSD COUNTER GATE OUTPUT
U2-8



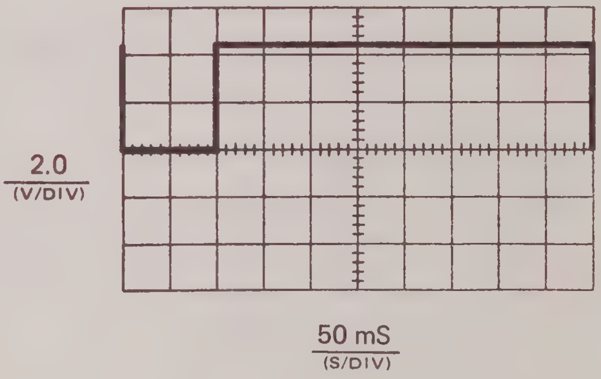
56
(NO.)

LSD COUNTER OUTPUT
U3-9



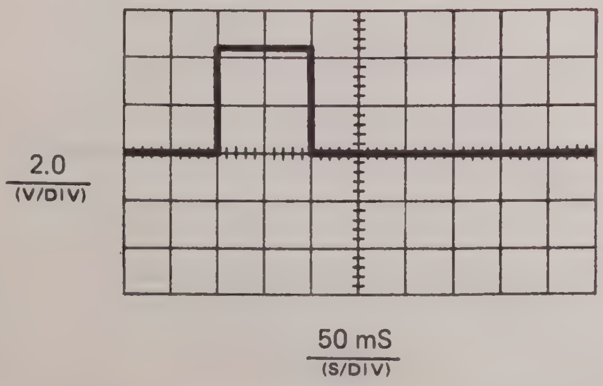
57
(NO.)

COUNTER CONTROL F/F "$\overline{Q}$" OUTPUT
U9-6



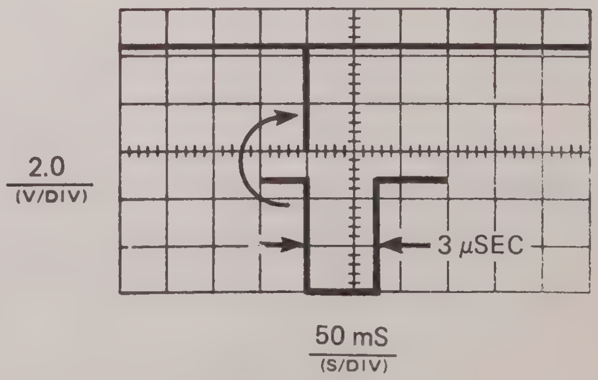
58
(NO.)

COUNTER GATE ENABLE
U12-11



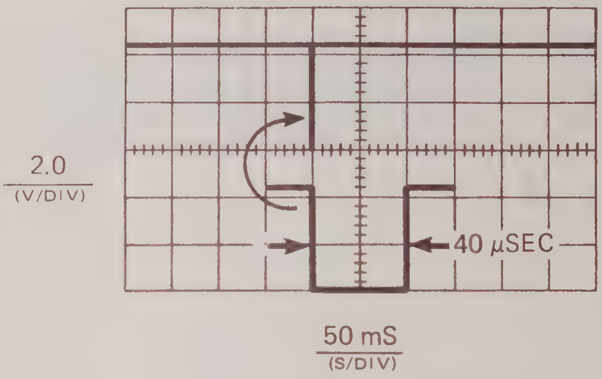
59
(NO.)

ONE-SHOT "A" $\overline{Q}$ OUTPUT
U11-4

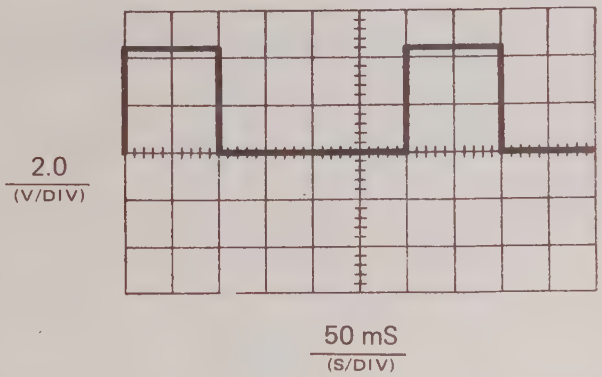


Waveforms for Table 5.16 continued

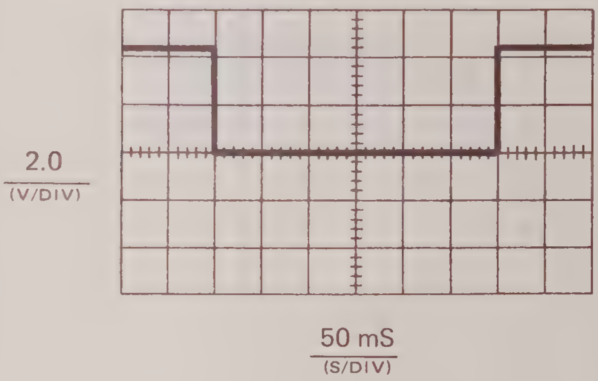
60 (NO.) ONE-SHOT "B" $\overline{Q}$ OUTPUT
U11-12



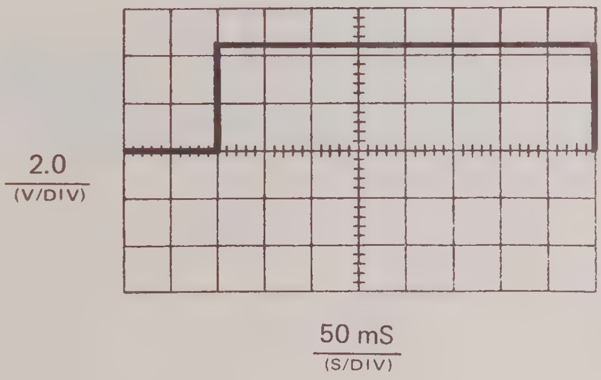
61 (NO.) Q_{e1} COUNTER OUTPUT
U10-18



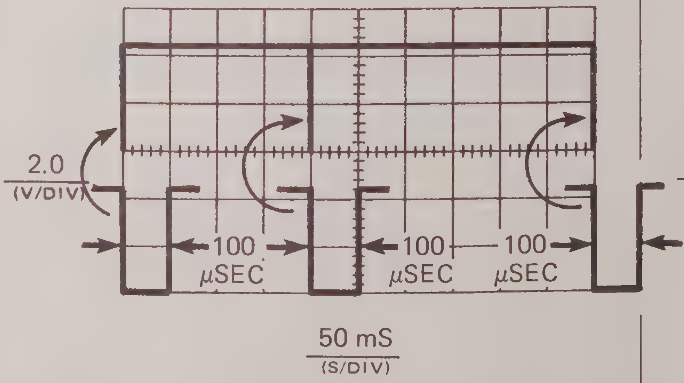
62 (NO.) Q_{e2} COUNTER OUTPUT
U10-16



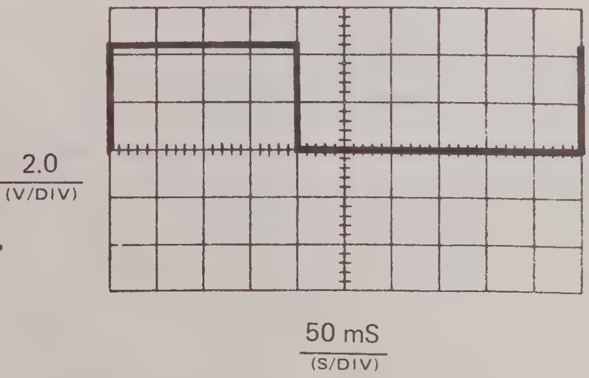
63 (NO.) $\overline{\text{SIGNAL INTEGRATE OUTPUT}}$ (EXT TRIG)
U13-6



64 (NO.) $\overline{\text{ND}}$ ($\overline{\text{NULL DETECTOR}}$) OUTPUT
U6-1/TP2



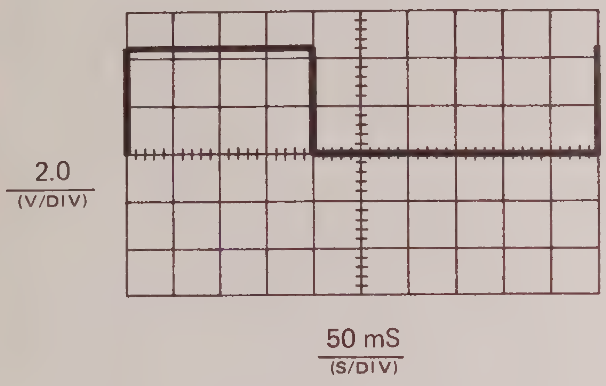
65 (NO.) + ND F/F OUTPUT
U14-1



Waveforms for Table 5.16 continued

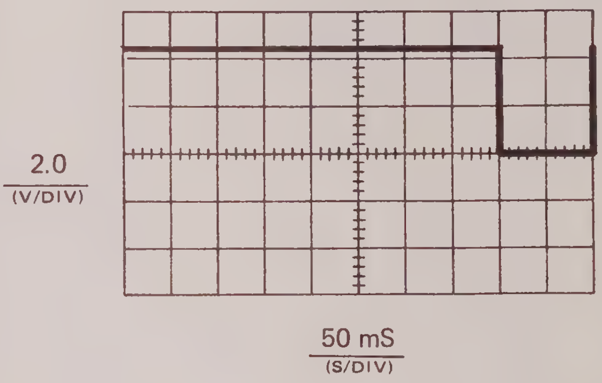
66
(NO.)

– ND F/F OUTPUT
U14-2



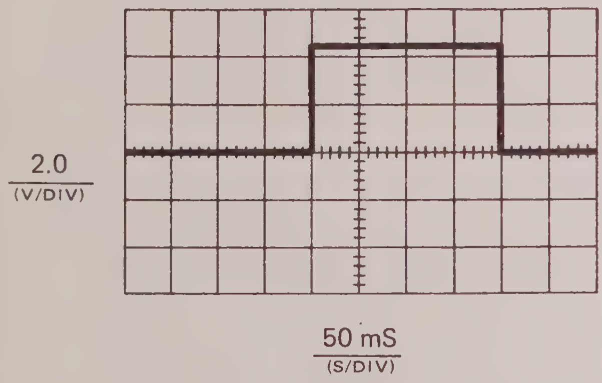
67
(NO.)

$\overline{\text{RESET}}$
U13-11



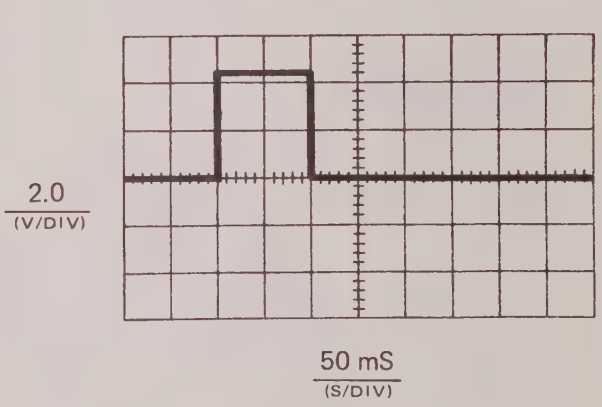
68
(NO.)

INTERNAL RESET
U14-12



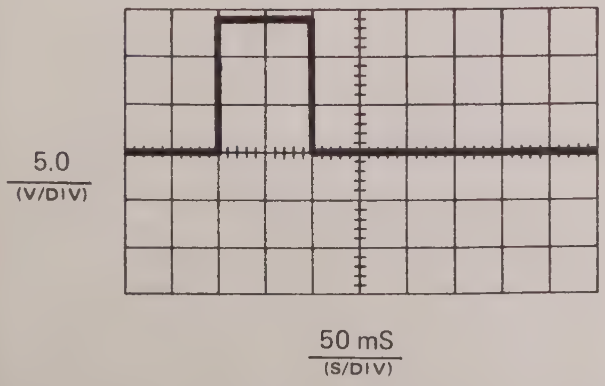
69
(NO.)

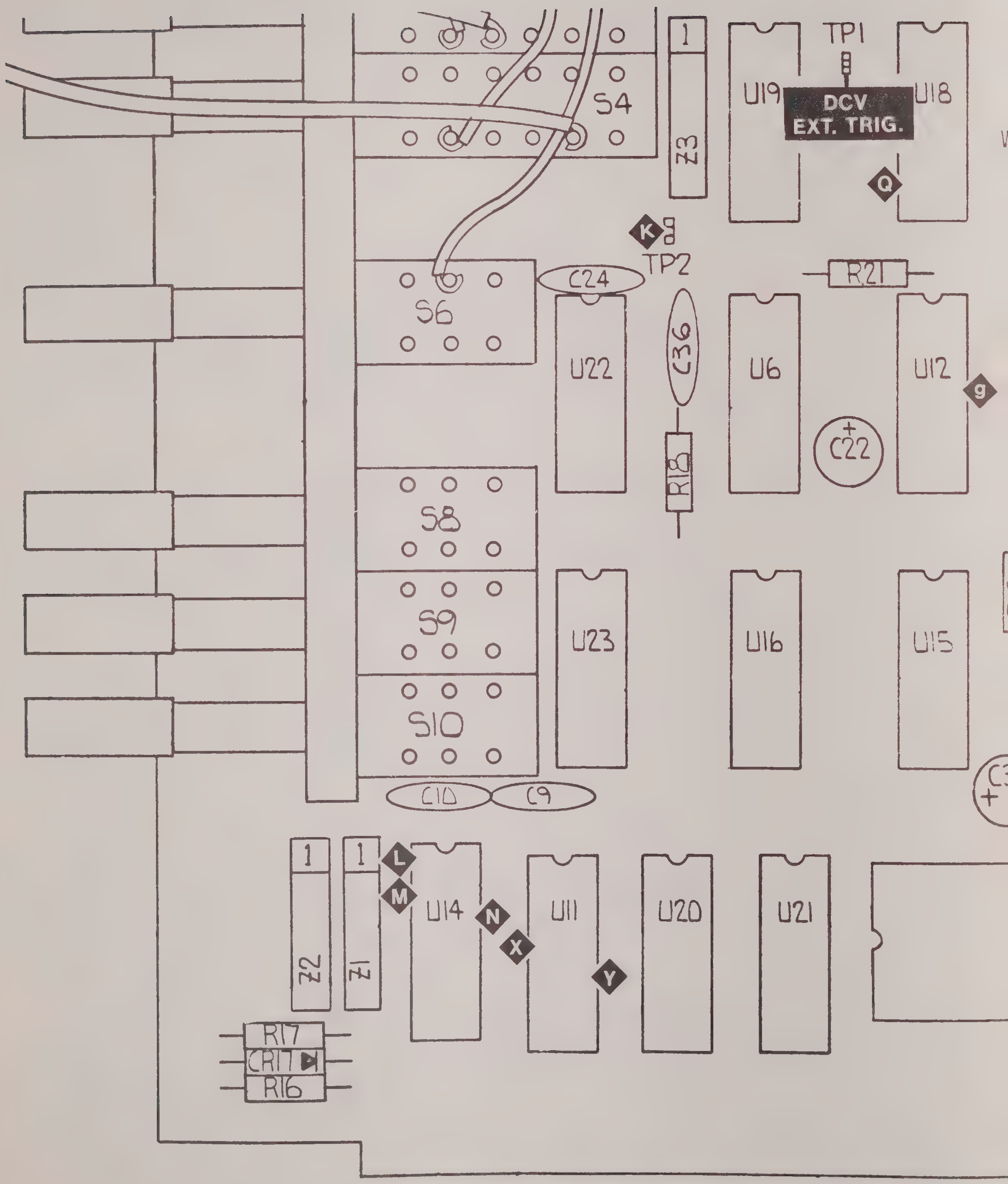
REFERENCE INTEGRATE ENABLE
U17-13



70
(NO.)

– REFERENCE SWITCH DRIVE
U18-6




S4
1
Z3
TP1
U19
DCV
EXT. TRIG.
U18
Q
K
TP2
R21
C24
S6
C36
U22
U6
U12
g
C22
R18
S8
S9
S10
U23
U16
U15
C10
C9
1
1
L
M
U14
N
X
U11
Y
U20
U21
Z2
Z1
R17
CR17
R16

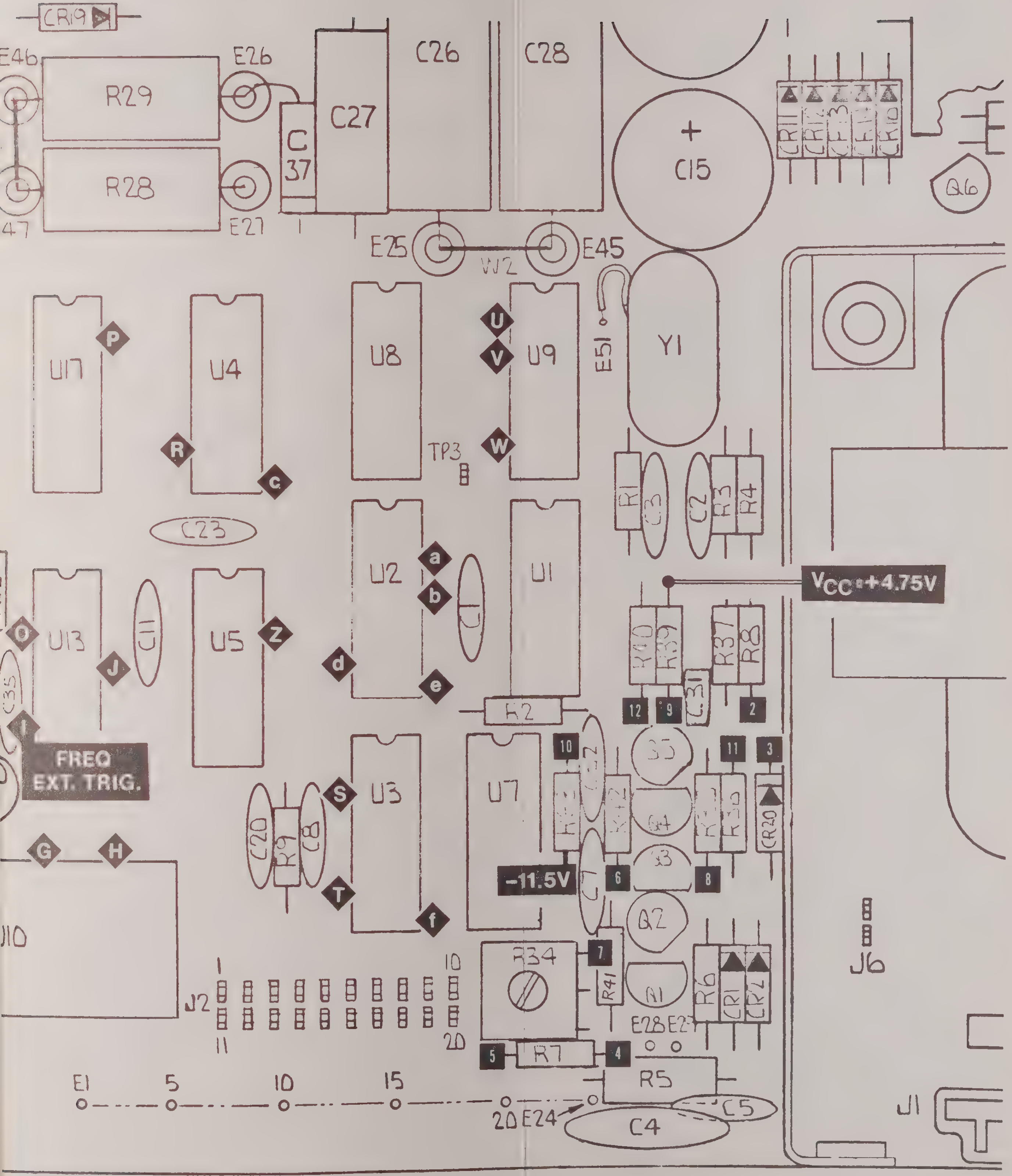

CR19
E46
R29
E26
C27
C26
C28
C
37
C15
+
CR11
CR12
CR13
CR14
CR10
Q6
R28
47
E27
E25
W2
E45
E51
Y1
U17
P
U4
R
c
U8
TP3
U
V
U9
W
C23
U2
a
b
C1
U1
R1
C3
C2
R3
R4
VCC=+4.75V
O
U13
J
C11
U5
Z
d
e
C35
FREQ
EXT. TRIG.
R40
R39
C31
R37
R8
12
9
2
R2
10
Q5
C22
11
3
CR20
U3
S
T
f
C20
R9
C8
U7
Q4
Q3
-11.5V
6
8
C7
Q2
G
H
U10
R34
7
R41
Q1
R6
CR1
CR2
J6
J2
1
10
11
20
E28
E27
5
R7
4
R5
E1
5
10
15
20
E24
C5
C4
J1

Figure 5.25 - Main PCB, Counter & Timing/Control Logic Test Point Locations

Table 5.17 - Main PCB, Measurement Filter Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Signal or function generator having a DC component must be decoupled with a .01 μF cap
	Filter Amp – Input	R30	13	Figure 5.26	±0.0001V DC
	Filter Amp Output	R31	14	Figure 5.26	±0.0001V DC
Remove jumper. Connect input terminals to a function generator set to 10 kHz @ 2V p-p measured at E27	Decoupled Isolator Input	E26	h	Figure 5.26	250 mV p-p (18 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	50 μV p-p (92 dB)
Filter: OUT Generator set to 2V p-p @ 1 kHz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	900 mV p-p (7 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	20 μV p-p (100 dB)
Filter: OUT Generator set to 2V p-p @ 100 Hz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	50 μV p-p (92 dB)
Filter: OUT Generator set to 2V p-p @ 60 Hz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	1.5 mV p-p (62 dB)

Table 5.17 - Main PCB, Measurement Filter Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Filter: OUT Generator set to 2V p-p @ 50 Hz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	2 mV p-p (60 dB)
Filter: OUT Generator set to 2V p-p @ 40 Hz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	4 mV p-p (54 dB)
Filter: OUT Generator set to 2V p-p @ 20 Hz measured @ E27	Decoupled Isolator Input	E26	h	Figure 5.26	1.7V p-p (1 dB)
Filter: IN	Decoupled Isolator Input	E26	h	Figure 5.26	20 mV p-p (40 dB)

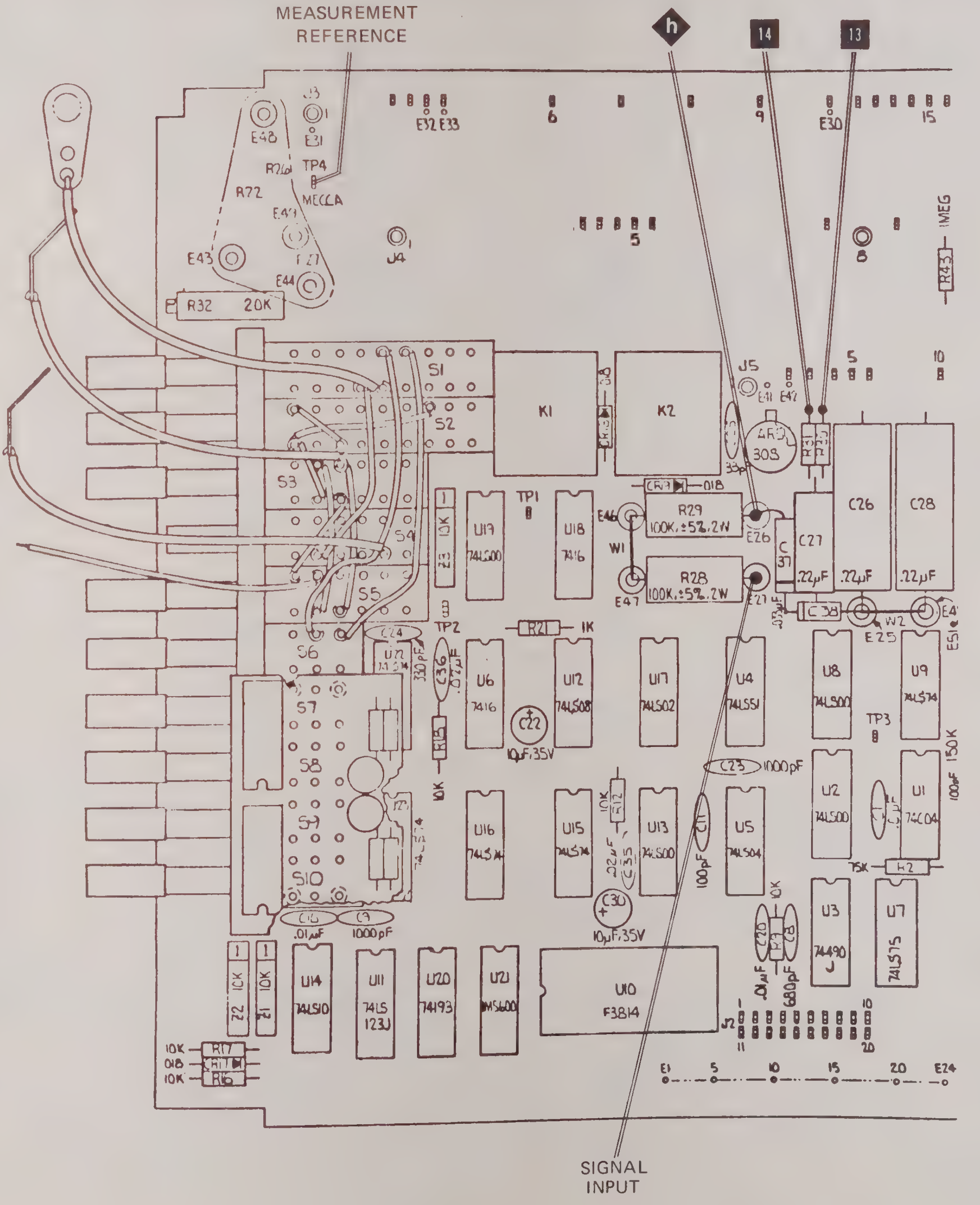

MEASUREMENT REFERENCE
h
14
13
E48
J3
E31
R26
TP4
MECCA
R72
E49
E43
E27
E44
J4
R32 20K
E32 E33
6
9
E30
15
5
8
IMEG
R43
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
K1
K2
J5
E41 E42
AR3 308
33pF
R31
5
10
CR9 .018
TP1
E46
R29 100K,±5%,2W
E26
C37
C27 .22μF
C26 .22μF
C28 .22μF
W1
E47
R28 100K,±5%,2W
E27
.033μF
C38
W2
E25
E51
E4
U19 74LS00
U18 7416
R21 1K
TP2
C24
U22
330pF
C36 .02μF
R13
10K
U6 7416
C22 10μF,35V
U12 74LS08
U17 74LS02
U4 74LS51
U8 74LS00
U9 74LS74
TP3
150K
U16 74LS74
U15 74LS74
R12 10K
C35 .22μF
U13 74LS00
C11 100pF
C23 1000pF
U5 74LS04
U2 74LS00
U1 74C04
100pF
75K
R2
C30 10μF,35V
C10 .01μF
C9 1000pF
Z2 10K
Z1 10K
U14 74LS10
U11 74LS123
U20 74193
U21 MM5600
U10 F3814
C20 .01μF
R1 10K
C8 680pF
U3 7490
U7 74LS75
J2
1
10
11
20
10K R17
.018 CR17
10K R16
E1 5 10 15 20 E24
SIGNAL INPUT

Figure 5.26 - Main PCB, Measurement Filter Test Point Locations

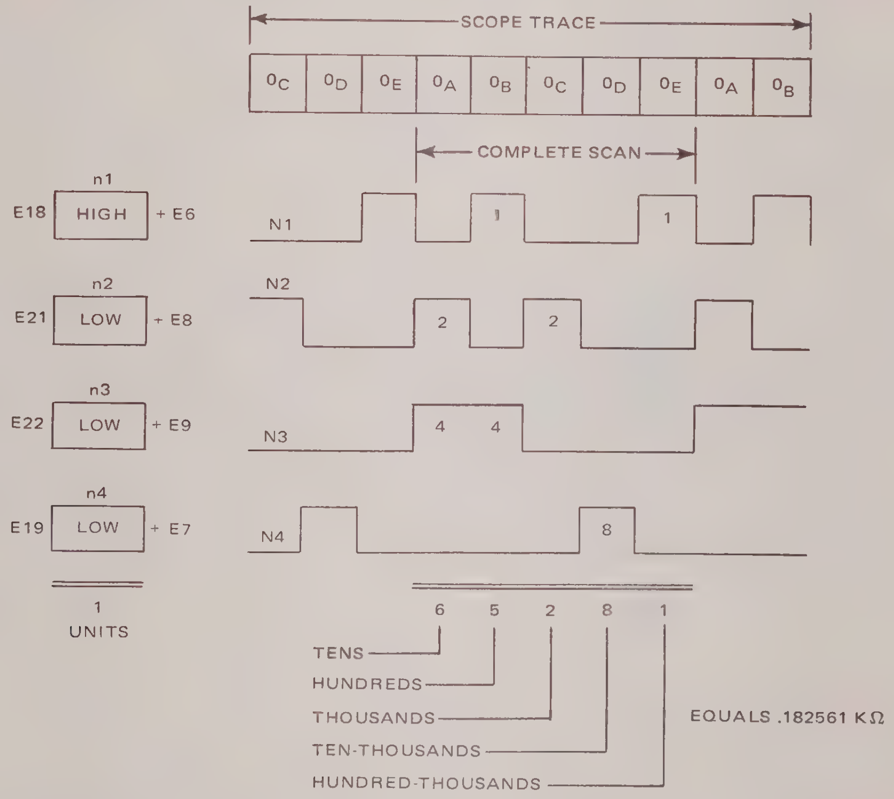
Table 5.18 - Display PCB, Subassembly Performance Test

<table>
<tr><th>Input and Control Setting</th><th>Signal Nomenclature</th><th>Reference Designation</th><th>Test Point</th><th>Illustration Reference</th><th colspan="2">Performance Standard</th></tr>
<tr><td rowspan="4">Function: KΩ
Range: .2 (manual)
Filter: OUT
Input Terminals: J101/J103 connected with a copper jumper to J102/J104. (Guard connected to J102/J104)</td><td></td><td></td><td></td><td></td><td colspan="2">NOTE: All measurements are referenced to TP3 (DIG COM) Main PCB
NOTE: Ext Trig for MUX output drive is J2-3, Main PCB
NOTE: Decimal input logic levels: High = +3.7V DC Low = +0.17V DC</td></tr>
<tr><td>RC1</td><td>E14</td><td>1</td><td>Figure 5.27</td><td>Logic Low</td><td rowspan="3">LED 2 Decimal Point</td></tr>
<tr><td>RC2</td><td>E13</td><td>2</td><td>Figure 5.27</td><td>High</td></tr>
<tr><td>RC3</td><td>E12</td><td>3</td><td>Figure 5.27</td><td>Low</td></tr>
<tr><td rowspan="3">Range: 2 (manual)</td><td>RC1</td><td>E14</td><td>1</td><td>Figure 5.27</td><td>Logic High</td><td rowspan="3">LED 3 Decimal Point</td></tr>
<tr><td>RC2</td><td>E13</td><td>2</td><td>Figure 5.27</td><td>High</td></tr>
<tr><td>RC3</td><td>E12</td><td>3</td><td>Figure 5.27</td><td>Low</td></tr>
<tr><td rowspan="3">Range: 20 (manual)</td><td>RC1</td><td>E14</td><td>1</td><td>Figure 5.27</td><td>Logic Low</td><td rowspan="3">LED 4 Decimal Point</td></tr>
<tr><td>RC2</td><td>E13</td><td>2</td><td>Figure 5.27</td><td>Low</td></tr>
<tr><td>RC3</td><td>E12</td><td>3</td><td>Figure 5.27</td><td>High</td></tr>
<tr><td rowspan="3">Range: 200 (manual)</td><td>RC1</td><td>E14</td><td>1</td><td>Figure 5.27</td><td>Logic High</td><td rowspan="3">LED 5 Decimal Point</td></tr>
<tr><td>RC2</td><td>E13</td><td>2</td><td>Figure 5.27</td><td>Low</td></tr>
<tr><td>RC3</td><td>E12</td><td>3</td><td>Figure 5.27</td><td>High</td></tr>
<tr><td rowspan="3">Range: 2000 (manual)</td><td>RC1</td><td>E14</td><td>1</td><td>Figure 5.27</td><td>Logic Low</td><td rowspan="3">LED 6 Decimal Point</td></tr>
<tr><td>RC2</td><td>E13</td><td>2</td><td>Figure 5.27</td><td>High</td></tr>
<tr><td>RC3</td><td>E12</td><td>3</td><td>Figure 5.27</td><td>High</td></tr>
</table>

Table 5.18 - Display PCB, Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Range: 20,000 (manual)	RC1	E14	1	Figure 5.27	Logic High LED 7 Decimal Point
	RC2	E13	2	Figure 5.27	High
	RC3	E12	3	Figure 5.27	High
	O_D	E1	A	Figure 5.27	Waveform 1
	O_C (Ext Trig)	E2	B	Figure 5.27	Waveform 2
	O_B	E3	C	Figure 5.27	Waveform 3
	O_E	E4	D	Figure 5.27	Waveform 4
	O_A	E5	E	Figure 5.27	Waveform 5
	LED 3 DR	Q2 Collector	F	Figure 5.27	Waveform 6
	LED 4 DR	Q3 Collector	G	Figure 5.27	Waveform 7
	LED 5 DR	Q4 Collector	H	Figure 5.27	Waveform 8
	LED 2 DR	Q1 Collector	I	Figure 5.27	Waveform 9
	LED 6/7 DR	Q5/Q6 Collector	J	Figure 5.27	Waveform 10
Remove Short from Input Terminals	$\overline{\text{Blank}}$	E20	K	Figure 5.27	Waveform 11 Display flashes 200000
Connect Input Terminals to a copper jumper. Connect DIG COM to E24	$\overline{\text{LED Segment}}$ Test			Figure 5.27	All Decade Segments illuminate 8 8 8 8 8 8
Remove Short from Input Terminals. Connect input terminal to a resistance value. Example: .182561 (KΩ) Ext Trig Scope @ J2-3, Main PCB	N_1 Counter Output	E6	L	Figure 5.27	Waveform 12
	N_2 Counter Output	E8	M	Figure 5.27	Waveform 13
	N_3 Counter Output	E9	N	Figure 5.27	Waveform 14
	N_4 Counter Output	E7	O	Figure 5.27	Waveform 15

Table 5.18 - Display PCB, Subassembly Performance Test continued

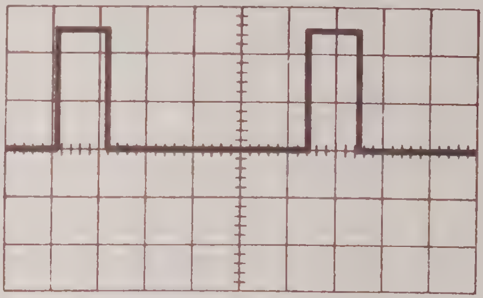
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Ext Trig Scope @ TP1, Main PCB	n_1 LSD Counter Output	E18	4	Figure 5.27	Logic High
	n_2 LSD Counter Output	E21	5	Figure 5.27	Logic Low
	n_3 LSD Counter Output	E22	6	Figure 5.27	Logic Low
	n_4 LSD Counter Output	E19	7	Figure 5.27	Logic Low
					
Function: DCV Range: AUTO Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected to a +1V source	$\overline{\text{Plus Polarity}}$	E10	8	Figure 5.27	Logic Low
Change Input to −1V Source	$\overline{\text{Minus Polarity}}$	E11	9	Figure 5.27	Logic Low
Disconnect Input Scope and Ext Trig Cables					

SCOPE TRACE
0C 0D 0E 0A 0B 0C 0D 0E 0A 0B
COMPLETE SCAN
n1
E18 HIGH + E6
N1
1
1
n2
E21 LOW + E8
N2
2
2
n3
E22 LOW + E9
N3
4
4
n4
E19 LOW + E7
N4
8
1
UNITS
6 5 2 8 1
TENS
HUNDREDS
THOUSANDS
TEN-THOUSANDS
HUNDRED-THOUSANDS
EQUALS .182561 KΩ

Waveforms for Table 5.18

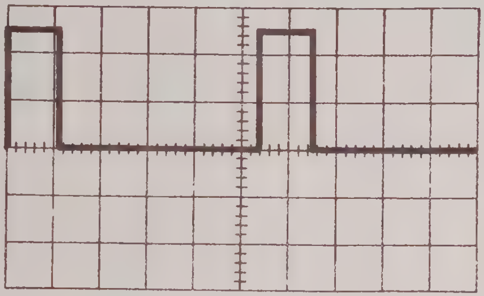
1
(NO.)

O_D MUX DR
E1



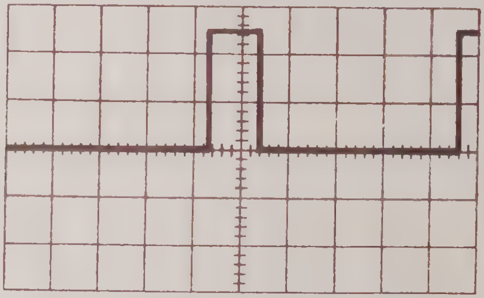
2
(NO.)

O_C MUX DR (EXT TRIG)
E2



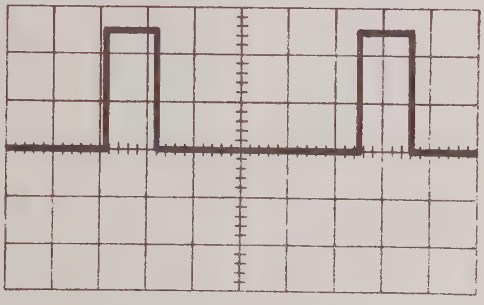
3
(NO.)

O_B MUX DR
E3



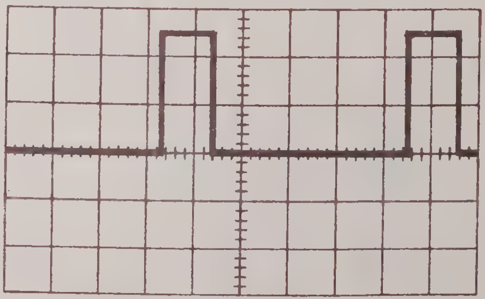
4
(NO.)

O_E MUX DR
E4



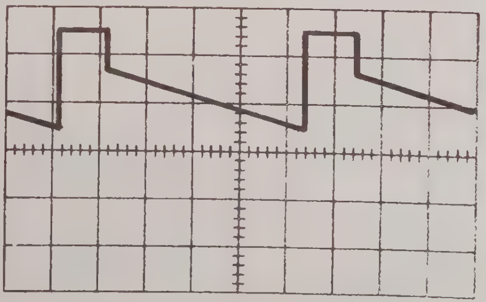
5
(NO.)

O_A MUX DR
E5



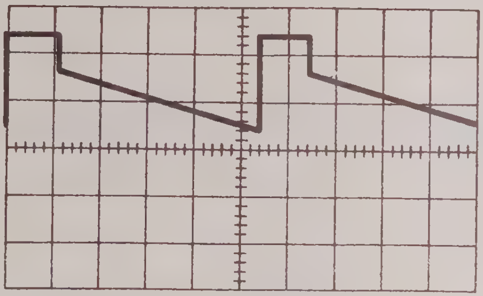
6
(NO.)

LED 3 DR
Q2 COLLECTOR



7
(NO.)

LED 4 DR
Q3 COLLECTOR

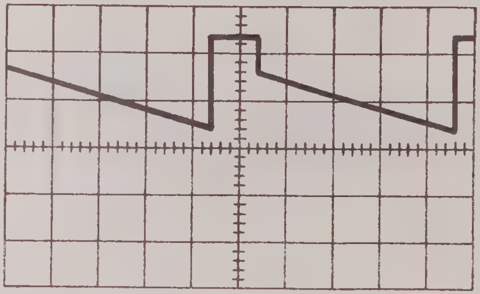


2.0
(V/DIV)

2 mS
(S/DIV)

8
(NO.)

LED 5 DR
Q4 COLLECTOR

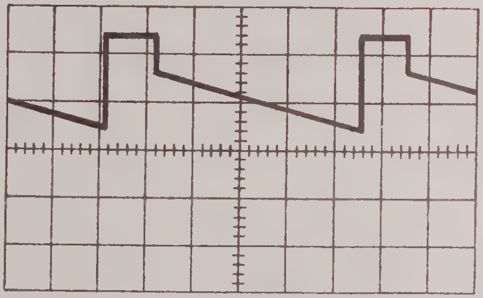


2.0
(V/DIV)

2 mS
(S/DIV)

9
(NO.)

LED 2 DR
Q1 COLLECTOR

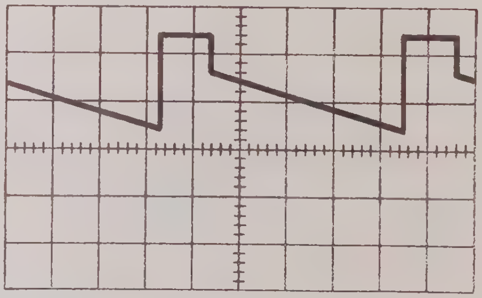


2.0
(V/DIV)

2 mS
(S/DIV)

10
(NO.)

LED 617 DR
Q5/6 COLLECTORS

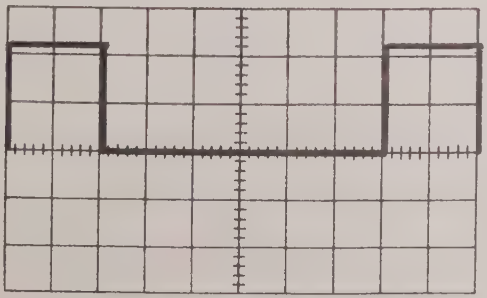


2.0
(V/DIV)

2 mS
(S/DIV)

11
(NO.)

$\overline{\text{BLANK}}$
E20



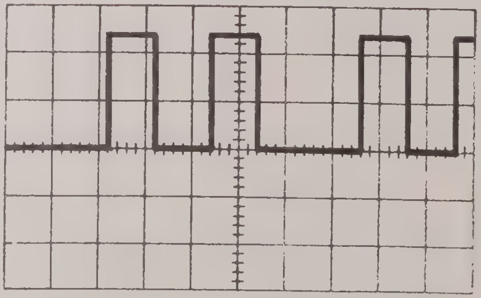
2.0
(V/DIV)

50 mS
(S/DIV)

EXT TRIG @ TP1 (SID) MAIN PCB

12
(NO.)

N_1 COUNTER OUTPUT
E6



2.0
(V/DIV)

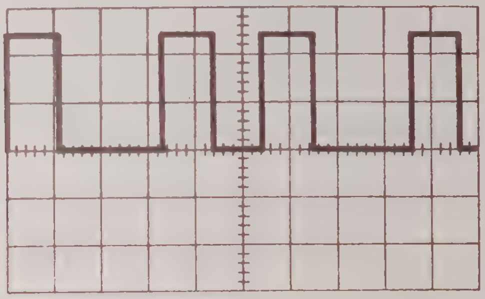
2 mS
(S/DIV)

EXT TRIG @ J2-3, MAIN PCB

Waveforms for Table 5.18 continued

13
(NO.)

N_2 COUNTER OUTPUT
E8

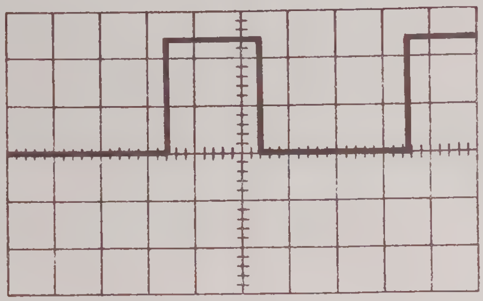


2.0
(V/DIV)

2 mS
(S/DIV)

14
(NO.)

N_3 COUNTER OUTPUT
E9

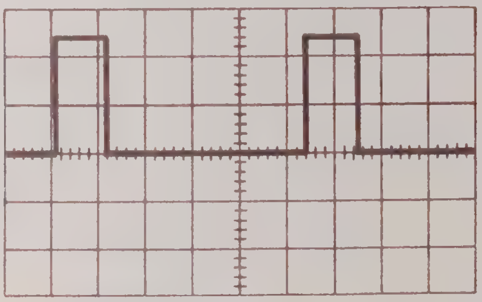


2.0
(V/DIV)

2 mS
(S/DIV)

15
(NO.)

N_4 COUNTER OUTPUT
E7



2.0
(V/DIV)

2 mS
(S/DIV)

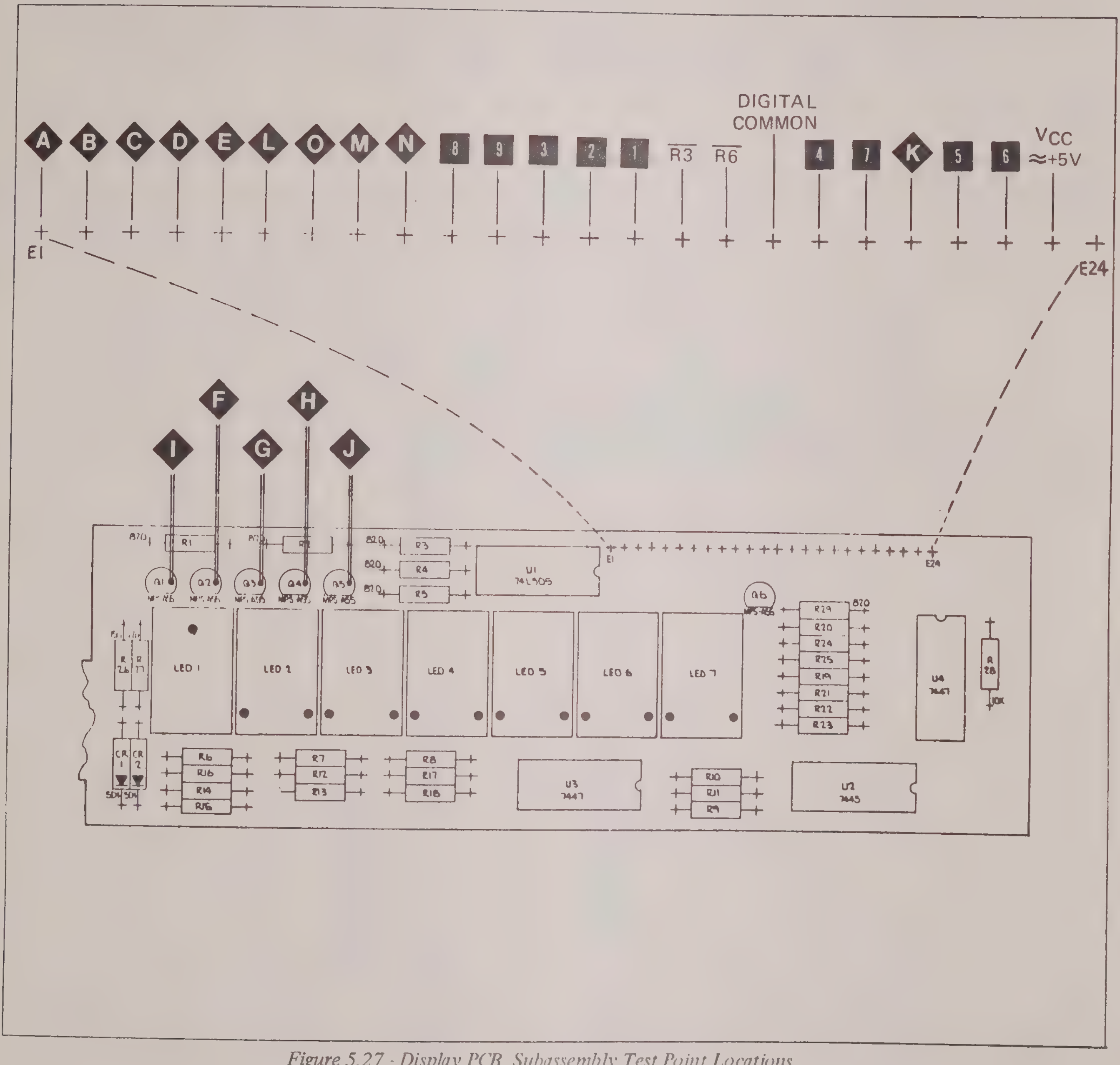
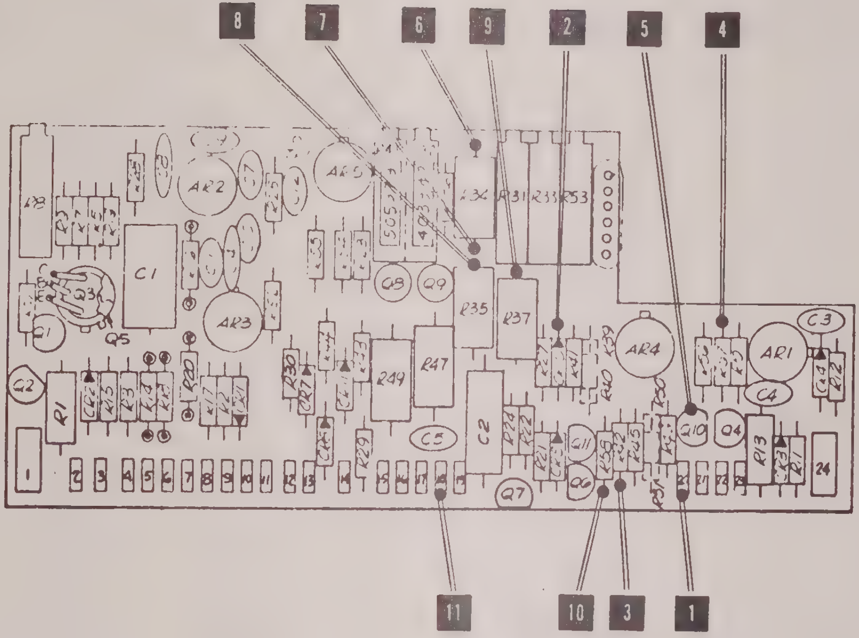

A
B
C
D
E
L
O
M
N
8
9
3
2
1
R3
R6
DIGITAL COMMON
4
7
K
5
6
VCC ≈+5V
E1
E24
F
H
I
G
J
R1
R2
R3
R4
R5
820
U1 74LS05
Q1
Q2
Q3
Q4
Q5
Q6
LED 1
LED 2
LED 3
LED 4
LED 5
LED 6
LED 7
R29
R20
R24
R25
R19
R21
R22
R23
U4 7447
R 28
10K
R 26
R 27
CR 1
CR 2
R6
R16
R14
R15
R7
R12
R13
R8
R17
R18
U3 7447
R10
R11
R9
U2 7445

Figure 5.27 - Display PCB, Subassembly Test Point Locations

Table 5.19 - Reference Isolator PCB, Internal Reference Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) NOTE: Reference Zener Diodes (CR10) can vary from +6.2V to +6.4V. Performance standard voltages are measured values on a sample DMM
Assembly is to be mounted on Extender PCB, P/N 403949	Reference Common	P5-20	1	Figure 5.28	+0.000156V DC
	Reference Zener	CR10 (Cathode)	2	Figure 5.28	+6.3326V DC
	Op Amp + In	R42	3	Figure 5.28	+6.1924V DC
	Op Amp Output	R57	4	Figure 5.28	+10.6387V DC
	Reference Gen. Output	Q10 (Emitter)	5	Figure 5.28	+10.0022V DC
	Bridge Gain Resistor	R34	6	Figure 5.28	+9.9918V DC
	Op Amp – In	R34	7	Figure 5.28	+6.1998V DC
	Bridge Gain Resistor	R35	8	Figure 5.28	+0.99620V DC
	Bridge Gain Resistor	R37	9	Figure 5.28	+0.99516V DC
	Current Sink Bias	R58	10	Figure 5.28	–0.63020V DC
	+1V Reference Out	P5-18	11	Figure 5.28	+0.99583V DC


8
7
6
9
2
5
4
11
10
3
1
AR1
AR2
AR3
AR4
AR5
C1
C2
C3
C4
C5
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
R1
R13
R31
R33
R34
R35
R37
R47
R49
R53

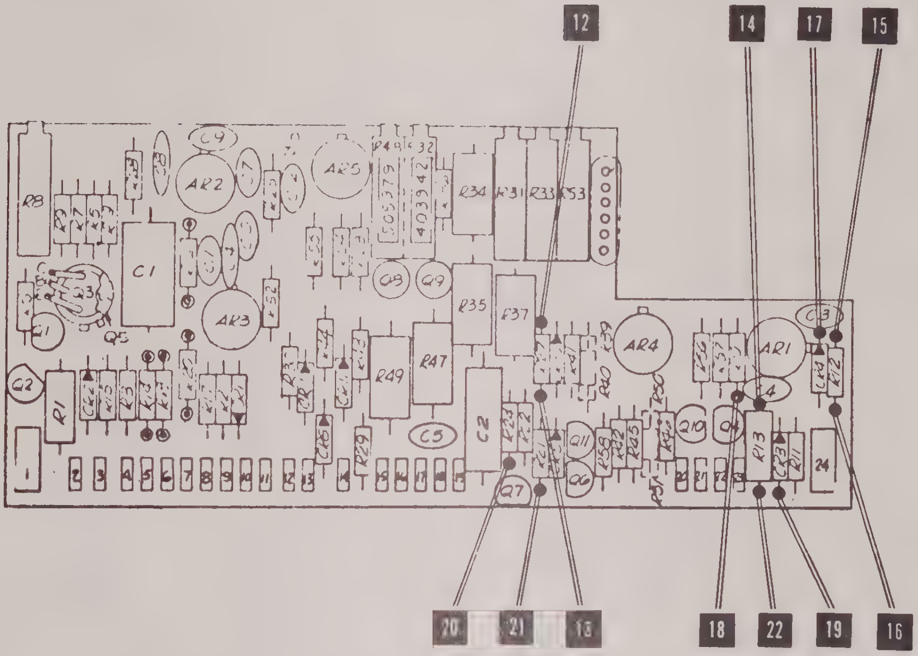
Typical DC Voltages for Reference Generator
Referenced to TP4 (MECCA) on Main PCB

1	+0.000156V DC	7	+6.1998V DC
2	+6.3326V DC	8	+0.99620V DC
3	+6.1924V DC	9	+0.99516V DC
4	+10.6387V DC	10	-0.63020V DC
5	+10.0022V DC	11	+0.99583V DC
6	+9.9918V DC		

Figure 5.28 - DC Reference Generator Test Point Locations

Table 5.20 - Reference Isolator PCB, KΩ Reference Generator Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) on Main PCB NOTE: DC reference generator circuit must be operational to obtain test results for the KΩ reference generator
Assembly is to be mounted on Extender PCB, P/N 403949	+10V DC Reference Generator Output	R27	12	Figure 5.29	+9.9986V DC
	KΩ Ref Op Amp – In	R27	13	Figure 5.29	+8.2630V DC
	KΩ Ref Op Amp + In	R13	14	Figure 5.29	+9.9985V DC
	KΩ Ref Op Amp Output	R12	15	Figure 5.29	+17.276V DC
	KΩ Ref Op Amp Decoupled Output	R12	16	Figure 5.29	+17.087V DC
	KΩ Over Voltage Protection Bias	CR4 (Cathode)	17	Figure 5.29	+17.633V DC
	KΩ Over Voltage Protection Bias	R10	18	Figure 5.29	+17.854V DC
	KΩ Over Voltage Protection Bias	CR3 (Anode)	19	Figure 5.29	+10.0525V DC
	KΩ Open Terminal Clamp Bias	R24	20	Figure 5.29	+17.009V DC
	KΩ Open Terminal Clamp Bias	R21	21	Figure 5.29	–2.5707V DC
	+10V KΩ Ref Voltage Output	R13	22	Figure 5.29	+9.9987V DC


12
14
17
15
R8
C9
AR2
AR5
C1
AR3
R34
R31
R33
R53
R35
R37
AR4
AR1
C3
Q8
Q9
Q1
Q2
Q5
R1
R49
R47
C2
C5
Q7
Q11
Q6
Q10
Q4
R13
C4
24
20
21
13
18
22
19
16

Typical Voltages for KΩ Reference Generator Circuit
Referenced to TP4 (MECCA) on Main PCB

12	+9.9986V DC
13	+8.2630V DC
14	+9.9985V DC
15	+17.276V DC
16	+17.087V DC
17	+17.633V DC
18	+17.854V DC
19	+10.5025V DC
20	+17.009V DC
21	−2.5707V DC
22	+9.9987V DC

Figure 5.29 - KΩ Reference Generator Test Point Locations

Table 5.21 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test

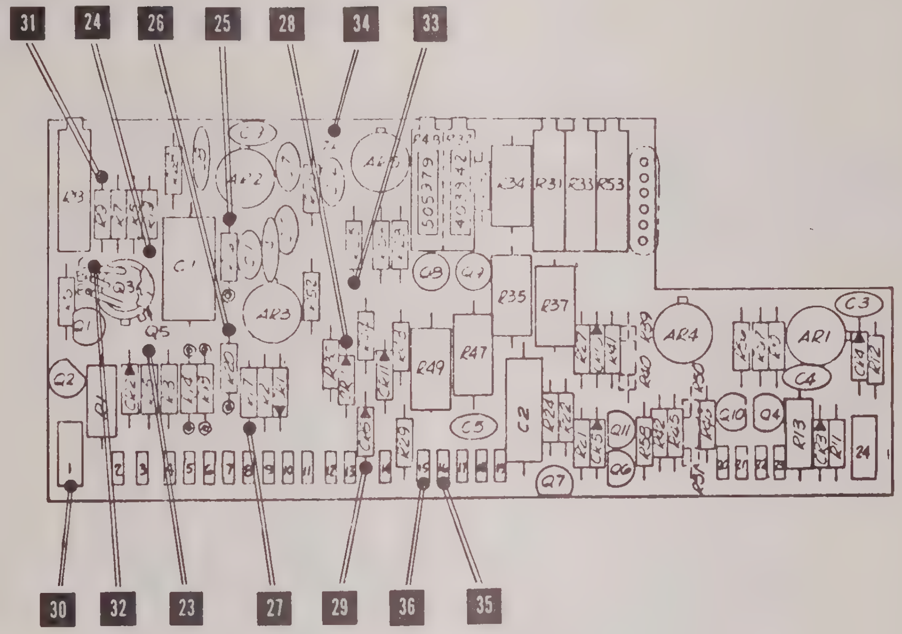
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
Assembly to be mounted on Extender PCB, P/N 403949	Isolator Op Amp – In	R15	23	Figure 5.30	+1.34425V DC
	Isolator Op Amp + In	R19	24	Figure 5.30	+1.34386V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.30	–0.44451V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.30	–0.44475V DC
	1st Stage Emitter Bias	R17	27	Figure 5.30	–0.44515V DC
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.30	+4.9464V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.30	–5.1634V DC
	Bootstrap Common	J5-1	30	Figure 5.30	–.004212V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.30	+0.32148V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.30	+0.113454V DC
	Current Sink Op Amp Output	R55	33	Figure 5.30	–0.005905V DC
	Isolator Output	TP1	34	Figure 5.30	–0.000002V DC

Table 5.21 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Remove copper jumper Range: .2 (manual) Connect the Input Terminals to a DC standard set to +.100000V DC	Isolator Op Amp – In	R15	23	Figure 5.30	+1.44185V DC
	Isolator Op Amp + In	R19	24	Figure 5.30	+1.44235V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.30	–0.34512V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.30	–0.34531V DC
	1st Stage Emitter Bias	R17	27	Figure 5.30	–0.34565V DC
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.30	+5.0446V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.30	–5.0639V DC
	Bootstrap Common	J5-1	30	Figure 5.30	+0.095790V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.30	+0.42076V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.30	+0.21343V DC
	Current Sink Op Amp Output	R55	33	Figure 5.30	–0.99200V DC
	Isolator Output	TP1	34	Figure 5.30	+0.99998V DC
	Isolator X10 DR	J5-16	35	Figure 5.30	–0.54680V DC
	Isolator X1 DR	J5-15	36	Figure 5.30	–4.7223
Range: 2 (manual) Connect Input Terminals to a –1.00000V DC	Isolator Op Amp – In	R15	23	Figure 5.30	+0.36620V DC
	Isolator Op Amp + In	R19	24	Figure 5.30	+0.36630V DC
	1st Stage Emitter Bias (Signal)	R16	25	Figure 5.30	–1.44490V DC
	1st Stage Emitter Bias (Reference)	R20	26	Figure 5.30	–1.44497V DC
	1st Stage Emitter Bias	R17	27	Figure 5.30	–1.44525V DC

Table 5.21 - Reference Isolator PCB, Isolator/Bootstrap Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	+ Bootstrap Voltage	CR7 (Cathode)	28	Figure 5.30	+3.9634V DC
	– Bootstrap Voltage	CR8 (Anode)	29	Figure 5.30	–6.1567V DC
	Bootstrap Common	J5-1	30	Figure 5.30	–1.00420V DC
	Input Bias Network Divider Bias	R9	31	Figure 5.30	–0.67852V DC
	Input Bias Network Diode Drop	Q3 (Collector)	32	Figure 5.30	–0.88592V DC
	Current Sink Op Amp Output	R55	33	Figure 5.30	+1.00380V DC
	Isolator Output	TP1	34	Figure 5.30	–0.99994V DC
	Isolator X10 DR	J5-16	35	Figure 5.30	–4.6812V DC
	Isolator X1 DR	J5-15	36	Figure 5.30	–0.54630V DC
Remove Input Voltage and remove Extender PCB					

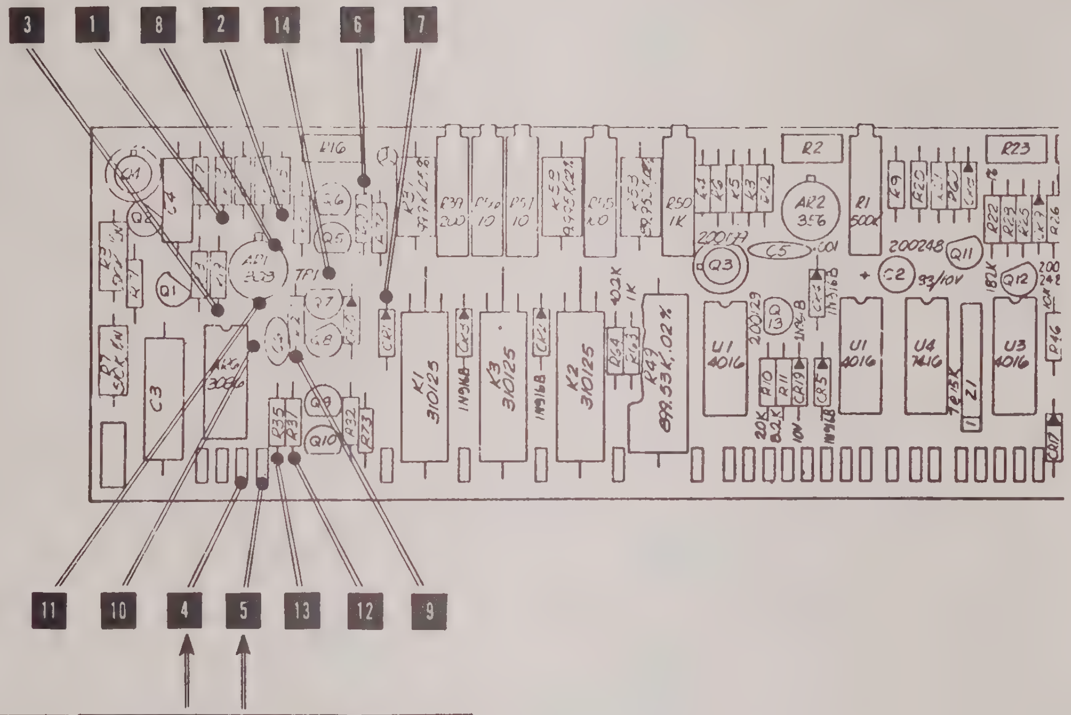

31
24
26
25
28
34
33
30
32
23
27
29
36
35
AR1
AR2
AR3
AR4
C1
C2
C3
C4
C5
C8
Q2
Q4
Q5
Q6
Q7
Q10
Q11
R1
R13
R31
R33
R34
R35
R37
R47
R49
R53

	Input Short	+.1V/ .2 Rng	−1V/ 2 Rng
23	+1.34425	+1.44185	+0.36620
24	+1.34386	+1.44235	+0.36630
25	−0.44451	−0.34512	−1.44490
26	0.44475	0.34531	−1.44497
27	0.44515	−0.34565	1.44525
28	+4.9464	+5.0446	+3.9634
29	−5.1634	−5.0639	−6.1567
30	−0.004212	+.095790	−1.00420
31	+0.32148	+0.42076	−0.67852
32	+0.113454	+0.21343	−0.88592
33	−0.005905	−0.99200	+1.00380
34	−0.000002	+0.99998	−0.99994
35	−0.54680	−0.54680	−4.6812
36	−4.7223	−4.7223	−0.54630

Figure 5.30 - Isolator/Bootstrap Test Point Locations

Table 5.22 - Digitizer PCB, HV Buffer Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 200 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Assy. is to be mounted on Extender PCB, P/N 403951					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	HV Buffer Op Amp – In	R14	1	Figure 5.31	+7.4196V DC
	HV Buffer Op Amp + In	R15	2	Figure 5.31	+7.4201V DC
	1st Stage Source Bias	R19	3	Figure 5.31	+2.0093V DC
	+300V Source	J3-4	4	Figure 5.31	+263.35V DC
	–300V Source	J3-5	5	Figure 5.31	–263.75V DC
	Plus Regulator Bias	R29	6	Figure 5.31	+134.50V DC
	Plus Zener Reference Voltage	CR10 (Cathode)	7	Figure 5.31	+9.8629V DC
	Plus Op Amp Drive Voltage	AR1-7	8	Figure 5.31	+9.3336V DC
	Op Amp Output	R27	9	Figure 5.31	–0.07155V DC
	Minus Reference Voltage	AR6-13	10	Figure 5.31	–9.1338V DC
	Minus Op Amp Drive Voltage	AR1-4	11	Figure 5.31	–8.5548V DC
	Minus Regulator Bias	R31	12	Figure 5.31	–135.00V DC
	Current Generator Emitter Bias	R35	13	Figure 5.31	–0.69025V DC
	HV Buffer Output	TP1	14	Figure 5.31	+0.00007V DC


3
1
8
2
14
6
7
11
10
4
5
13
12
9
Q1
Q2
Q4
C4
AR1 308
TP1
Q5
Q6
Q7
Q8
Q9
Q10
C3
R35
R37
R32
R73
R30 200
R48 10
R51 10
R45 1.0
R50 1K
R2
R23
AR2 356
R1 500K
Q3
C5
.001
Q11
Q12
C2
33/10V
K1 310125
K3 310125
K2 310125
R43 899.53K, .02%
U1 4016
U1 4016
U4 7416
U3 4016
Z1
IN916B

WARNING

HIGH VOLTAGE PRESENT

1	+7.4196	8	+9.3336
2	+7.4201	9	0.07155
3	+2.0093	10	–9.1338
4	+263.35	11	–8.5548
5	–263.75	12	–135.00
6	+134.50	13	–0.69025
7	+9.8629	14	+0.00007

Figure 5.31 - HV Buffer Test Point Locations

Table 5.23 - Digitizer PCB, Switching/Null Detector Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: 2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Assy. is to be mounted on Extender PCB, P/N 403951					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB NOTE: Ext Trig Scope at TP1, SID, Main PCB
	Buffer Op Amp – Input	R62	15	Figure 5.32	+10.1640V DC
	Buffer Op Amp + Input	R64	16	Figure 5.32	+10.1707V DC
	Buffer 1st Stage Source Bias	Q13 (Collector)	17	Figure 5.32	+1.39200V DC
	Buffer Current Generator Base Bias	CR19 (Anode)	18	Figure 5.32	–9.3282V DC
	Buffer Current Generator Emitter Bias	R10	19	Figure 5.32	–9.9560V DC
Remove input jumper. Connect input to DC standard set to +1.0000V DC	SID	J3-18	A	Figure 5.32	Waveform 1
	CPD	U4-8	B	Figure 5.32	Waveform 2
	$\overline{\text{Reset}}$	J3-21	C	Figure 5.32	Waveform 3
	AZ	J3-20	D	Figure 5.32	Waveform 4
	$\overline{\text{SIF}}$	J3-19	E	Figure 5.32	Waveform 5
	AZC	J3-23	F	Figure 5.32	Waveform 6
	– RD	J3-13	G	Figure 5.32	Waveform 7
	CID	U4-12	H	Figure 5.32	Waveform 8
	IND	U4-6	I	Figure 5.32	Waveform 9
	Reference Cap Switching, +	U3-3	J	Figure 5.32	Waveform 10
	Reference Cap Switching, –	U3-2	K	Figure 5.32	Waveform 11
	Measurement Cap Switching, +	U1-2	L	Figure 5.32	Waveform 12

Table 5.23 - Digitizer PCB, Switching/Null Detector Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Measurement Cap Switching, –	U1-10	M	Figure 5.32	Waveform 13
	Buffer Input Switching	U2-4	N	Figure 5.32	Waveform 14
	Buffer Output Switching	TP2	O	Figure 5.32	Waveform 15
	Integrator Output	TP3	P	Figure 5.32	Waveform 16
	Minus Feed-Forward Switching	R25	Q	Figure 5.32	Waveform 17
	Plus Feed-Forward Switching	R26	R	Figure 5.32	Waveform 18
	Null Detector Input (1st Stage)	CR13 (Cathode)	S	Figure 5.32	Waveform 19
	Null Detector Input (2nd Stage)	R51	T	Figure 5.32	Waveform 20
	Null Detector Output	J3-29	U	Figure 5.32	Waveform 21
Change input to –1.9900V DC	AZ	J3-20	D	Figure 5.32	Waveform 22
	AZC	J3-23	F	Figure 5.32	Waveform 23
	+ RD	J3-12	V	Figure 5.32	Waveform 24
	IND	U4-6	I	Figure 5.32	Waveform 25
	Reference Cap Switching, +	U3-3	J	Figure 5.32	Waveform 26
	Reference Cap Switching, –	U3-2	K	Figure 5.32	Waveform 27
	Measurement Cap Switching, +	U1-2	L	Figure 5.32	Waveform 28
	Measurement Cap Switching, –	U1-10	M	Figure 5.32	Waveform 29
	Buffer Input Switching	U2-4	N	Figure 5.32	Waveform 30

Table 5.23 - Digitizer PCB, Switching/Null Detector Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Buffer Output Switching	TP2	O	Figure 5.32	Waveform 31
	Integrator Output	TP3	P	Figure 5.32	Waveform 32
	Minus Feed-Forward Switching	R25	Q	Figure 5.32	Waveform 33
	Plus Feed-Forward Switching	R26	R	Figure 5.32	Waveform 34
	Null Detector Input (1st Stage)	CR13 (Cathode)	S	Figure 5.32	Waveform 35
	Null Detector Input (2nd Stage)	R51	T	Figure 5.32	Waveform 36
	Null Detector Output	J3-29	U	Figure 5.32	Waveform 37
Remove DC standard voltage from input Function: kHz Range: 2000 (manual) Input Terminals: J101 (Hi) and J102 (Lo) connected to a frequency (function) generator set to 1RMS volt @ 1 MHz	CPD	U4-8	B	Figure 5.32	Waveform 38
	$\overline{\text{Reset}}$	J3-21	C	Figure 5.32	Waveform 39
	AZ	J3-20	D	Figure 5.32	Waveform 40
	– RD	J3-13	G	Figure 5.32	Waveform 41
	+ RD	J3-12	V	Figure 5.32	Waveform 42
	IND	U4-6	I	Figure 5.32	Waveform 43
	Reference Cap Switching, +	U3-3	J	Figure 5.32	Waveform 44
	Reference Cap Switching, –	U3-2	K	Figure 5.32	Waveform 45
	Buffer Input Switching	U2-4	N	Figure 5.32	Waveform 46
	Buffer Output Switching	TP2	O	Figure 5.32	Waveform 47
	Integrator Output	TP3	P	Figure 5.32	Waveform 48
	Minus Feed-Forward Switching	R25	Q	Figure 5.32	Waveform 49
	Plus Feed-Forward Switching	R26	R	Figure 5.32	Waveform 50

Table 5.23 - Digitizer PCB, Switching/Null Detector Subassembly Performance Test continued

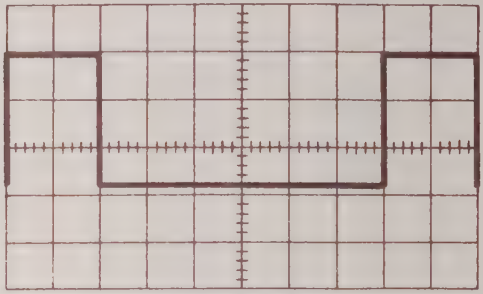
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	Null Detector Input (1st Stage)	CR13 (Cathode)	S	Figure 5.32	Waveform 51
	Null Detector Input (2nd Stage)	R51	T	Figure 5.32	Waveform 52
	Null Detector Output	J3-29	U	Figure 5.32	Waveform 53
Remove input cables and extender PCB					

Waveforms for Table 5.23

COUPLING: DC REF: TP4 (MECCA) MAIN PCB

1 (NO.) SID J3-18

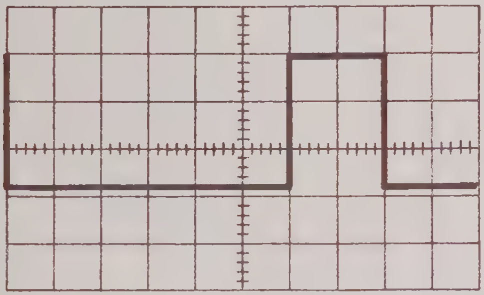
5.0 (V/DIV)



50 mS (S/DIV)

2 (NO.) CPD U4-8

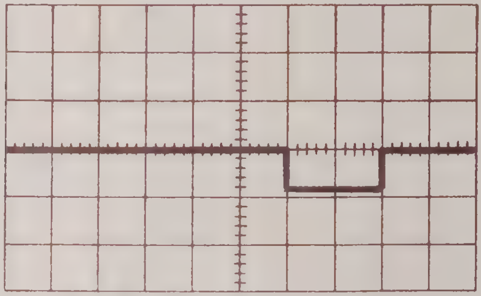
5.0 (V/DIV)



50 mS (S/DIV)

3 (NO.) $\overline{\text{RESET}}$ J3-21

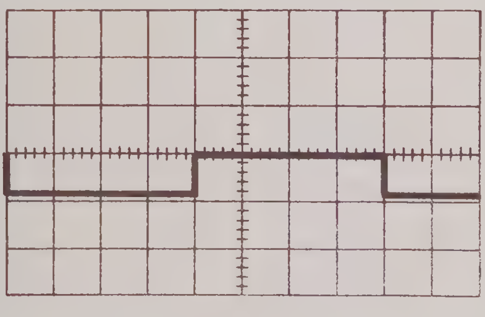
5.0 (V/DIV)



50 mS (S/DIV)

4 (NO.) AZ J3-20

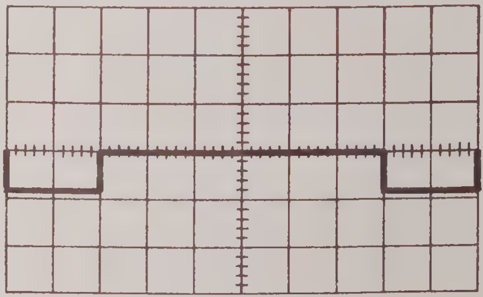
5.0 (V/DIV)



50 mS (S/DIV)

5 (NO.) $\overline{\text{SIF}}$ J3-19

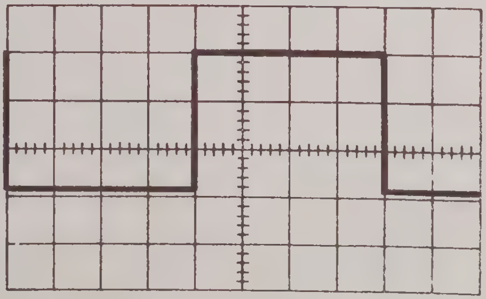
5.0 (V/DIV)



50 mS (S/DIV)

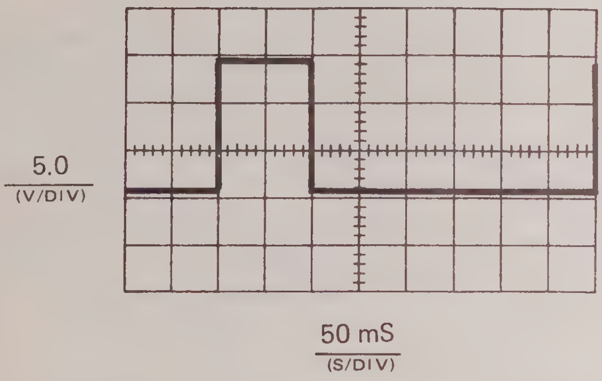
6 (NO.) AZC J3-23

5.0 (V/DIV)

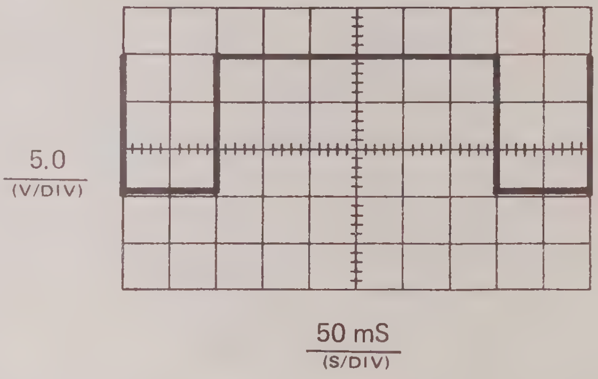


50 mS (S/DIV)

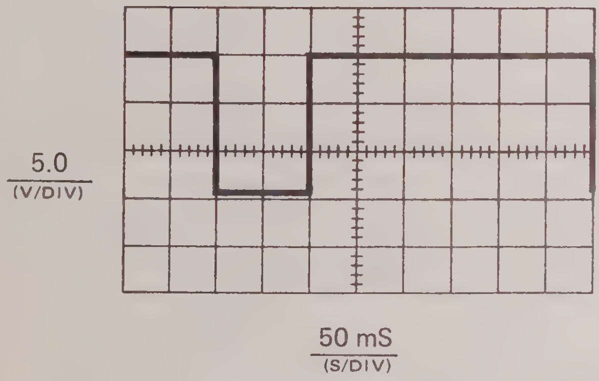
7 (NO.) — RD
J3-13



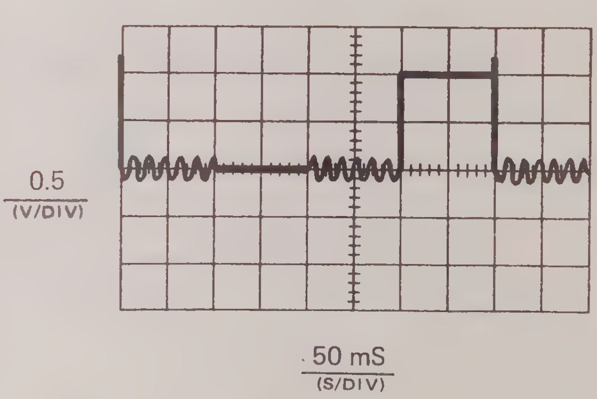
8 (NO.) CID
U4-12



9 (NO.) IND
U4-6



10 (NO.) REFERENCE CAP SWITCHING, +
U3-3



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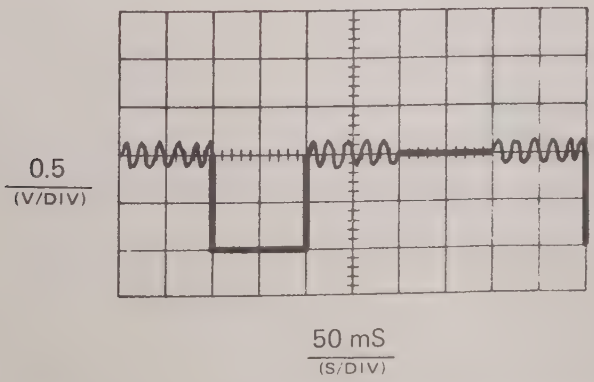
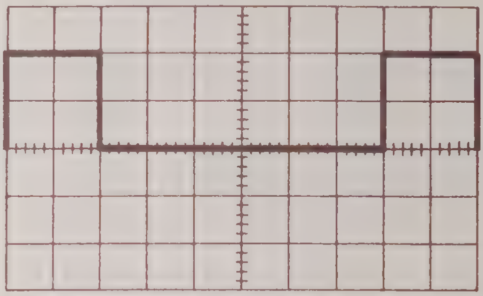
U3-2



Waveforms for Table 5.23 continued

12
(NO.)

MEASUREMENT CAP SWITCHING, +
U1-2



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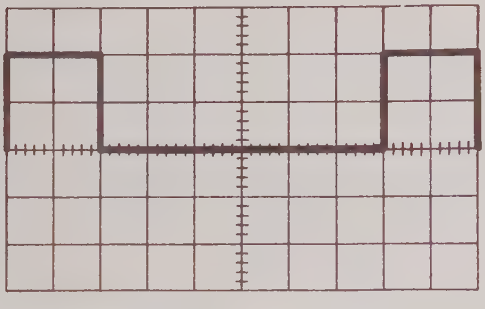
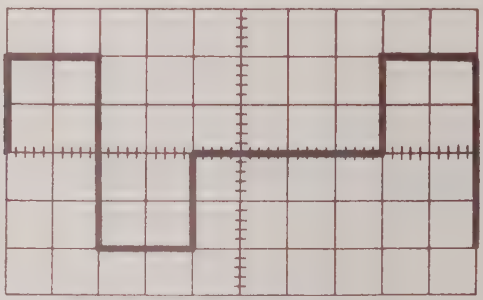
MEASUREMENT CAP SWITCHING, –
U1-10



14
(NO.)

BUFFER INPUT SWITCHING
U2-4



15
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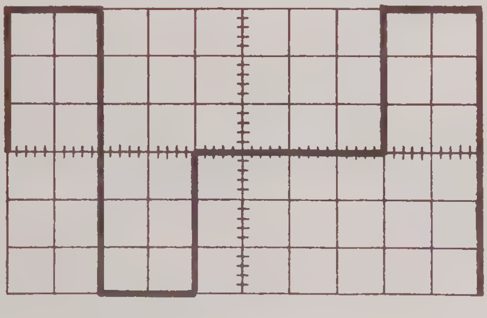
BUFFER OUTPUT SWITCHING
TP2



16
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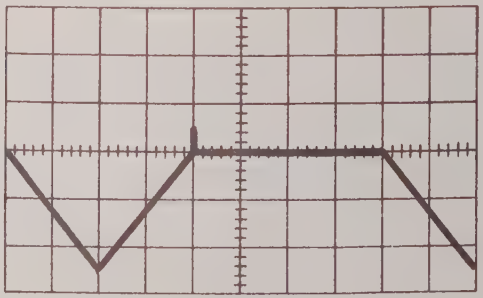
INTEGRATOR OUTPUT
TP3



17
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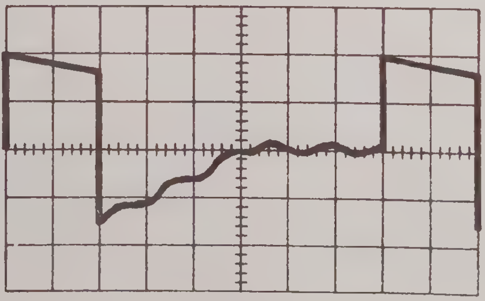
MINUS FEED-FORWARD SWITCHING
R25



Waveforms for Table 5.23 continued

18
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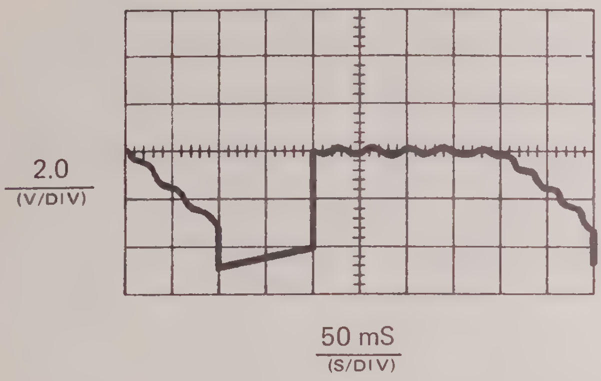
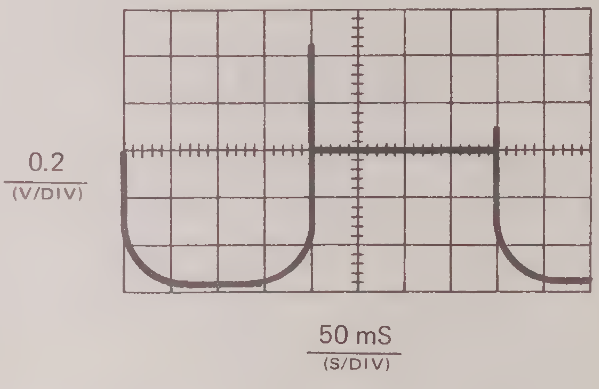
PLUS FEED-FORWARD SWITCHING
R26



19
(NO.)

NULL DETECTOR INPUT (1ST STAGE)
CR13 (CATHODE)



20
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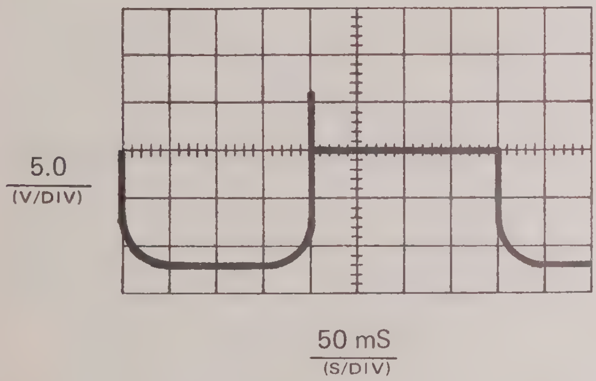
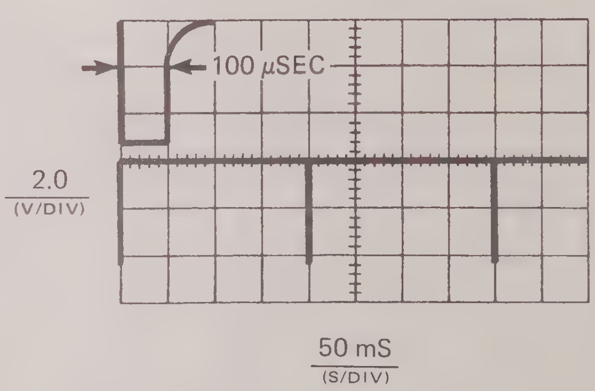
NULL DETECTOR INPUT (2ND STAGE)
R51



21
(NO.)

NULL DETECTOR OUTPUT
J3-24



22
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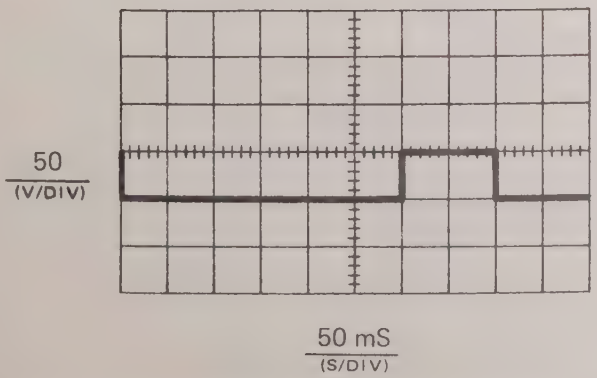
AZ
J3-20



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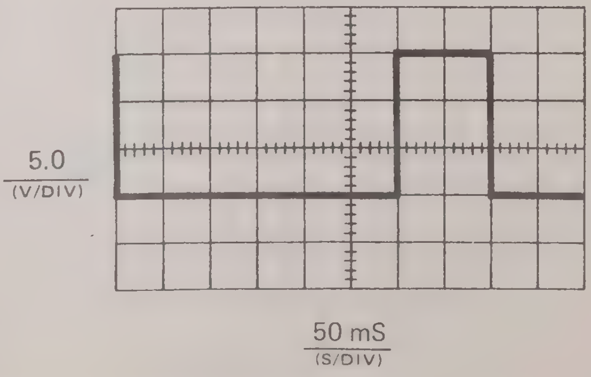
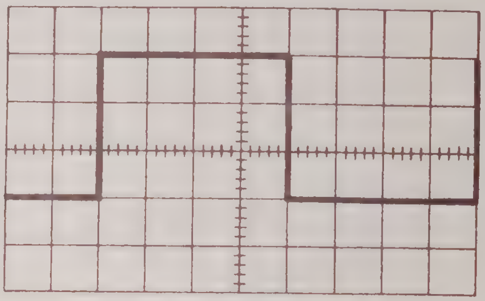
AZC
J3-23



Waveforms for Table 5.23 continued

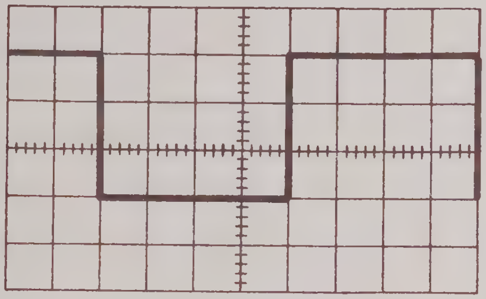
24
(NO.)

+ RD
J3-12



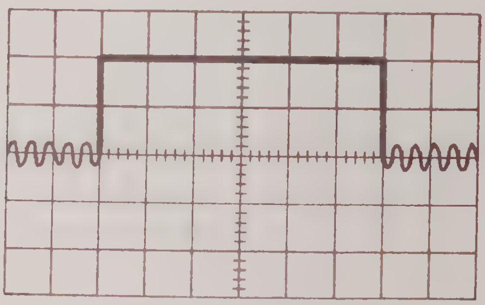
25
(NO.)

IND
U4-6



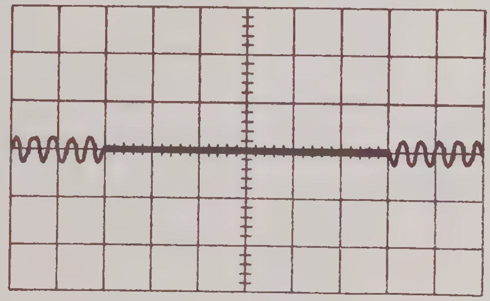
26
(NO.)

REFERENCE CAP SWITCHING, +
U3-3



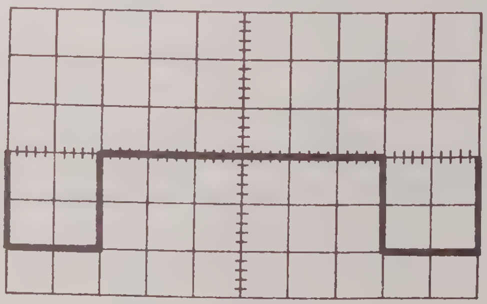
27
(NO.)

REFERENCE SWITCHING CAP, –
U3-2



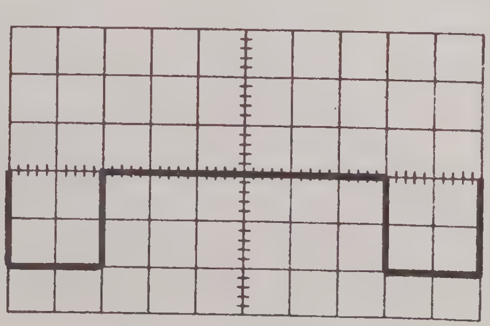
28
(NO.)

MEASUREMENT CAP SWITCHING, +
U1-2



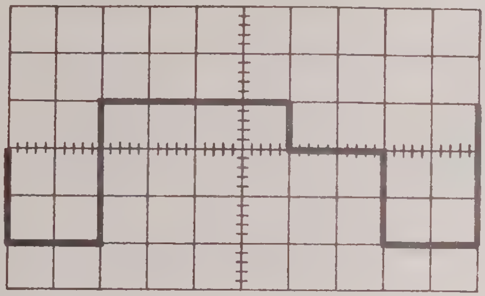
29
(NO.)

MEASUREMENT CAP SWITCHING, –
U1-10

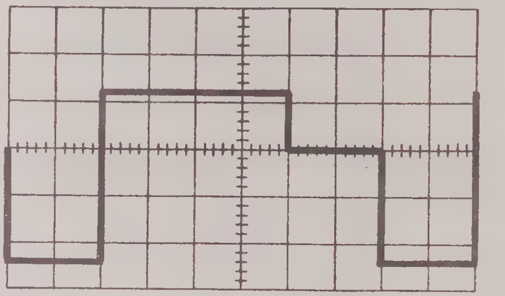


Waveforms for Table 5.23 continued

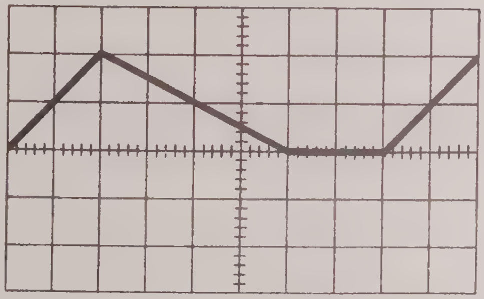
30 (NO.) BUFFER INPUT SWITCHING
U2-4



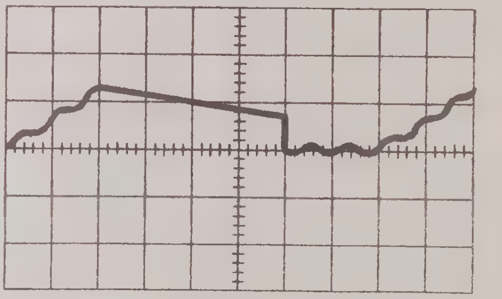
31 (NO.) BUFFER OUTPUT SWITCHING
TP2



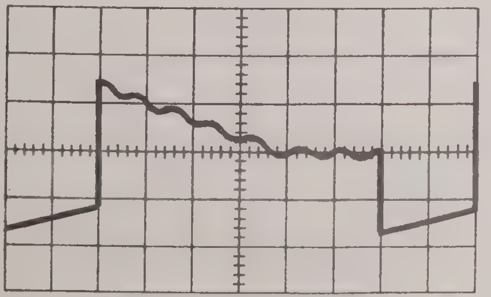
32 (NO.) INTEGRATOR OUTPUT
TP3



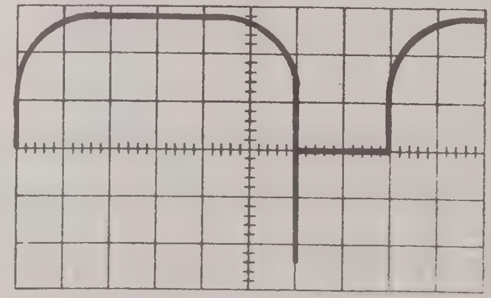
33 (NO.) MINUS FEED-FORWARD SWITCHING
R25



34 (NO.) PLUS FEED-FORWARD SWITCHING
R26

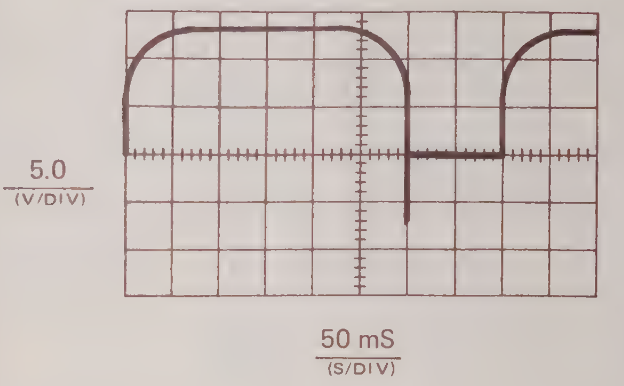


35 (NO.) NULL DETECTOR INPUT (1ST STAGE)
CR13

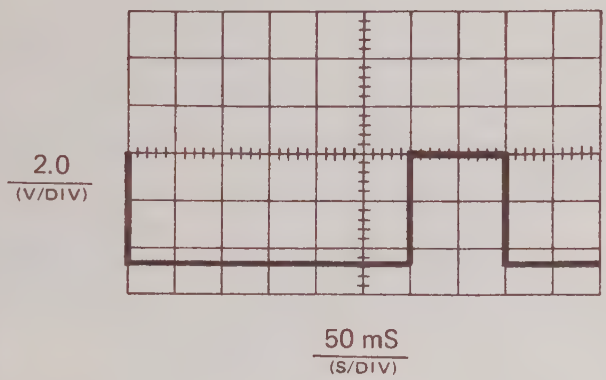


Waveforms for Table 5.23 continued

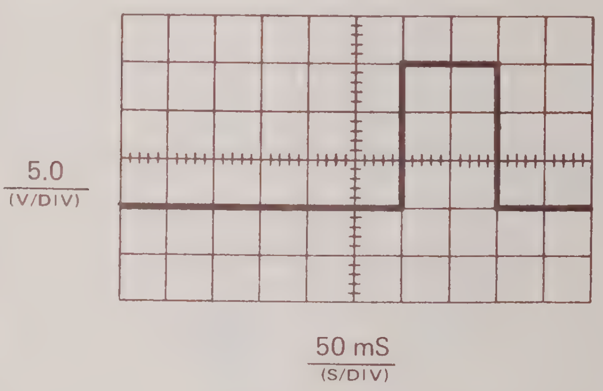
36
(NO.)
NULL DETECTOR INPUT (2ND STAGE)
R51



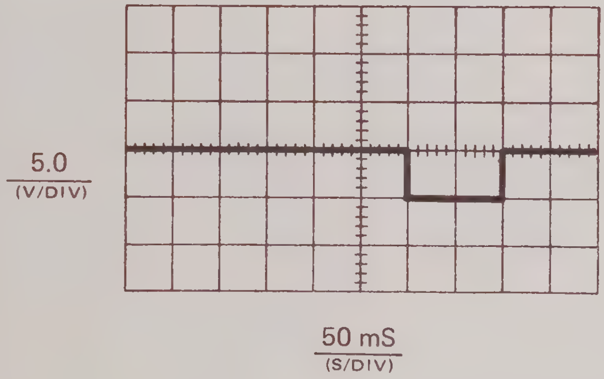
37
(NO.)
NULL DETECTOR OUTPUT
J3-29



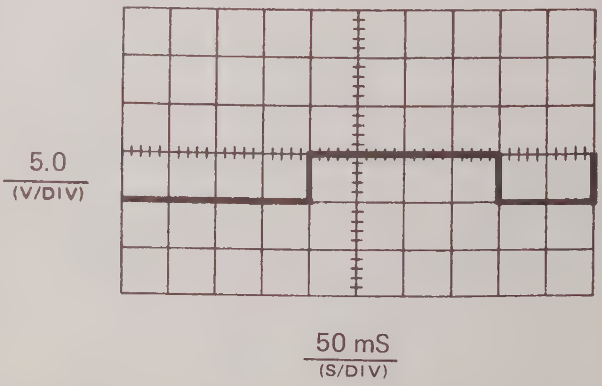
38
(NO.)
CPD
U4-8



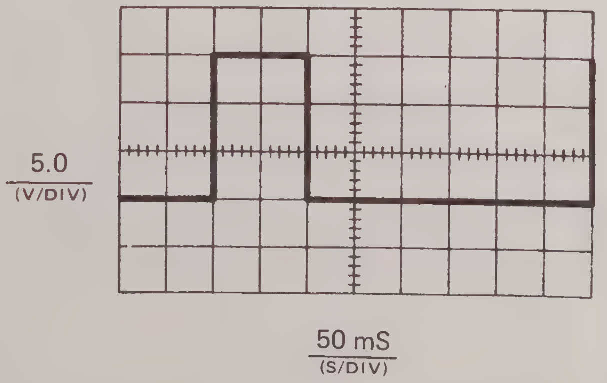
39
(NO.)
$\overline{\text{RESET}}$
J3-21



40
(NO.)
AZ
J3-20



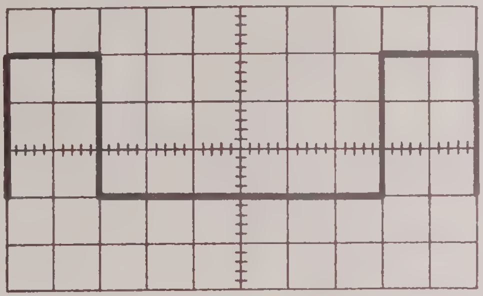
41
(NO.)
– RD
J3-13



Waveforms for Table 5.23 continued

42 (NO.)

+ RD
J3-12

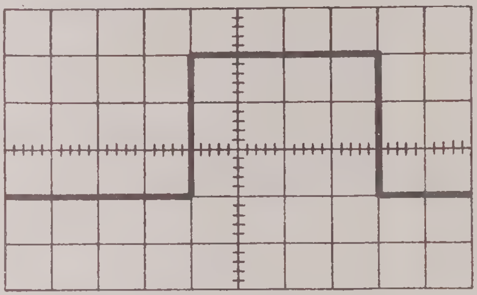


5.0 (V/DIV)

50 mS (S/DIV)

43 (NO.)

IND
U4-6

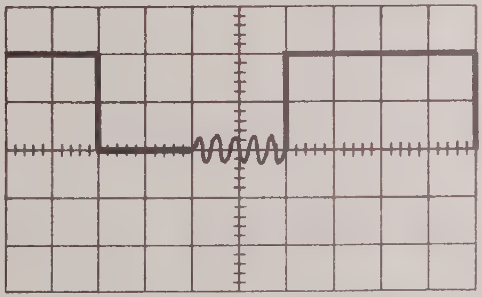


(V/DIV)

50 mS (S/DIV)

44 (NO.)

REFERENCE CAP SWITCHING, +
U3-3

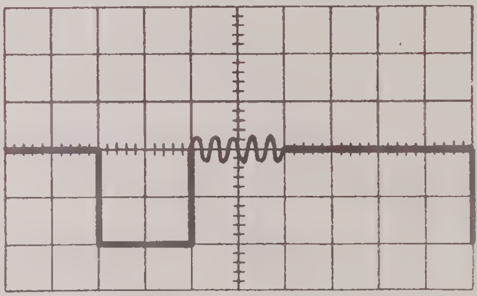


0.5 (V/DIV)

50 mS (S/DIV)

45 (NO.)

REFERENCE CAP SWITCHING, –
U3-2

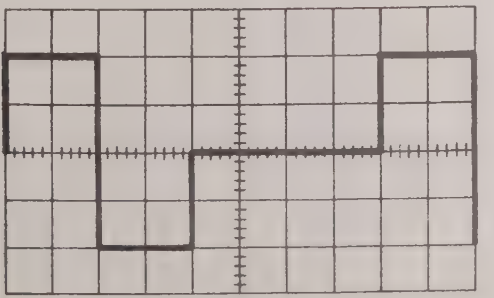


0.5 (V/DIV)

50 mS (S/DIV)

46 (NO.)

BUFFER INPUT SWITCHING
U2-4

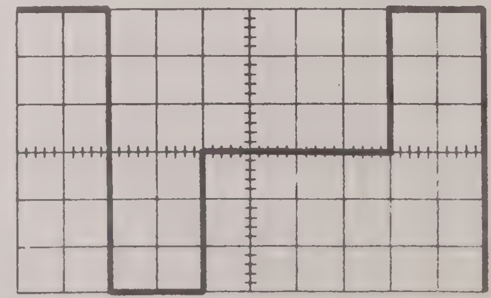


0.5 (V/DIV)

50 mS (S/DIV)

47 (NO.)

BUFFER OUTPUT SWITCHING
TP2



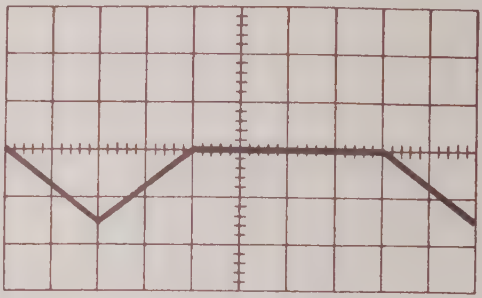
2.0 (V/DIV)

50 mS (S/DIV)

Waveforms for Table 5.23 continued

48
(NO.)

INTEGRATOR OUTPUT
TP3

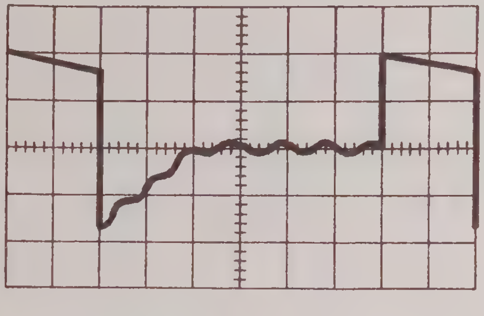


2.0
(V/DIV)

50 mS
(S/DIV)

49
(NO.)

MINUS FEED-FORWARD SWITCHING
R25

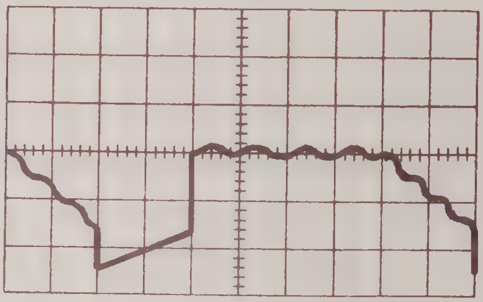


2.0
(V/DIV)

50 mS
(S/DIV)

50
(NO.)

PLUS FEED-FORWARD SWITCHING
R26

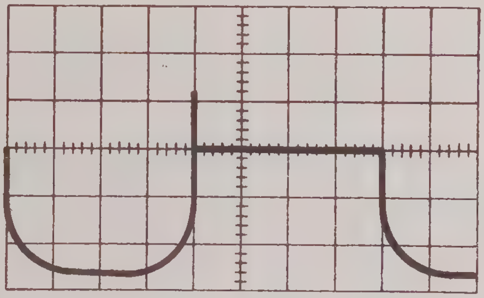


2.0
(V/DIV)

50 mS
(S/DIV)

51
(NO.)

NULL DETECTOR INPUT (1ST STAGE)
CR13 (CATHODE)

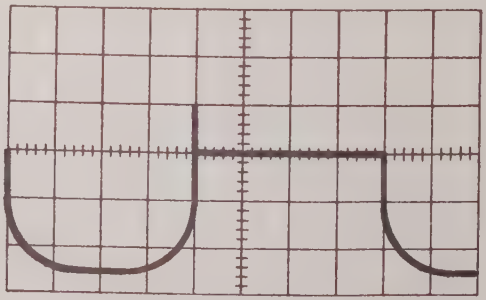


0.2
(V/DIV)

50 mS
(S/DIV)

52
(NO.)

NULL DETECTOR INPUT (2ND STAGE)
R51

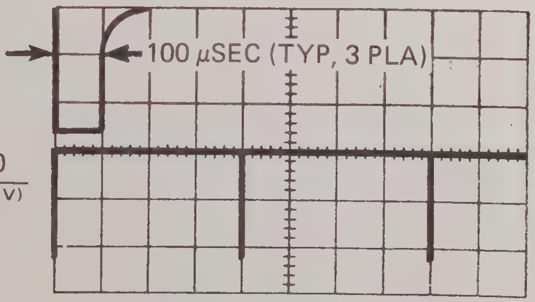


5.0
(V/DIV)

50 mS
(S/DIV)

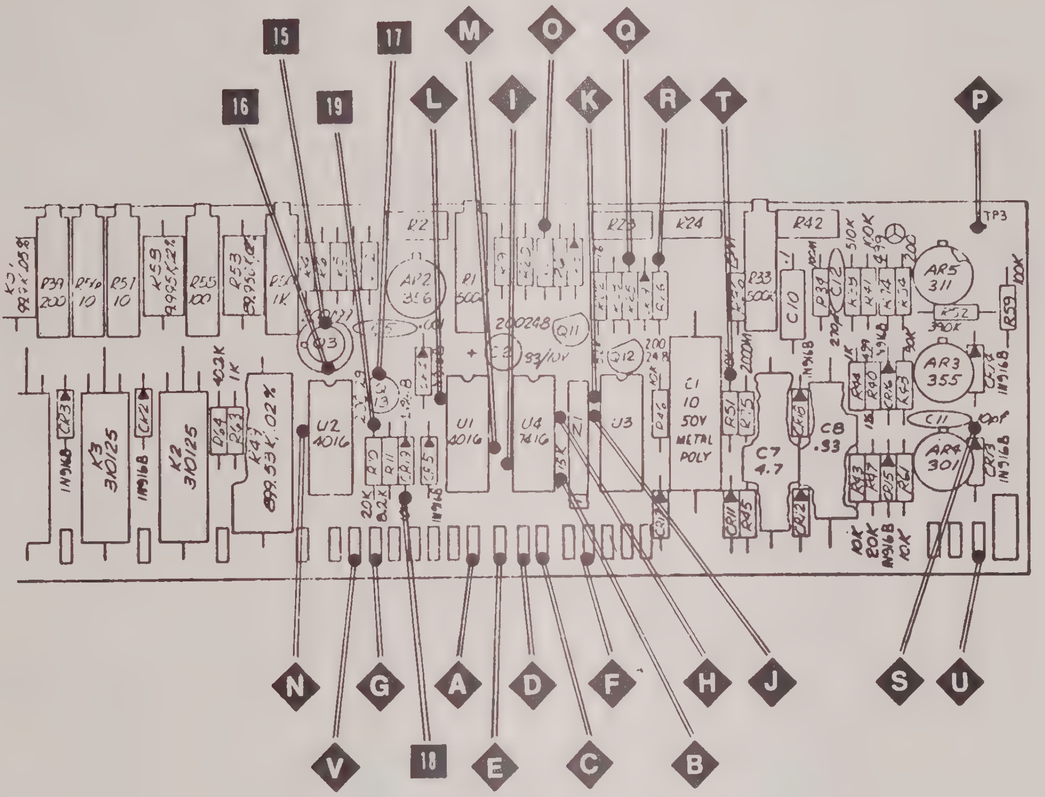
53
(NO.)

NULL DETECTOR OUTPUT



2.0
(V/DIV)

50 mS
(S/DIV)


15
17
M
O
Q
16
19
L
I
K
R
T
P
TP3
R2
R23
R24
R42
AR2
356
R1
500K
R33
500K
C10
AR5
311
R39
200
R40
10
R51
10
R59
R55
100
R53
R50
1K
Q3
Q11
Q12
C2
33/10V
AR3
355
U2
4016
U1
4016
U4
741C
U3
Z1
C1
10
50V
METAL
POLY
C7
4.7
C8
.33
C11
AR4
301
K3
310125
K2
310125
K4
999.53K, .02%
CR3
CR2
1N916B
20K
8.2K
10K
20K
10K
100K
390K
N
G
A
D
F
H
J
S
U
V
18
E
C
B

WARNING

HIGH VOLTAGE PRESENT

@ J3 pin 4 (+300V DC) and 5 (−300V DC)

15	+10.1640
16	+10.1707
17	+1.3920
18	9.3282
19	−9.9560

Figure 5.32 - Switching/Integrator/Null Detector Test Point Locations

Table 5.24 - AC (Averaging) Converter PCB, Subassembly Performance Test

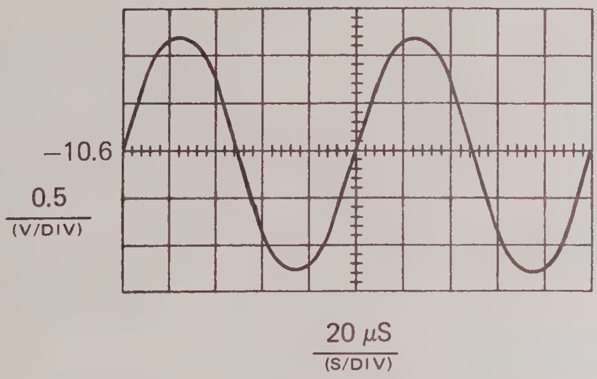
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: 2 (manual) Filter: IN (automatically selected) Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Shield must be removed and assembly placed on extender PCB, 403950 for test					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	Scaling Op Amp – Input	R3	1	Figure 5.33	+1.42425V DC
	Scaling Op Amp + Input	R4	2	Figure 5.33	+1.42408V DC
	1st Stage Source Load Bias	R15	3	Figure 5.33	–14.506V DC
	Scaling Op Amp Output	AR1-6	4	Figure 5.33	–10.677V DC
	Rectifier Output Driver Bias	CR6 (Anode)	5	Figure 5.33	+13.260V DC
	Rectifier Output Driver Bias	CR7 (Cathode)	6	Figure 5.33	–12.910V DC
	PNP Output Driver Emitter Bias	R7	7	Figure 5.33	+13.896V DC
	NPN Output Driver Emitter Bias	R8	8	Figure 5.33	–13.500V DC
	Rectifier Output	CR8 (Cathode)	9	Figure 5.33	0V (.3V p-p Switching Noise)
Remove jumper. Connect input to a signal (function) generator set to 1.9V RMS @ 10 kHz	Scaling Op Amp Output	AR1-6	A	Figure 5.33	Waveform 1
	Scaling Rectifier Output	CR8 (Cathode)	B	Figure 5.33	Waveform 2
	Minus Rectified Output	CR8 (Anode)	C	Figure 5.33	Waveform 3
	Plus Rectified Output	CR9 (Cathode)	D	Figure 5.33	Waveform 4
	Plus Output	J4-11	E	Figure 5.33	Waveform 5 (Note ripple)
	Minus Output	J4-10	F	Figure 5.33	Waveform 6 (Note ripple)
Remove voltage, cables, extender PCB, and replace shields					

INPUT
1.9V RMS @ 10 kHz/2 RNG

Waveforms for Table 5.24

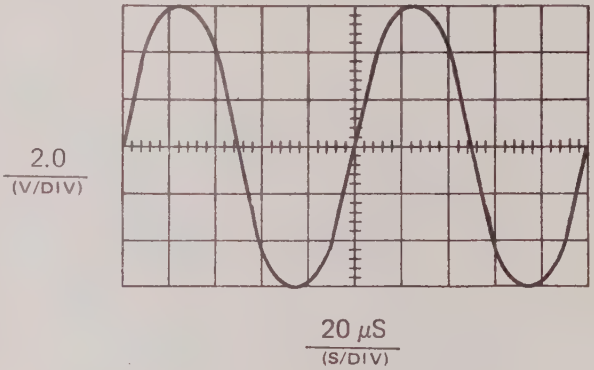
REF: TP4 (MECCA) MAIN PCB
COUPLING: DC, UNLESS NOTED

1 (NO.) SCALING OP AMP OUTPUT
AR1-6

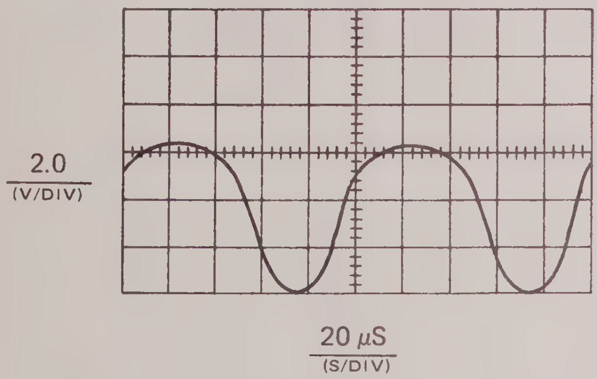


AC COUPLED

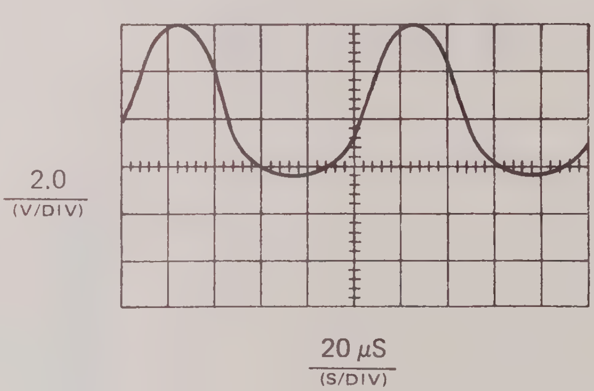
2 (NO.) SCALING RECTIFIER OUTPUT
CR8 (CATHODE)



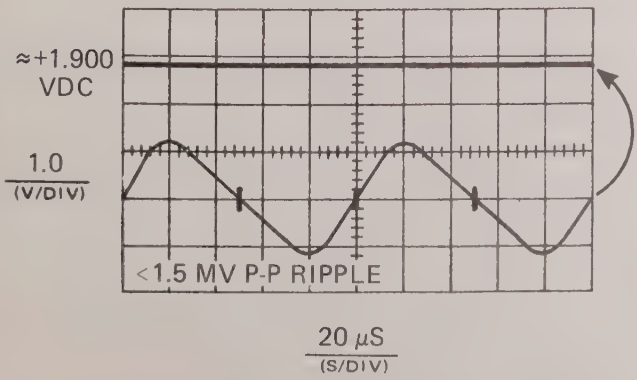
3 (NO.) MINUS RECTIFIED OUTPUT
CR8 (ANODE)



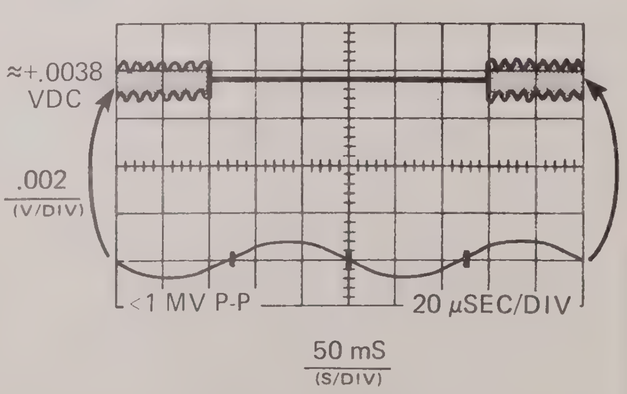
4 (NO.) PLUS RECTIFIED OUTPUT
CR9 (CATHODE)



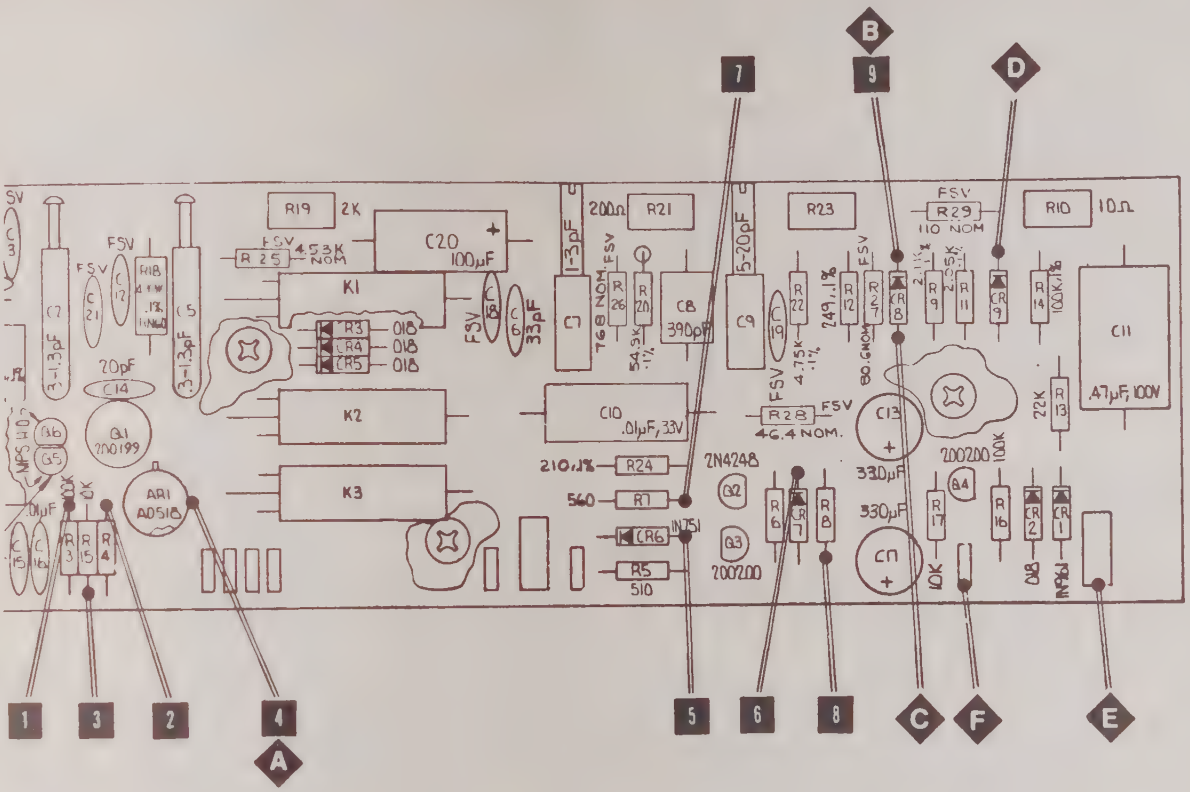
5 (NO.) PLUS OUTPUT
J4-11



6 (NO.) MINUS OUTPUT
J4-10



EXT TRIG; TP1 (SID) MAIN PCB


B
9
7
D
R19
2K
C20
100μF
R25
4.53K NOM
FSV
K1
R3
CR4
CR5
018
K2
K3
C14
20pF
Q1
2N0199
AR1
AD518
Q5
Q6
C7
3-1.3pF
C5
3-1.3pF
R18
C21
C17
C18
C16
33pF
1-3pF
200Ω
R21
C7
R26
768 NOM
R20
54.9K .1%
C8
390pF
5-20pF
C9
C19
C10
.01μF, 33V
R24
210 .1%
R7
560
CR6
1N751
R5
510
Q2
2N4248
Q3
200200
R23
R22
4.75K .1%
249 .1%
R12
R27
80.6NOM
CR8
R9
R11
R28
46.4 NOM.
C13
330μF
C11
330μF
R29
110 NOM
R10
10Ω
CR9
R14
100K .1%
C11
.47μF, 100V
R13
22K
Q4
200200
R17
10K
R16
100K
CR2
CR1
R3
R15
R4
C15
C16
.01μF
1
3
2
4
A
5
6
8
C
F
E

1	+1.42425
2	+1.42408
3	−14.506
4	−10.677
5	+13.260
6	−12.910
7	+13.896
8	−13.500
9	0V (.3 mV P-P Switching Noise)

Figure 5.33 - Averaging AC Converter Test Point Locations

Table 5.25 - AC (True RMS) Converter PCB Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: ACV Range: 2 (manual) Filter: IN (automatically selected) Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper Converter shields must be removed and assembly placed on extender PCB, 403950, for test					NOTE: All measurements are referenced to TP4 (MECCA) Main PCB
	+ Regulated Supply	CR3 (Cathode)	1	Figure 5.34	+13.6715V DC
	– Regulated Supply	CR4 (Anode)	2	Figure 5.34	–13.8673V DC
	Scaling Op Amp – Input	R7	3	Figure 5.34	+0.00125V DC
	Scaling Op Amp Output	TP2	4	Figure 5.34	–0.13692V DC
	Rectifier Driver Bias Level	CR12 (Anode)	5	Figure 5.34	+8.505V DC
	Rectifier Driver Bias Level	CR11 (Anode)	6	Figure 5.34	–9.325V DC
	Rectifier Op Amp Output	R29	7	Figure 5.34	+2.24V DC
	Rectifier Amp Output	TP5	8	Figure 5.34	–0.480V DC
	Log Driving Amp Bias (Dynamic)	R25	9	Figure 5.34	+3.5460V DC
	Log Driving Amp Bias Level	CR10 (Cathode)	10	Figure 5.34	+2.9635V DC
	Log Driving Amp Output	R37	11	Figure 5.34	+1.3642V DC
	Log Driving Amp 1st Stage Emitter Bias	R33	12	Figure 5.34	–0.6315V DC
	Log Driving Amp Base Bias	R36	13	Figure 5.34	+0.1120V DC
	Log Driving Amp Output	TP3	14	Figure 5.34	–0.8200V DC
	Output Op Amp – Input	R39	15	Figure 5.34	–0.0027V DC
	Output Op Amp Output	R46	16	Figure 5.34	+0.0114V DC

Table 5.25 - AC (True RMS) Converter PCB Subassembly Performance Test continued

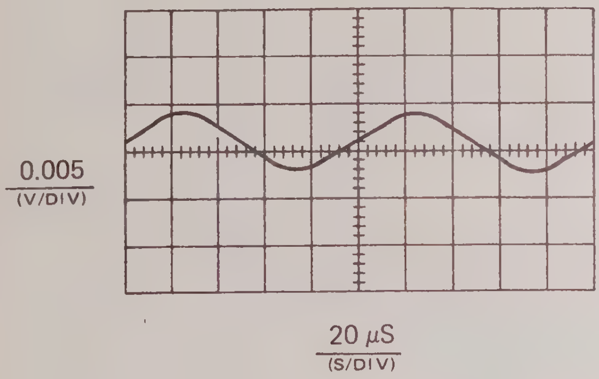
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Remove jumper. Connect input to an AC voltage standard set to 1.9V RMS @ 10 kHz	Scaling Op Amp – Input	R7	A	Figure 5.34	Waveform 1
	Scaling Op Amp Output	TP2	B	Figure 5.34	Waveform 2
	Rectifier Amp Output	TP5	C	Figure 5.34	Waveform 3
	Minus Rectified Output	CR8 (Anode)	D	Figure 5.34	Waveform 4
	Plus Rectified Output	CR9 (Cathode)	E	Figure 5.34	Waveform 5
	Log Driving Amp Output	TP3	F	Figure 5.34	Waveform 6
	Output Op Amp Output	R46	G	Figure 5.34	Waveform 7
	Attenuated/ Filtered Output	J4-11	H	Figure 5.34	Waveform 8
Remove test cables, extender, and replace shields					

Waveforms for Table 5.25

COUPLING: DC
REF: TP4 (MECCA) MAIN PCB

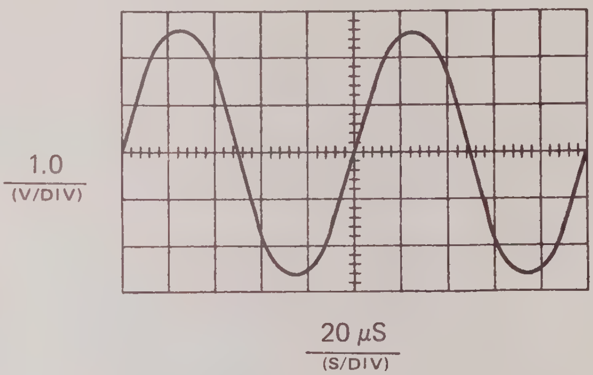
1
(NO.)

SCALING OP AMP – INPUT
R7



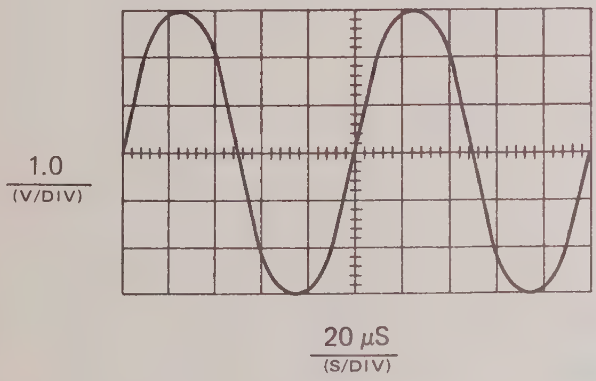
2
(NO.)

SCALING OP AMP OUTPUT
TP2



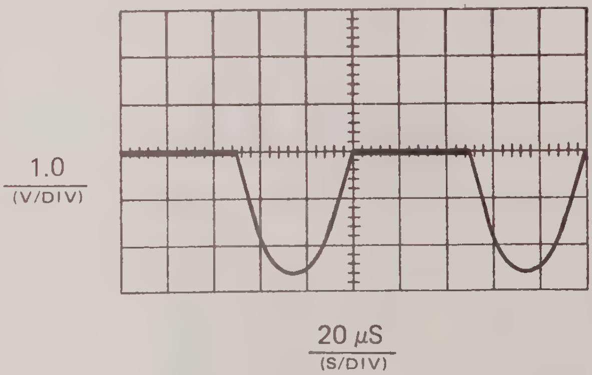
3
(NO.)

RECTIFIER AMP OUTPUT
TP5



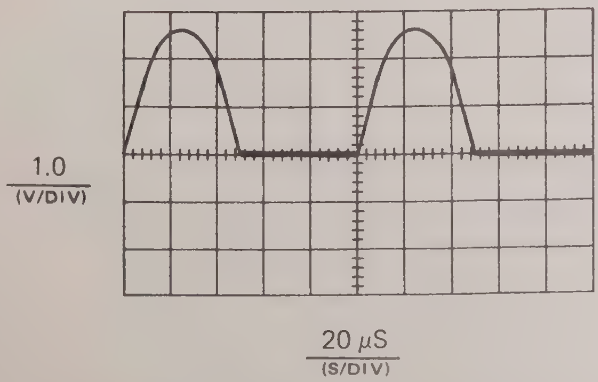
4
(NO.)

MINUS RECTIFIED OUTPUT
CR8 (ANODE)



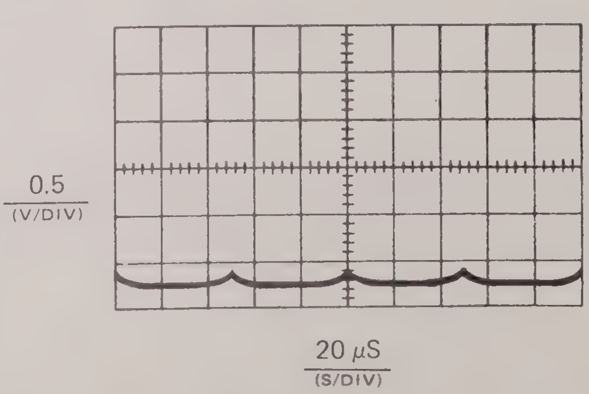
5
(NO.)

PLUS RECTIFIED OUTPUT
CR9 (CATHODE)

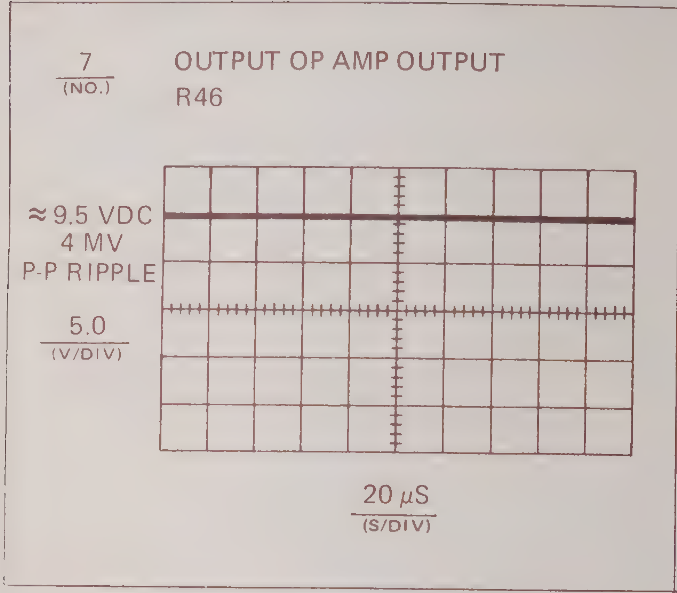


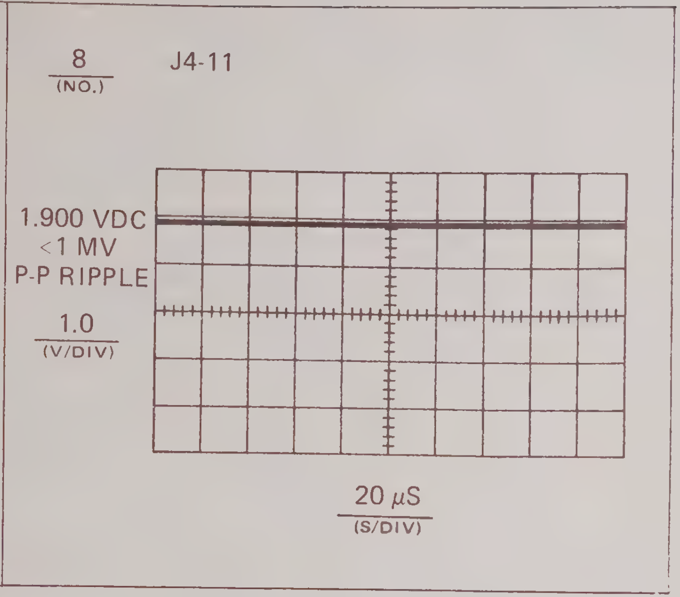
6
(NO.)

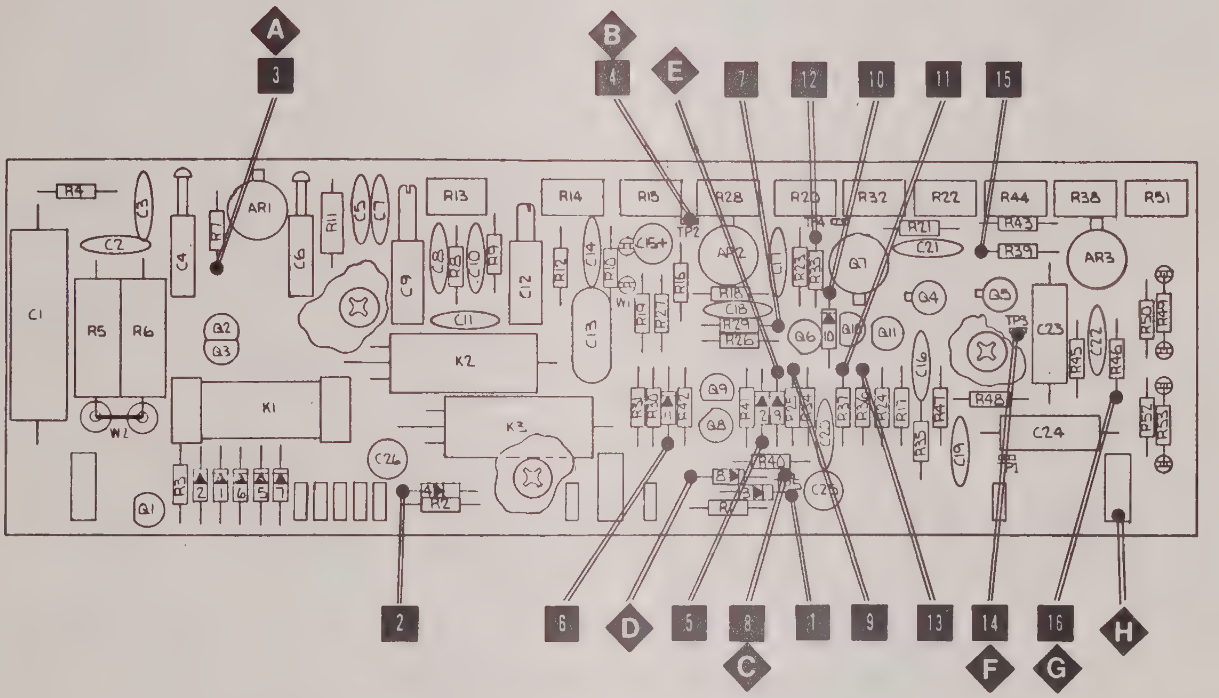
LOG DRIVING AMP OUTPUT
TP3



Waveforms for Table 5.25 continued






A
3
B
4
E
7
12
10
11
15
R4
C3
AR1
R7
C2
C4
C6
R11
C5
C7
R13
C9
C8
R8
C10
R9
C12
C11
R14
R12
C14
R10
C15+
TP2
W1
C13
R19
R27
R16
R15
R28
AR2
R18
C18
R29
R26
C17
R20
R23
R33
TP4
Q7
Q6
Q10
Q11
R32
R21
C21
Q4
R22
R44
R43
R39
Q5
R38
AR3
R51
TP3
C23
C16
R45
C22
R46
R50
R49
C1
R5
R6
Q2
Q3
K2
K1
W2
K3
Q9
Q8
R48
R41
R35
C19
C24
R52
R53
R40
C25
C26
R3
R2
R1
Q1
2
6
D
5
8
C
1
9
13
14
F
16
G
H

1	+13.6715
2	–13.8673
3	+0.00125
4	–0.13692
5	+8.505
6	–9.325
7	+2.24
8	–0.480
9	+3.5460
10	+2.9635
11	+1.3642
12	–0.6315
13	+0.1120
14	–0.8200
15	–0.0027
16	+0.0114

Figure 5.34 - True RMS AC Converter Test Point Locations

Table 5.26 - Data Output Subassembly Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Function: DCV Range: .2 (manual) Filter: OUT Input Terminals: J101 (Hi) and J102 (Lo) connected with a copper jumper					NOTE: All measurements are referenced to TP3 (DIG COM) Main PCB NOTE: For test purposes, the data output common can be tied to digital common NOTE: Ext Trig Scope (+) @ TP1 (SID) Main PCB
	Isolated Bridge Rectifier Output	C2 "+"	1	Figure 5.35	+9.650V DC Ripple: 1.4V p-p
	Isolated Regulator Output	R9	2	Figure 5.35	+5.05V DC Ripple: <4 mV p-p
Remove jumper; Connect input to DC voltage standard set to +1.9900V DC	O/S-B F/F Output	U3-5	A	Figure 5.35	Waveform 1
	Synchronizer Output	U3-9	B	Figure 5.35	Waveform 2
	MUX Clock Gate Enable	U3-13	C	Figure 5.35	Waveform 3
	Gated MUX Clock	U4-14	D	Figure 5.35	Waveform 4
	Counter Q1 Output	U4-1	E	Figure 5.35	Waveform 5
	Counter Q4 Output	U4-8	F	Figure 5.35	Waveform 6
	Counter Q2 Output	U4-9	G	Figure 5.35	Waveform 7
	Multiplexer "A" Select Drive	U2-10	H	Figure 5.35	Waveform 8
	Multiplexer "B" Select Drive	U2-13	I	Figure 5.35	Waveform 9
	$\overline{\text{Serial Strobe}}$	U1-12	J	Figure 5.35	Waveform 10
	1 Bit Serial Output (1)	U7-6	K	Figure 5.35	Waveform 11

Table 5.26 - Data Output Subassembly Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
	2 Bit Serial Output (2)	U7-4	L	Figure 5.35	Waveform 12
	3 Bit Serial Output (4)	U7-2	M	Figure 5.35	Waveform 13
	4 Bit Serial Output (8)	U7-12	N	Figure 5.35	Waveform 14
	Serial Strobe Output	U8-6	O	Figure 5.35	Waveform 15
	Serial Strobe Output	U7-10	P	Figure 5.35	Waveform 16
	$\overline{\text{Inhibit Parallel Data Output}}$	U7-8	Q	Figure 5.35	Waveform 17
	Parallel Data Valid	U8-2	R	Figure 5.35	Waveform 18
	Inhibit Parallel Data Output	U8-3	S	Figure 5.35	Waveform 19

Verify parallel function code below:

	FUNCTION CODE		
	FC1	FC2	BCD WEIGHT
DCV	1	1	3
ACV	0	1	2
KΩ	1	0	1
kHz	0	0	0
	14	P	
	J203 PIN No.		

Verify parallel range code below:

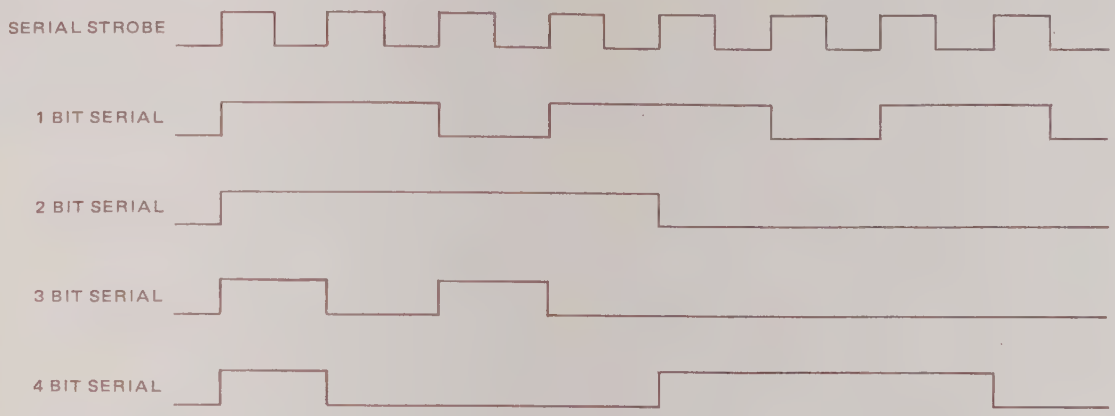
	RANGE CODE			
	RC1	RC2	RC3	BCD WEIGHT
.2	0	1	0	2
2	1	1	0	3
20	0	0	1	4
200	1	0	1	5
2000	0	1	1	6
20,000	1	1	1	7
	15	R	7	
	J203 PIN No.			

Verify parallel numerical codes below:

UNITS	J203 PIN	TENS	J203 PIN	HUNDREDS	J203 PIN	THOUSANDS	J203 PIN	TEN-THOUSANDS	J203 PIN	HUNDRED-THOUSANDS	J203 PIN
1	16	10	17	100	18	1000	19	10,000	22	100,000	21
2	5	20	T	200	U	2000	V	20,000	Y	O/L	X
4	8	40	9	400	10	4000	11	40,000	12		
8	E	80	F	800	H	8000	J	80,000	L		

Table 5.26 - Data Output Subassembly Performance Test continued

To verify the serial quantity of the data output, the 1, 2, 3, and 4 bit serial outputs should be synchronized with serial strobe. Example: +1.98936V DC



	WORD							
	1	2	3	4	5	6	7	8
LINE 1	FC1	RC1	1	10	100	1K	10K	100K
LINE 2	FC2	RC2	2	20	200	2K	20K	O/L
LINE 4	POL	RC3	4	40	400	4K	40K	LOW
LINE 8	HIGH	LOW	8	80	800	8K	80K	LOW

DCV — 3 — FUNCTION/POL
2 — 3 — RANGE
6 — UNITS
3 — TENS
9 — HUNDREDS
8 — THOUSANDS
9 — TEN-THOUSANDS
1 — HUNDRED-THOUSANDS

Connect a jumper from data output common, J203-4 to Hold, J203-3 and verify that the DMM does not take any readings.

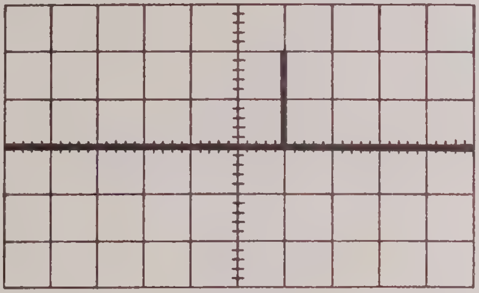
Remove test cables, scopes and meters.

+1.99 V_{IN}/2. RNG
DCV R/O +1.98936

Waveforms for Table 5.26

1
(NO.)

$\overline{\text{ONE-SHOT "B"}}$ F/F OUTPUT
U3-5

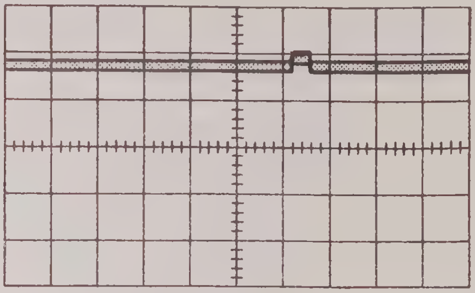


2.0
(V/DIV)

50 mS
(S/DIV)

2
(NO.)

SYNCHRONIZER OUTPUT DRIVE
U3-9

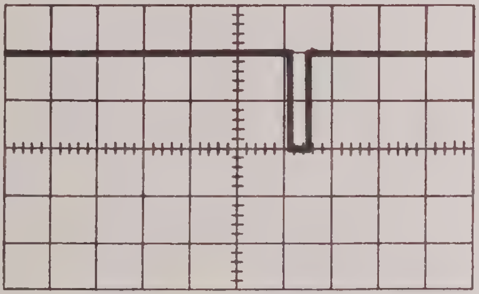


.050
(V/DIV)

50 mS
(S/DIV)

3
(NO.)

MUX CLOCK GATE ENABLE
U3-13

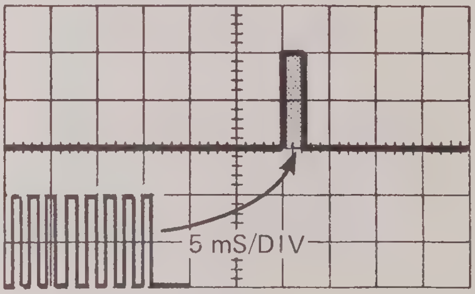


2.0
(V/DIV)

50 mS
(S/DIV)

4
(NO.)

GATED MUX CLOCK
U4-14

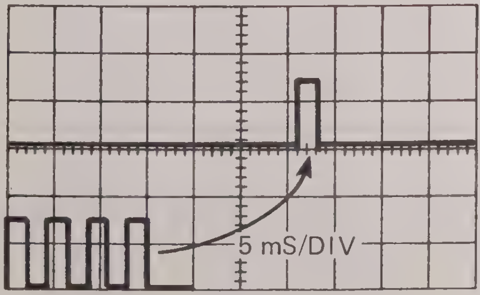


2.0
(V/DIV)

50 mS
(S/DIV)

5
(NO.)

COUNTER OUTPUT, Q1
U4-1

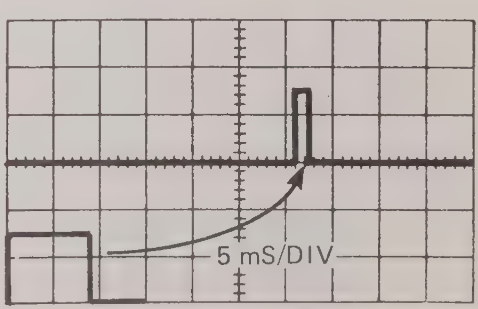


2.0
(V/DIV)

50 mS
(S/DIV)

6
(NO.)

COUNTER OUTPUT, Q4
U4-8



2.0
(V/DIV)

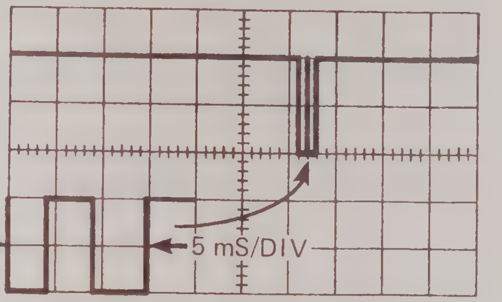
50 mS
(S/DIV)

Waveforms for Table 5.26 continued

7
(NO.)

COUNTER OUTPUT, Q2
U4-9

2.0
(V/DIV)

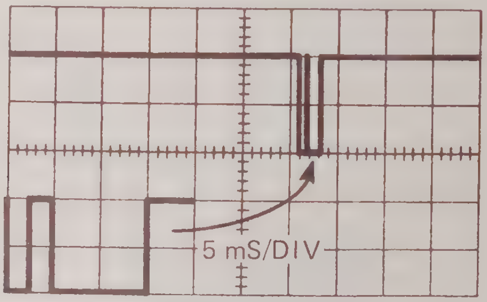


50 mS
(S/DIV)

8
(NO.)

MULTIPLEXER "A" SELECT DRIVE
U2-10

2.0
(V/DIV)

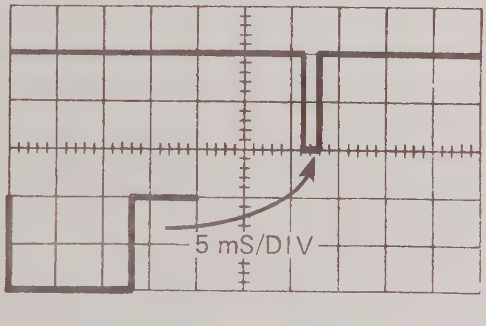


50 mS
(S/DIV)

9
(NO.)

MULTIPLEXER "B" SELECT DRIVE
U2-13

2.0
(V/DIV)

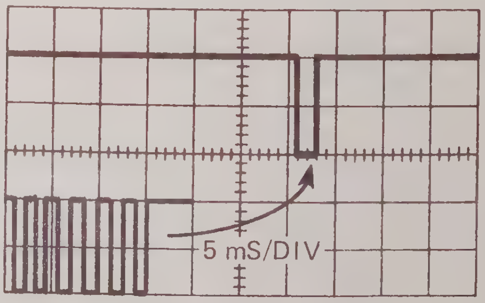


50 mS
(S/DIV)

10
(NO.)

$\overline{\text{SERIAL STROBE}}$
U1-12

2.0
(V/DIV)

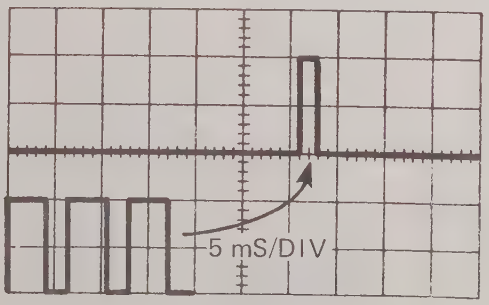


50 mS
(S/DIV)

11
(NO.)

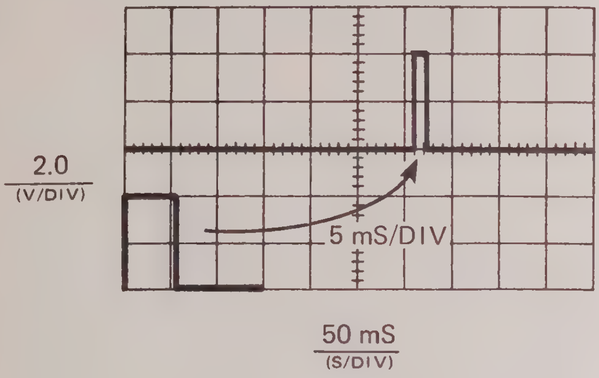
1 BIT SERIAL OUTPUT
U7-6

2.0
(V/DIV)

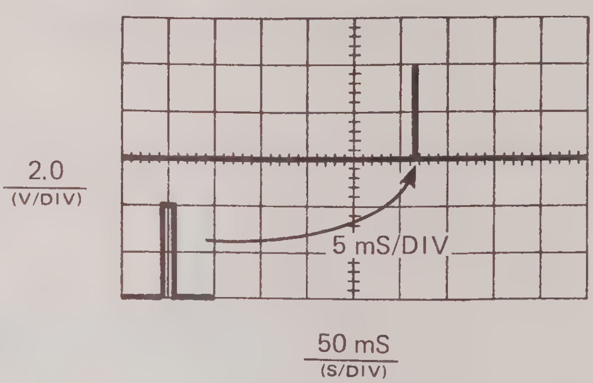


50 mS
(S/DIV)

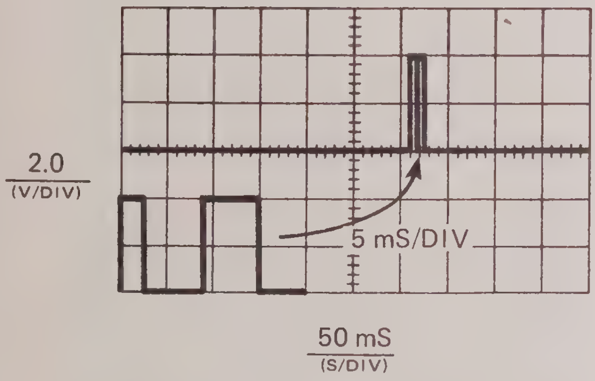
12 (NO.) 2 BIT SERIAL OUTPUT (2)
U7-4



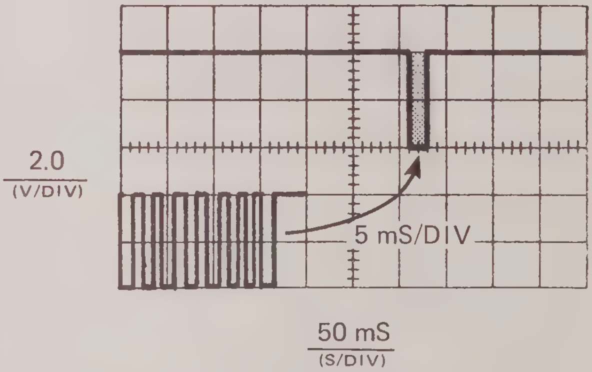
13 (NO.) 3 BIT SERIAL OUTPUT (4)
U7-2



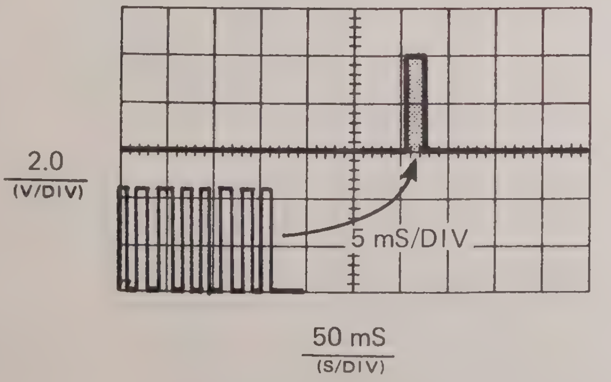
14 (NO.) 4 BIT SERIAL OUTPUT (8)



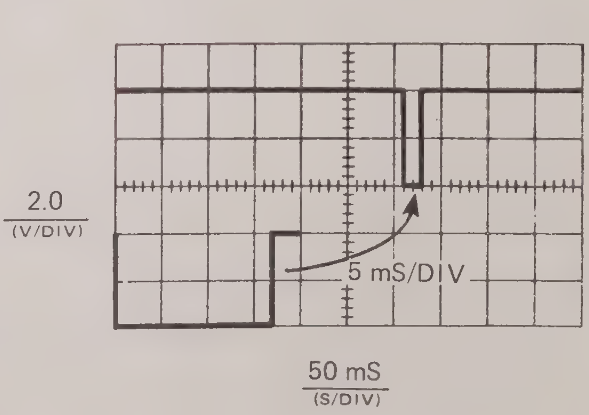
15 (NO.) $\overline{\text{SERIAL STROBE}}$
U8-6



16 (NO.) SERIAL STROBE
U7-10



17 (NO.) PARALLEL DATA VALID
U7-8

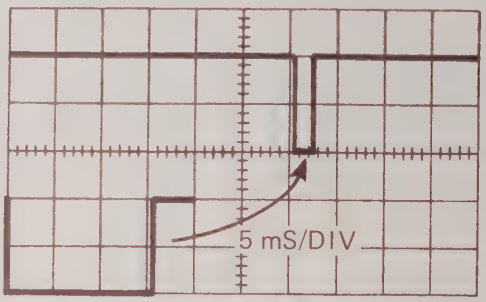


Waveforms for Table 5.26 continued

18
(NO.)

INHIBIT PARALLEL DATA ENABLE
U8-2

2.0
(V/DIV)

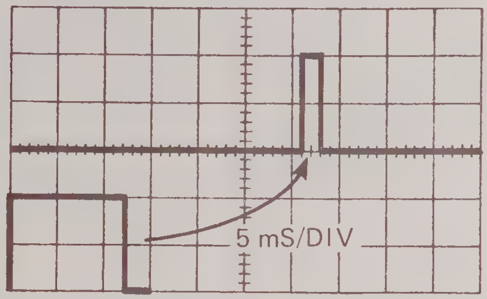


50 mS
(S/DIV)

19
(NO.)

INHIBIT PARALLEL DATA
U8-3

2.0
(V/DIV)



50 mS
(S/DIV)

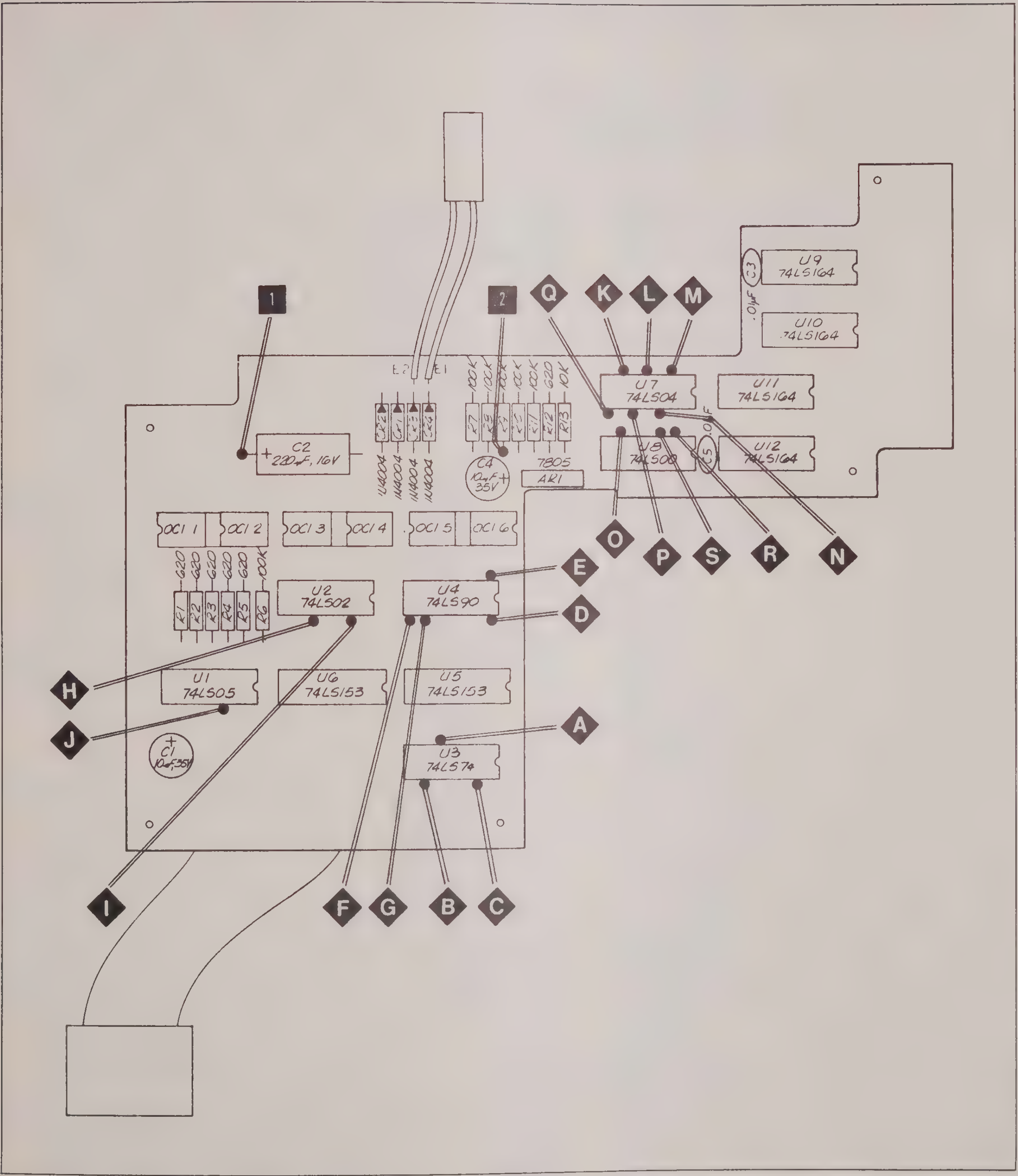

1
2
Q
K
L
M
E2
E1
CR2
CR1
CR3
CR4
1N4004
1N4004
1N4004
1N4004
R7
R8
R9
R10
R11
R12
R13
100K
100K
100K
100K
100K
620
10K
C2
220µF, 16V
C4
10µF
35V
7805
AR1
U7
74LS04
U8
74LS08
U9
74LS164
U10
74LS164
U11
74LS164
U12
74LS164
C3
.01µF
C5
.01µF
O
P
S
R
N
OC1 1
OC1 2
OC1 3
OC1 4
OC1 5
OC1 6
620
620
620
620
620
100K
R1
R2
R3
R4
R5
R6
U2
74LS02
U4
74LS90
E
D
H
U1
74LS05
U6
74LS153
U5
74LS153
J
A
C1
10µF,35V
U3
74LS74
I
F
G
B
C

Figure 5.35 - Data Output Test Point Locations

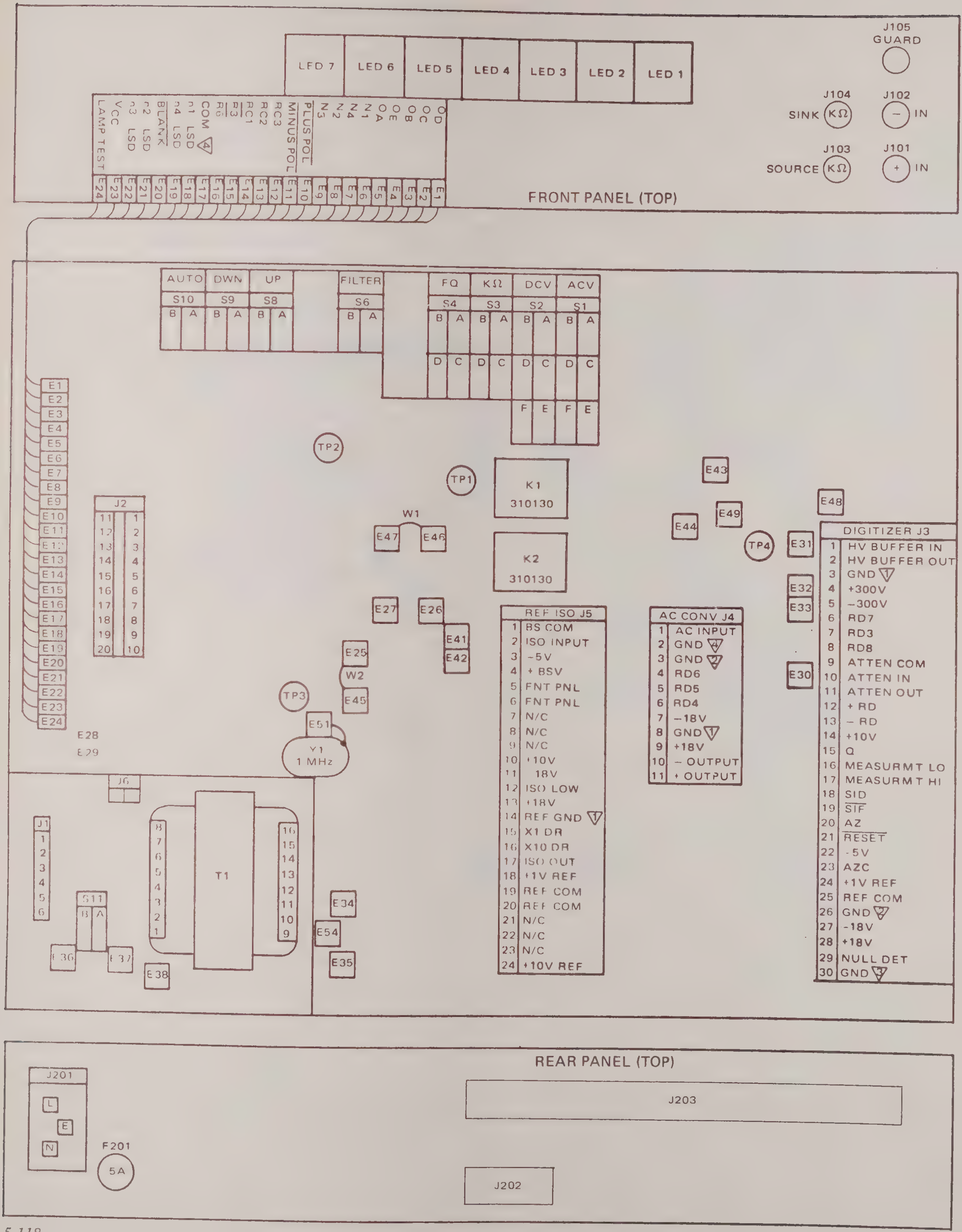

LED 7
LED 6
LED 5
LED 4
LED 3
LED 2
LED 1
J105
GUARD
J104
SINK
KΩ
J102
–
IN
J103
SOURCE
KΩ
J101
+
IN
FRONT PANEL (TOP)
OD
OC
OB
OE
OA
N1
N4
N2
N3
PLUS POL
MINUS POL
RC3
RC2
RC1
R3
R6
COM
n1 LSD
n4 LSD
BLANK
r2 LSD
n3 LSD
VCC
LAMP TEST
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20
E21
E22
E23
E24
AUTO
DWN
UP
FILTER
FQ
KΩ
DCV
ACV
S10
S9
S8
S6
S4
S3
S2
S1
B
A
D
C
F
E
TP2
TP1
TP3
TP4
K1
310130
K2
310130
W1
W2
E47
E46
E43
E44
E49
E48
E31
E32
E33
E30
E27
E26
E41
E42
E25
E45
E51
Y1
1 MHz
E28
E29
J2
1 2 3 4 5 6 7 8 9 10
11 12 13 14 15 16 17 18 19 20
REF ISO J5
1 BS COM
2 ISO INPUT
3 –5V
4 + BSV
5 FNT PNL
6 FNT PNL
7 N/C
8 N/C
9 N/C
10 +10V
11 18V
12 ISO LOW
13 +18V
14 REF GND 1
15 X1 DR
16 X10 DR
17 ISO OUT
18 +1V REF
19 REF COM
20 REF COM
21 N/C
22 N/C
23 N/C
24 +10V REF
AC CONV J4
1 AC INPUT
2 GND 4
3 GND 2
4 RD6
5 RD5
6 RD4
7 –18V
8 GND 1
9 +18V
10 – OUTPUT
11 + OUTPUT
DIGITIZER J3
1 HV BUFFER IN
2 HV BUFFER OUT
3 GND 1
4 +300V
5 –300V
6 RD7
7 RD3
8 RD8
9 ATTEN COM
10 ATTEN IN
11 ATTEN OUT
12 + RD
13 – RD
14 +10V
15 Q
16 MEASURMT LO
17 MEASURMT HI
18 SID
19 SIF
20 AZ
21 RESET
22 -5V
23 AZC
24 +1V REF
25 REF COM
26 GND 2
27 -18V
28 +18V
29 NULL DET
30 GND 3
J6
J1
1 2 3 4 5 6
S11
B A
E36
E37
E38
T1
1 2 3 4 5 6 7 8
9 10 11 12 13 14 15 16
E34
E54
E35
REAR PANEL (TOP)
J201
L
E
N
F201
5A
J203
J202

Figure 5.36 - Model 5100 Interconnect Diagram

Table 5.27 - 5100 Interconnect Pinouts

J101 – "+" IN (DCV, ACV, KΩ)/S1-D-2
J102 – "–" IN (DCV, ACV, KΩ)/S4-D-2
J103 – KΩ Source
J104 – KΩ Sink
J105 – GUARD/E52

S1 – ACV
S2 – DCV
S3 – KΩ
S4 – FQ (Inoperative)

S6 – Filter

S8 – Up
S9 – Down
S10 – Auto
S11 – Power

E1 – 0_D
E2 – 0_C
E3 – 0_B
E4 – 0_E
E5 – 0_A
E6 – N_1
E7 – N_4
E8 – N_2
E9 – N_3
E10 – $\overline{\text{Plus Pol}}$
E11 – $\overline{\text{Minus Pol}}$
E12 – RC3
E13 – RC2
E14 – RC1
E15 – $\overline{\text{R3}}$
E16 – $\overline{\text{R6}}$
E17 – Dig Com
E18 – LSD n1
E19 – LSD n4
E20 – $\overline{\text{Blank}}$
E21 – LSD N_2
E22 – LSD N_3
E23 – V_{CC} (MECCA)
E24 – Lamp Test (Not Used)
E25 – W2-Filter Output
E26 – E42-Iso Input/R29, S1-C-3, S6-A-3

E27 – S1-B-2/R28
E28 – Freq Sig Cond Input
E29 – Dig Com ▽4
E30 – Attenuator In
E31 – HV Buffer In
E32 – +300V
E33 – –300V
E34 – +300V
E35 – –300V
E36 – F201 to S11-B-3 (Line ACV)
E37 – J201-N to S11-A-3 (Neutral)
E38 – Earth Gnd to E53
E39 – S4-B-3 (Freq Signal)
E40 – Freq Shield (Dig Com)
E41 – Shield to BSC
E42 – Isolator Input/E26
E43 – S2-B-1, S2-E-1, K1-8, S3-B-2, & R22
E44 – R27, K1-9, S2-A-1, & S2-B-3
E45 – W2-Filter Output
E46 – W1/R29
E47 – R28/W1
E48 – R22, R26
E49 – R26, R27
E50 – +18V
E51 – Gnd ▽4 to Crystal Can
E52 – Chassis, xfmr core, & Guard (J105)
E53 – XFMR Primary Shield (Earth Gnd.)
E54 – Mecca (shield for E34/35)

J1 – Voltage select PCB Assy. – 403928
J2 – Data Output
J3 – Digitizer PCB Assy. – 403935
J4 – AC (Avg) Converter PCB Assy. – 403905
J5 – Ref Isolator PCB Assy. – 403934
J6 – Data Output Isolated PWR

TP1 – SID (Signal Integrate Drive)
TP2 – Null Detect
TP3 – Digital Ground
TP4 – MECCA Ground

F201 – Line Fuse

J201 – Line Power Conn.
J202 – Read/Hold Conn
J203 – Data Out Conn

SECTION 6 DRAWINGS

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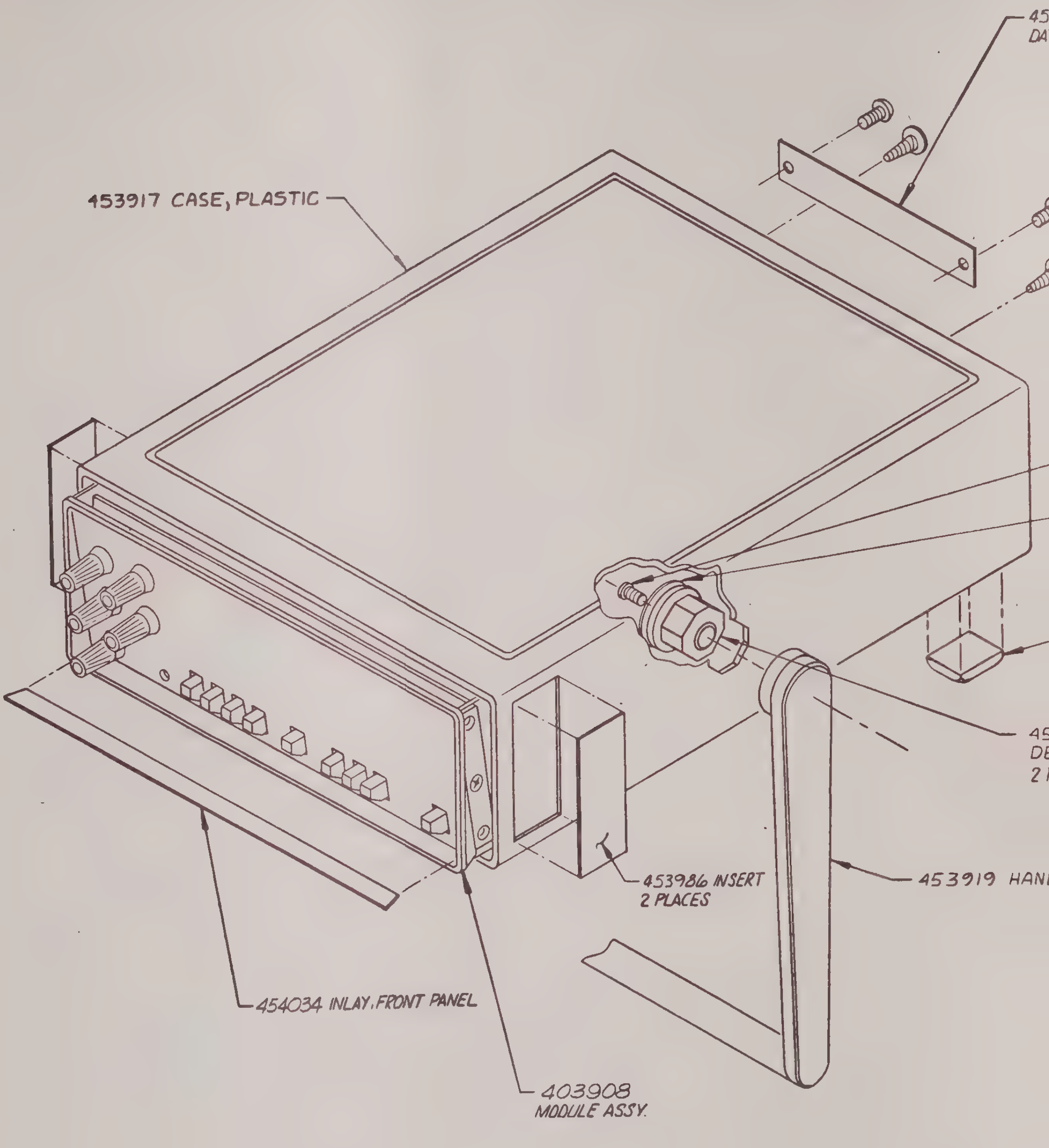
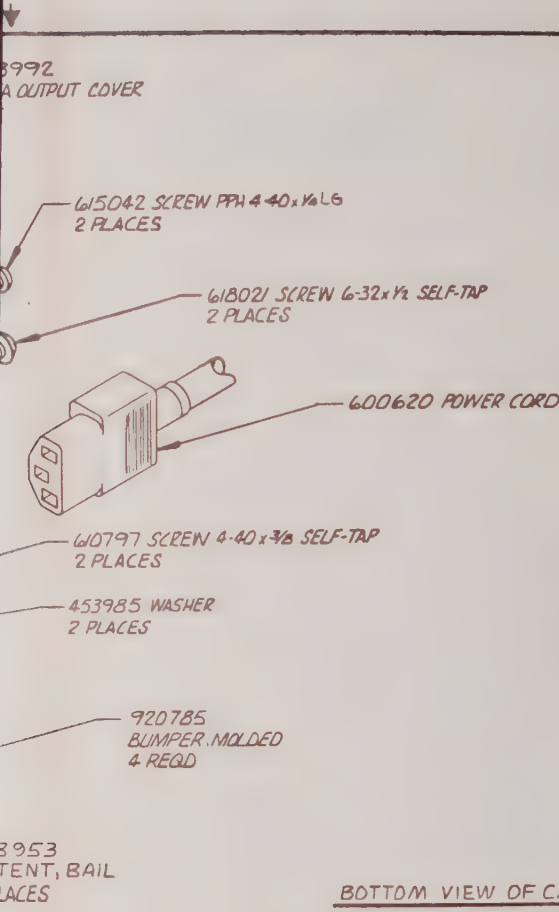
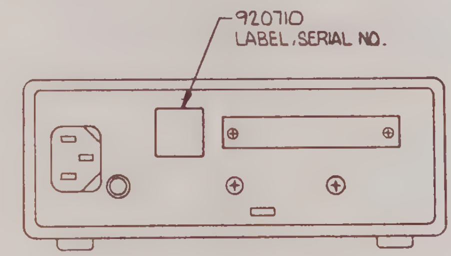

45
DA
453917 CASE, PLASTIC
45
DE
2
453919 HAN
453986 INSERT
2 PLACES
454034 INLAY, FRONT PANEL
403908
MODULE ASSY.

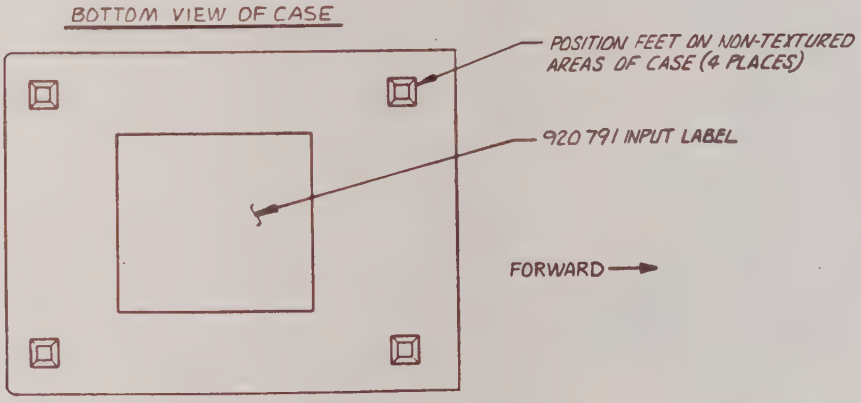
NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN #1120 4/9/76	Magnus		
B	ADDED POWER CORD 600620/PER ED 10159			
C	ADDED 615042 SCREW TO P.L. POWER CORD WAS 600620. / PER ED 10303	7/13/76		
D	POWER CORD WAS 403530 PER ED 10365		9-21-76	
E	ADDED 618021 SCREW LABEL SER NO WAS 920636 / PER ED10445		9-1-76	


3992
A OUTPUT COVER
615042 SCREW PPH 4-40x1/4LG
2 PLACES
618021 SCREW 6-32x1/2 SELF-TAP
2 PLACES
600620 POWER CORD
610797 SCREW 4-40x3/8 SELF-TAP
2 PLACES
453985 WASHER
2 PLACES
920785
BUMPER, MOLDED
4 REQD
3953
TENT, BAIL
LACES
LE, PLASTIC


920710
LABEL, SERIAL NO.

BOTTOM VIEW OF CASE


POSITION FEET ON NON-TEXTURED AREAS OF CASE (4 PLACES)
920791 INPUT LABEL
FORWARD

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

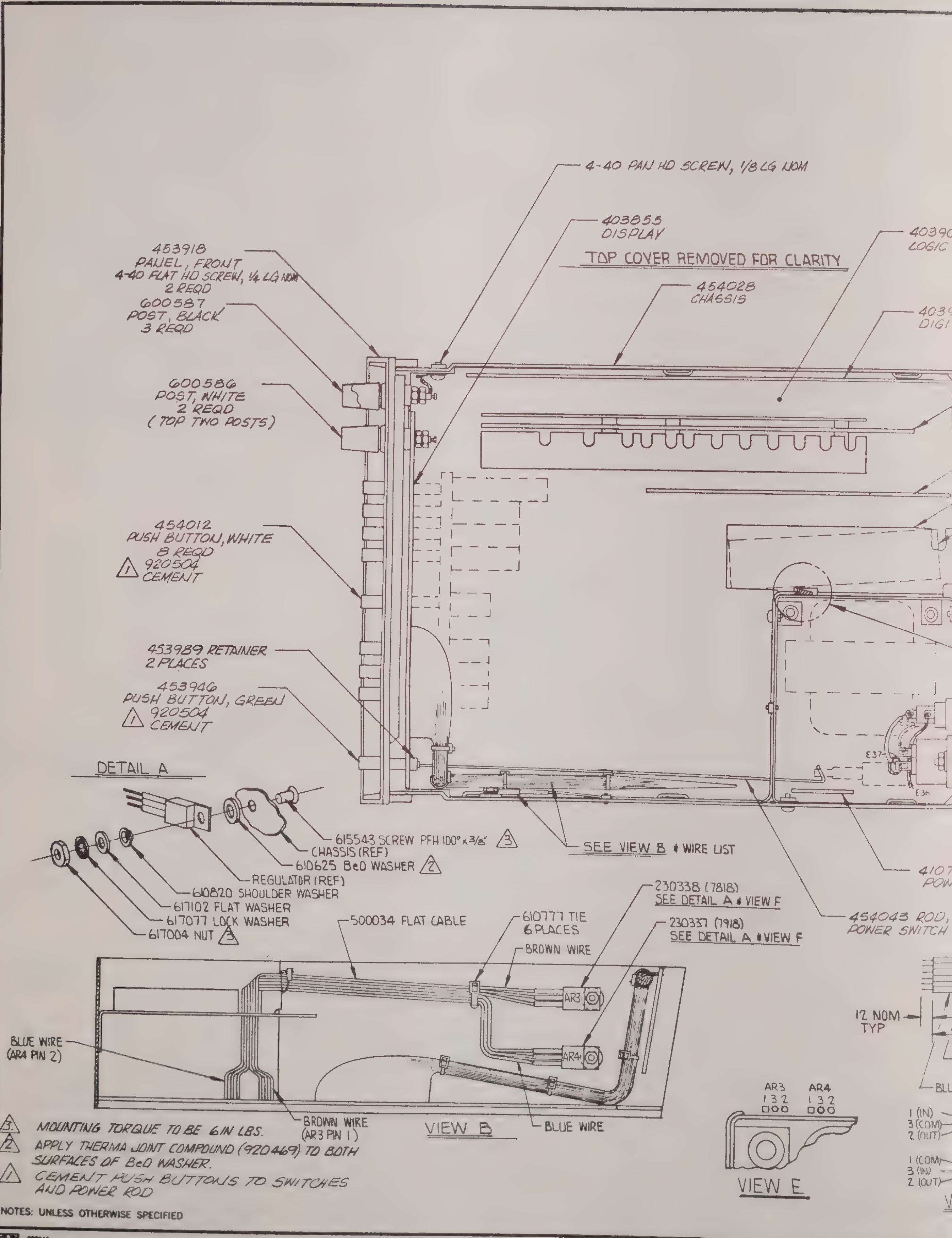
DRAWN		4/20/76
CHECK		
DESIGN		4/9/76
MECH ENGR	Guercio	4-9-76
PROJ ENGR	R. Coleman Jr	4-9-76
PROD ENGR		4976

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DIGITAL MULTIMETER
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	400979	E

SCALE NONE SHEET 1 OF 2


4-40 PAN HD SCREW, 1/8 LG NOM
403855
DISPLAY
TOP COVER REMOVED FOR CLARITY
40390
LOGIC
454028
CHASSIS
4039
DIGI
453918
PANEL, FRONT
4-40 FLAT HD SCREW, 1/4 LG NOM
2 REQD
600587
POST, BLACK
3 REQD
600586
POST, WHITE
2 REQD
(TOP TWO POSTS)
454012
PUSH BUTTON, WHITE
8 REQD
1 920504
CEMENT
453989 RETAINER
2 PLACES
453946
PUSH BUTTON, GREEN
1 920504
CEMENT
E37
E36
DETAIL A
615543 SCREW PFH 100° x 3/8" 3
CHASSIS (REF)
610625 BeO WASHER 2
REGULATOR (REF)
610820 SHOULDER WASHER
617102 FLAT WASHER
617077 LOCK WASHER
617004 NUT 3
SEE VIEW B & WIRE LIST
410
POW
454043 ROD,
POWER SWITCH
230338 (7818)
SEE DETAIL A & VIEW F
230337 (7918)
SEE DETAIL A & VIEW F
500034 FLAT CABLE
610777 TIE
6 PLACES
BROWN WIRE
AR3
AR4
BLUE WIRE
(AR4 PIN 2)
BROWN WIRE
(AR3 PIN 1)
VIEW B
BLUE WIRE
12 NOM
TYP
BLU
AR3
1 3 2
AR4
1 3 2
VIEW E
1 (IN)
3 (COM)
2 (OUT)
1 (COM)
3 (IN)
2 (OUT)
V

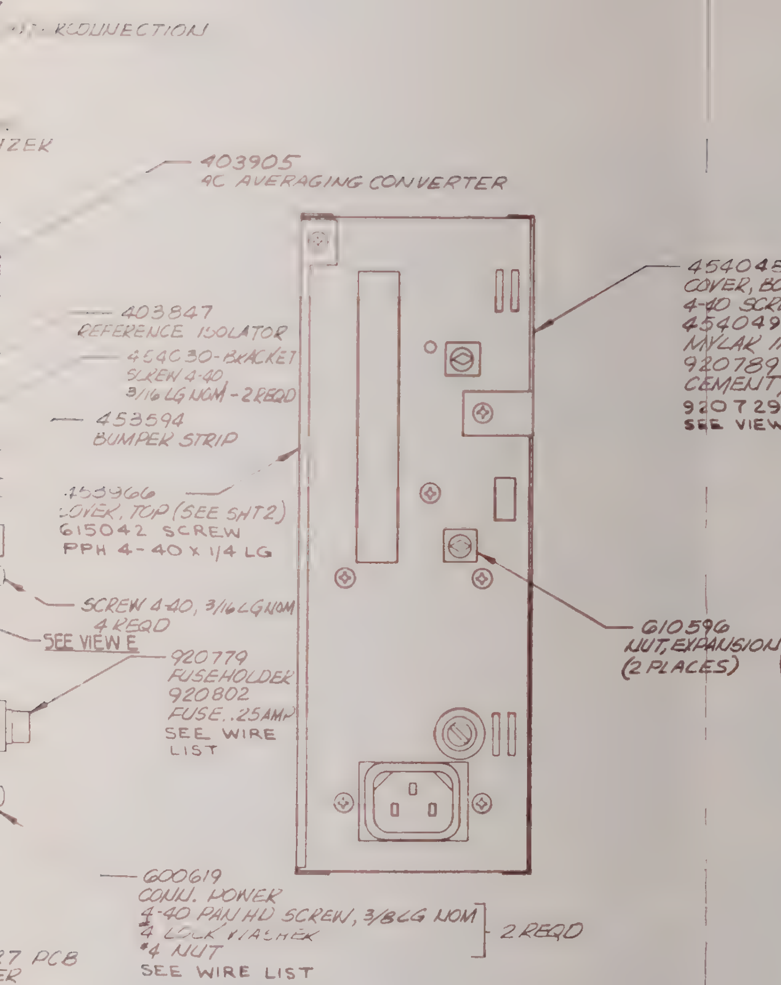
3. MOUNTING TORQUE TO BE 6 IN LBS.

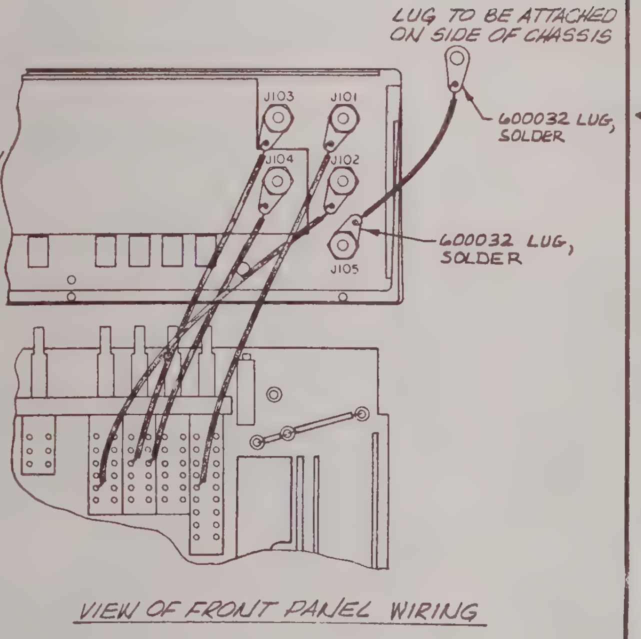
2. APPLY THERMA JOINT COMPOUND (920469) TO BOTH SURFACES OF BeO WASHER.

1. CEMENT PUSH BUTTONS TO SWITCHES AND POWER ROD

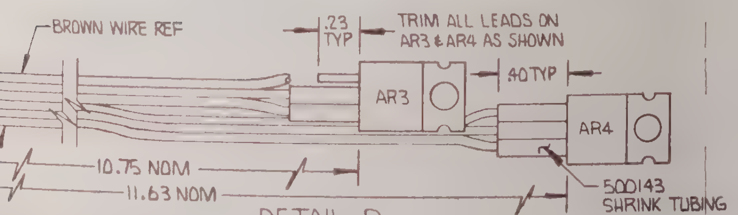
NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1122 4/20/76			
B	REVISED PER E.O 10225	KAM 6 18 76	RLH 7-15-76	
C	REVISED PER E.O 10273	KAM 6-18-76	RLH 7-15-76	
D	REVISED PER E.O 10294	KAM 6.18.76	RLH 7-15-76	J KOCH 7-22-76
E	REVISED PER E.O 10316	KAM 6 18.76	7-15-76	[illegible]
F	10356	KAM	RLH 11-19-76	
H	10399	KAM		J KOCH 11-22-76
J	10495	KAM		
K	10551	KAM 9 8 76	RLH 11-19-76	
L	REVISED PER EO # 10580	RLH 11-19-76		
M	REVISED PER EO # 10581	RLH 11-19-76		
N	REVISED PER EO # 10620	RLH 11-19-76		J KOCH 11-22-76
P	REVISED PER EO # 10720	RLH 12-2-76		
R	ADDED FLAT CABLE / EO 10761	Z.B. 12/14/76		
S	ADDED MOUNTING & WIRE ROUTING FOR AR3 & AR4 ALSO WIRE ROUTING FOR DISPLAY / EO 10815	Z.B. 12/16/76		J KOCH 1-4-77

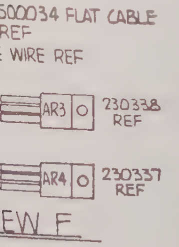

RCONNECTION
IZER
403905
4C AVERAGING CONVERTER
403847
REFERENCE ISOLATOR
454030-BRACKET
SCREW 4-40,
3/16 LG NOM - 2 REQD
453594
BUMPER STRIP
453966
COVER, TOP (SEE SHT 2)
615042 SCREW
PPH 4-40 x 1/4 LG
SCREW 4-40, 3/16 LG NOM
4 REQD
SEE VIEW E
920779
FUSEHOLDER
920802
FUSE .25AMP
SEE WIRE
LIST
454048
COVER, BOTTOM
4-40 SCREW, 3/16 LG NOM
454049
MYLAR INSERT
920789
CEMENT, SPRAY
920729 LABEL
SEE VIEW 'C'
610596
NUT, EXPANSION
(2 PLACES)
600619
CONN. POWER
4-40 PAN HD SCREW, 3/8 LG NOM
4 LOCK WASHER
#4 NUT
SEE WIRE LIST
2 REQD
27 PCB
ER


LUG TO BE ATTACHED
ON SIDE OF CHASSIS
600032 LUG,
SOLDER
J103
J101
J104
J102
600032 LUG,
SOLDER
J105

VIEW OF FRONT PANEL WIRING


BROWN WIRE REF
.23
TYP
TRIM ALL LEADS ON
AR3 & AR4 AS SHOWN
.40 TYP
AR3
AR4
10.75 NOM
11.63 NOM
500143
SHRINK TUBING

DETAIL D


500034 FLAT CABLE
REF
WIRE REF
AR3
230338
REF
AR4
230337
REF

EW F

400979	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL
FINISH

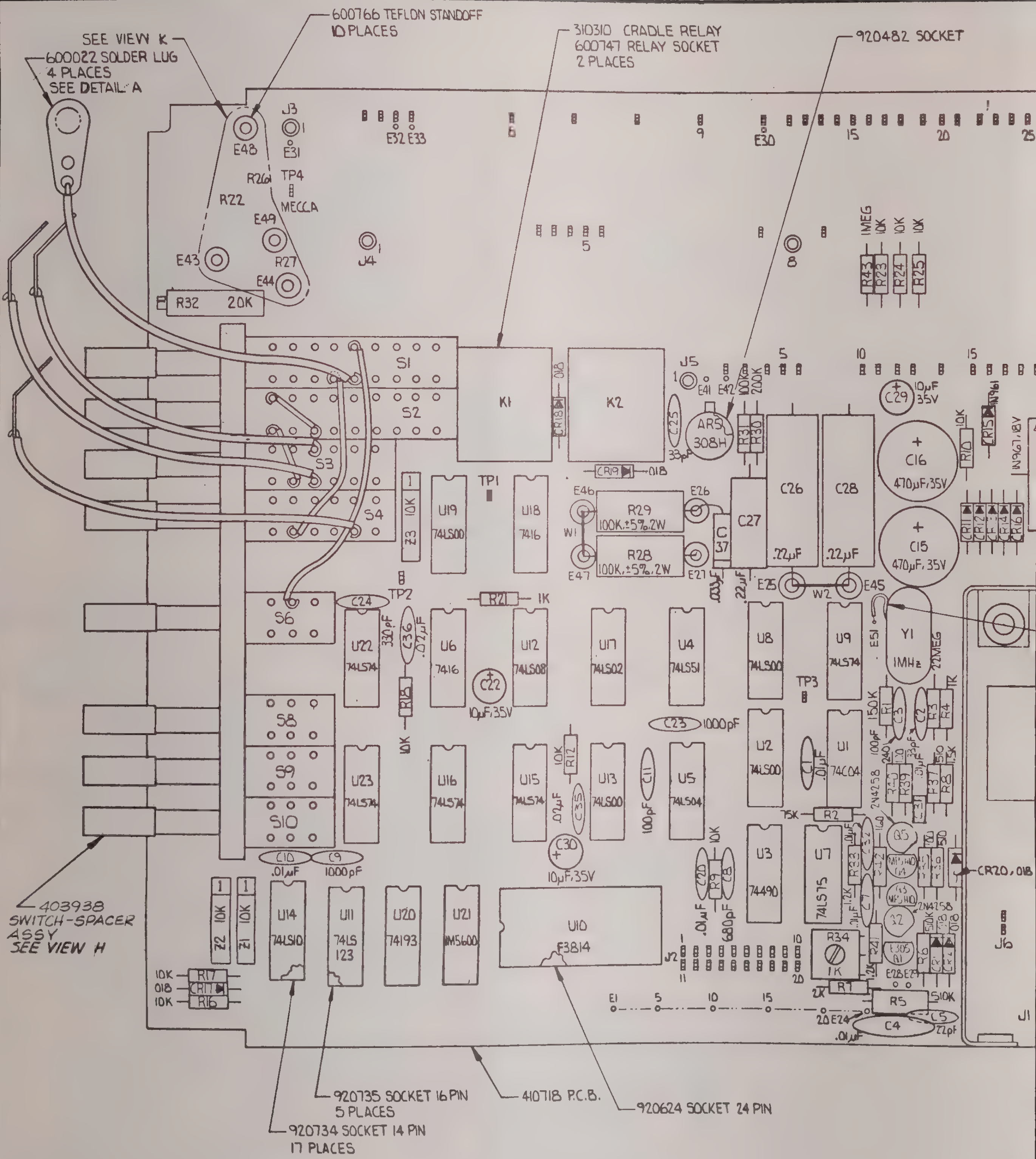
DRAWN		2/12/76
CHECK		
DESIGN		4/15/76
MECH ENGR		4-9-76
PROJ ENGR		4-15-76
PROD ENGR		4-9-76

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

MODULE ASSY
5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403908	S

SCALE NONE
SHEET 1 OF 6

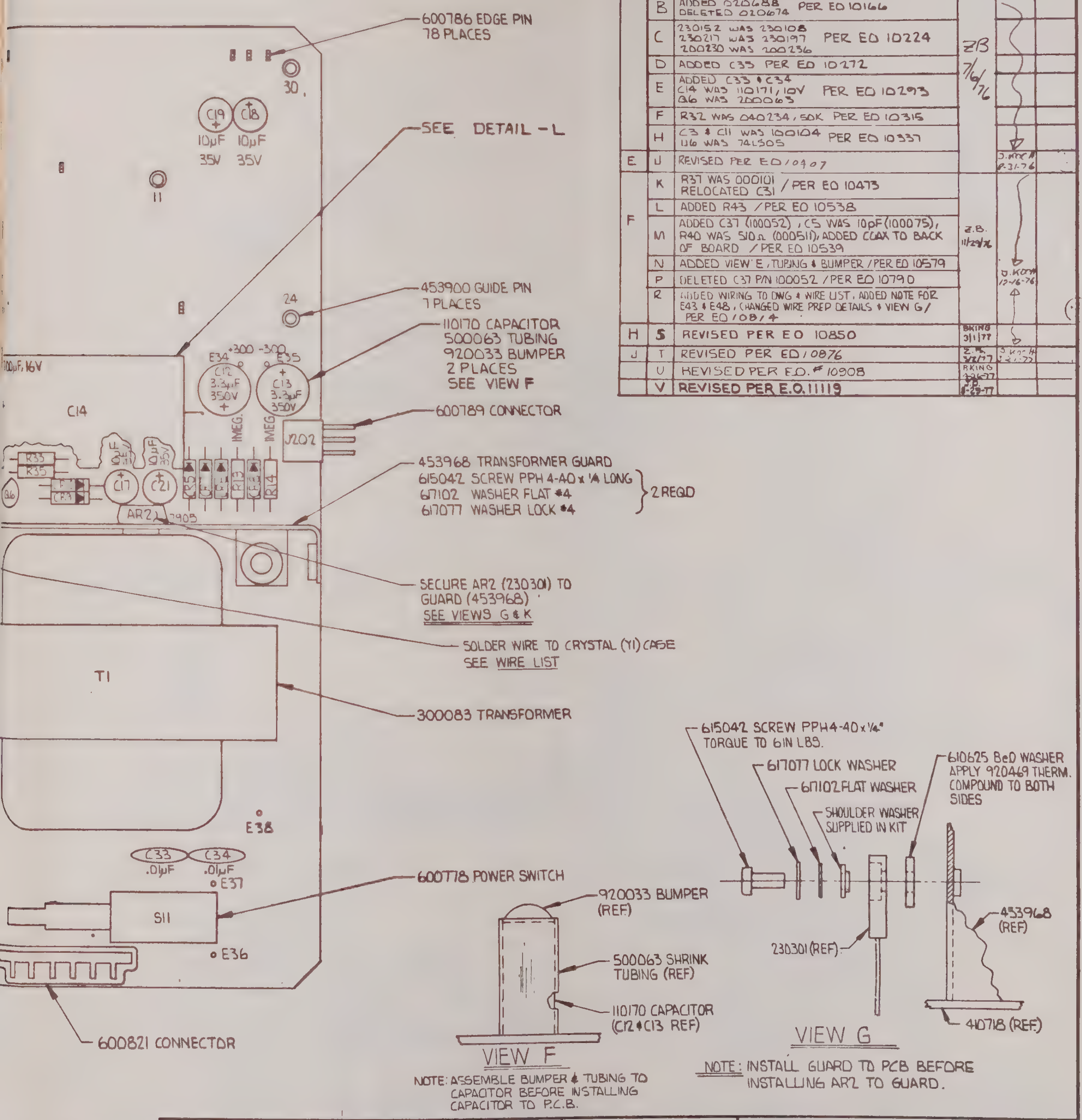


600766 TEFLON STANDOFF 10 PLACES
310310 CRADLE RELAY
600747 RELAY SOCKET
2 PLACES
920482 SOCKET
SEE VIEW K
600022 SOLDER LUG
4 PLACES
SEE DETAIL A
J3
E48
E31
E32 E33
E30
R26
TP4
MECCA
R22
E49
E43
R27
E44
J4
R32 20K
S1
S2
S3
S4
S6
S8
S9
S10
K1
K2
CR18
CR19
J5
E41 E42
AR5 308H
C25 33pF
R31 R30
C29 10µF 35V
C16 470µF/35V
C15 470µF, 35V
CR15 1N961
1N967, 18V
C26 .22µF
C28 .22µF
C27
C37
R29 100K, ±5%, 2W
R28 100K, ±5%, 2W
E46 E26 W1 E47 E27 E25 W2 E45
U19 74LS00
U18 7416
TP1
Z3 10K
TP2
C24 330pF
C36 .02µF
R21 1K
U22 74LS74
U6 7416
U12 74LS08
U17 74LS02
U4 74LS51
U8 74LS00
U9 74LS74
Y1 1MHz
22MEG
E51
TP3
C22 10µF, 35V
R18 10K
C23 1000pF
U2 74LS00
U1 74C04
U23 74LS74
U16 74LS74
U15 74LS74
R12 10K
C35 .02µF
U13 74LS00
C11 100pF
U5 74LS04
U3 74490
U7 74LS75
R2 75K
Q5 Q4 Q3 Q2 Q1
2N4258
CR20, 018
C10 .01µF
C9 1000pF
C30 10µF, 35V
Z2 10K
Z1 10K
U14 74LS10
U11 74LS 123
U20 74193
U21 IM5600
U10 F3814
C20 .01µF
R9
C8 680pF
J2
R34 1K
R1
R5 510K
C4 .01µF
C5 22pF
E24
J6
J1
R17 10K
CR17 018
R16 10K
403938 SWITCH-SPACER ASSY SEE VIEW H
920735 SOCKET 16 PIN 5 PLACES
920734 SOCKET 14 PIN 17 PLACES
410718 P.C.B.
920624 SOCKET 24 PIN

4. DIODES CR5 THRU CR14 ARE IN4004
3. RESISTORS ARE IN OHMS, 5%, ¼W.
2. SCHEMATIC REF. 432095.
1 ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	A	RELEASED PER DRN # 1122 4/20/76			
	B	ADDED 020688 DELETED 020674 PER EO 10166	ZB 7/6/76		
	C	230152 WAS 230108 230217 WAS 230197 PER EO 10224 200230 WAS 200236			
	D	ADDED C33 PER EO 10272			
	E	ADDED C33 & C34 C14 WAS 110171, 10V PER EO 10293 Q6 WAS 200063			
	F	R32 WAS 040234, 50K PER EO 10315			
	H	C3 & C11 WAS 100104 PER EO 10337 U6 WAS 74LS05			
E	J	REVISED PER EO 10407		J. Koch 8-31-76	
F	K	R37 WAS 000101 RELOCATED C31 / PER EO 10473	Z.B. 11/29/76	D. Koch 12-16-76	
	L	ADDED R43 / PER EO 10538			
	M	ADDED C37 (100052), C5 WAS 10pF (100075), R40 WAS 510Ω (000511), ADDED COAX TO BACK OF BOARD / PER EO 10539			
	N	ADDED VIEW E, TUBING & BUMPER / PER EO 10579			
	P	DELETED C37 P/N 100052 / PER EO 10790			
	R	ADDED WIRING TO DWG & WIRE LIST, ADDED NOTE FOR E43 & E48, CHANGED WIRE PREP DETAILS & VIEW G / PER EO 10814			
H	S	REVISED PER EO 10850	BKING 3/1/77		
J	T	REVISED PER EO 10876	Z.B. 3/2/77	J. Koch 3-21-77	
	U	REVISED PER E.O. # 10908	RKING 3-26-77		
	V	REVISED PER E.O. 11119	Z.B. 8-29-77		


600786 EDGE PIN
78 PLACES
30
C19
C18
10µF
10µF
35V
35V
SEE DETAIL - L
11
453900 GUIDE PIN
7 PLACES
24
110170 CAPACITOR
500063 TUBING
920033 BUMPER
2 PLACES
SEE VIEW F
100µF, 16V
+300
-300
E34
E35
C12
3.3µF
350V
C13
3.3µF
350V
C14
600789 CONNECTOR
IMEG
IMEG
J202
R33
R35
10µF
35V
10µF
35V
C17
C21
CR3
Q6
R15
R13
R14
AR2
7905
453968 TRANSFORMER GUARD
615042 SCREW PPH 4-40 x 1/4 LONG
617102 WASHER FLAT #4
617077 WASHER LOCK #4
2 REQD
SECURE AR2 (230301) TO
GUARD (453968)
SEE VIEWS G & K
SOLDER WIRE TO CRYSTAL (Y1) CASE
SEE WIRE LIST
T1
300083 TRANSFORMER
E38
C33
.01µF
C34
.01µF
E37
600778 POWER SWITCH
S11
E36
600821 CONNECTOR
920033 BUMPER
(REF)
500063 SHRINK
TUBING (REF)
110170 CAPACITOR
(C12 & C13 REF)
VIEW F
615042 SCREW PPH4-40 x 1/4"
TORQUE TO 6IN LBS.
617077 LOCK WASHER
617102 FLAT WASHER
SHOULDER WASHER
SUPPLIED IN KIT
610625 BeO WASHER
APPLY 920469 THERM.
COMPOUND TO BOTH
SIDES
453968
(REF)
230301 (REF)
410718 (REF)
VIEW G

NOTE: ASSEMBLE BUMPER & TUBING TO CAPACITOR BEFORE INSTALLING CAPACITOR TO P.C.B.

NOTE: INSTALL GUARD TO PCB BEFORE INSTALLING AR2 TO GUARD.

PROPRIETARY NOTICE

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NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403908	5100	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

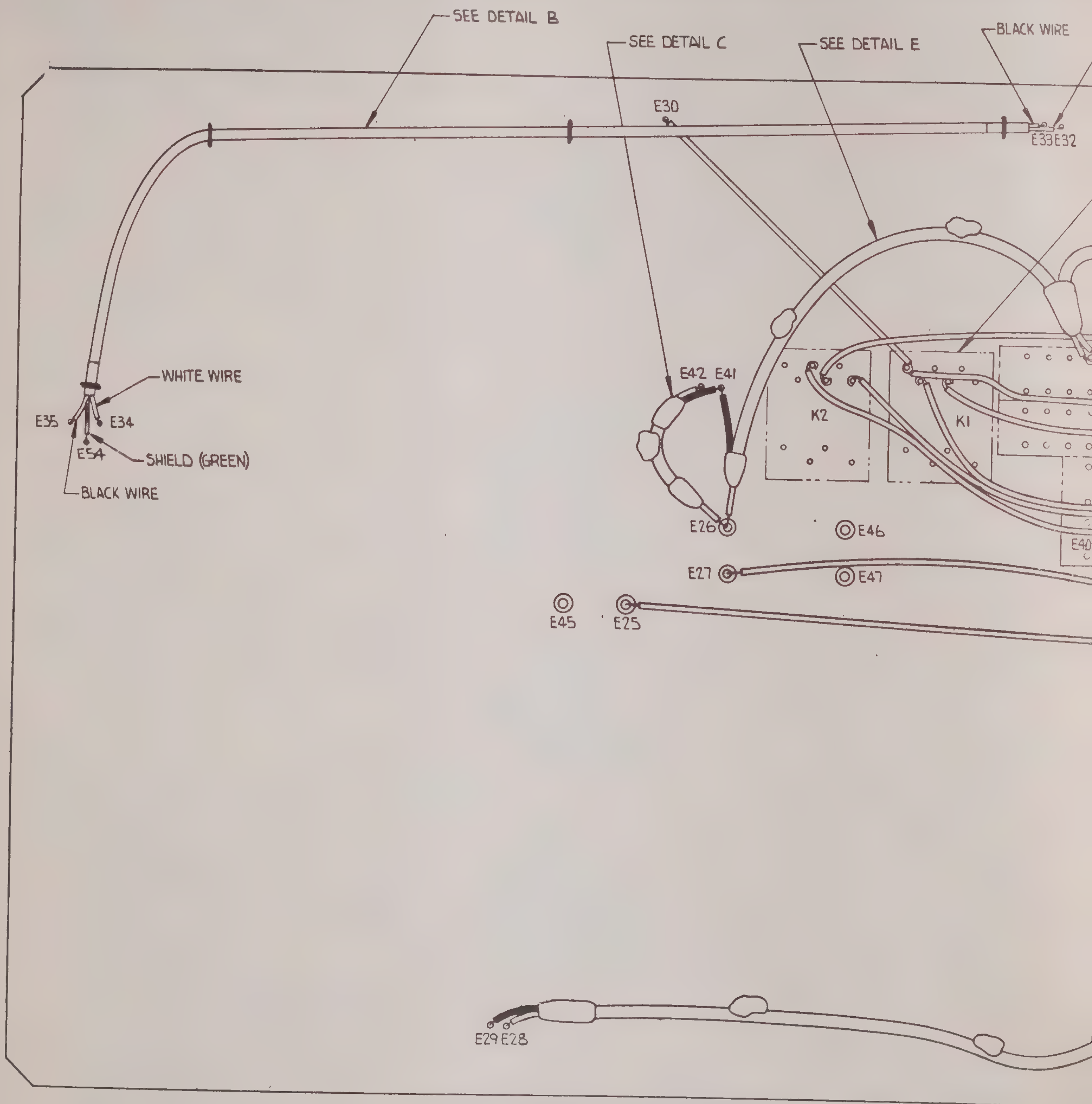
MATERIAL	FINISH

DRAWN	Y. Enson	4/19/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R. Kelemek	4-19-76
PROD ENGR	C.A.	4-2...

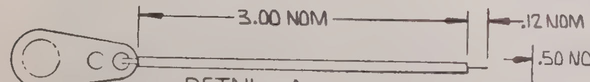
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSEMBLY-
MAIN BOARD LOGIC & INTERCONNECTION
MODEL 5100

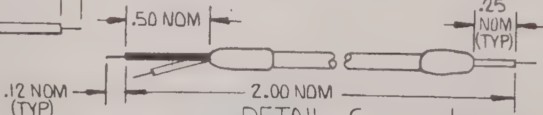
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403907	V
SCALE 2/1		SHEET 1 OF 9	


SEE DETAIL B
SEE DETAIL C
SEE DETAIL E
BLACK WIRE
E30
E33 E32
WHITE WIRE
E35
E34
E54
SHIELD (GREEN)
BLACK WIRE
E42 E41
K2
K1
E26
E46
E27
E47
E40
E45
E25
E29 E28

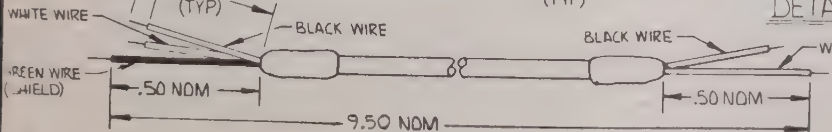
CIRCUIT SIDE SHOWN


3.00 NOM
.12 NOM

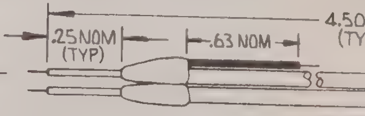
DETAIL A


.50 NOM
.25 NOM (TYP)
.12 NOM (TYP)
2.00 NOM

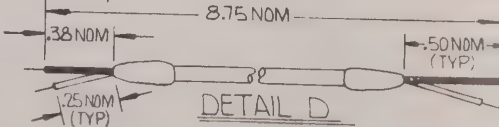
DETAIL C


.12 NOM (TYP)
.38 NOM (TYP)
WHITE WIRE
BLACK WIRE
GREEN WIRE (SHIELD)
.50 NOM
BLACK WIRE
WHITE WIRE
.50 NOM
9.50 NOM

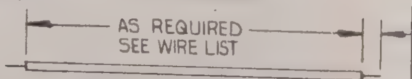
DETAIL B


4.50
(TY
.25 NOM (TYP)
.63 NOM

DET


8.75 NOM
.38 NOM
.50 NOM (TYP)
.25 NOM (TYP)

DETAIL D

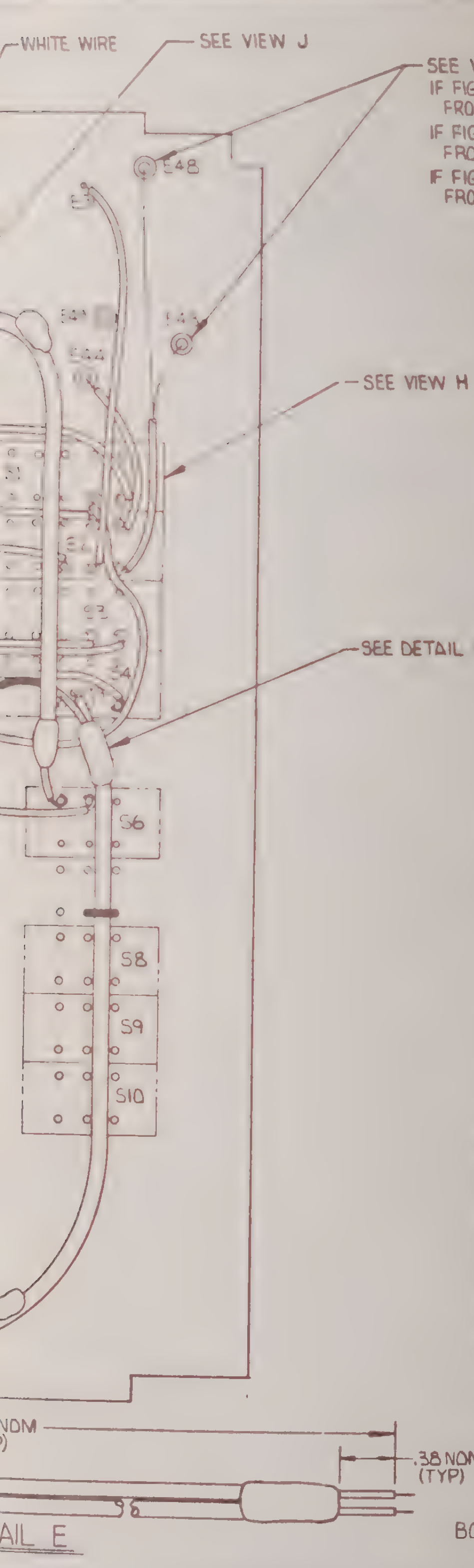

AS REQUIRED SEE WIRE LIST

JUMPER PREPARATION

~~NOTES: UNLESS OTHERWISE SPECIFIED~~

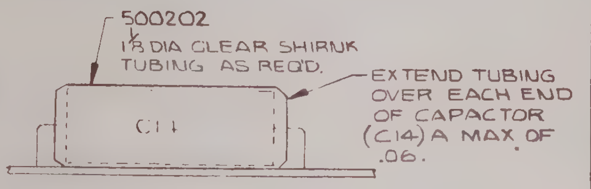
DATA 980346 DIETERICH POST CLEARPRINT 1000

LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
	RELEASED PER DRN # SEE SHEET 1			



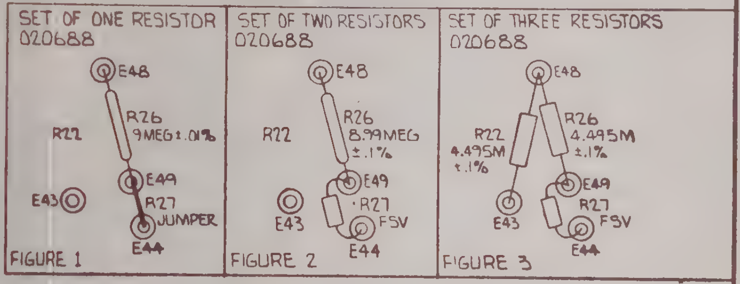
WHITE WIRE
SEE VIEW J
SEE VIEW K (REF)
E48
E43
E44
SEE VIEW H
SEE DETAIL D
S6
S8
S9
S10
NOM
.38 NOM (TYP)
AIL E

IF FIG. 1 IS USED INSTALL WIRE FROM E48 TO S2-B-1 ONLY.
IF FIG. 2 IS USED INSTALL WIRE FROM E48 TO S2-B-1 ONLY.
IF FIG 3 IS USED INSTALL WIRE FROM E43 TO S2-B-1 ONLY.



500202
1/8 DIA CLEAR SHIRNK TUBING AS REQ'D.
EXTEND TUBING OVER EACH END OF CAPACTOR (C14) A MAX OF .06.
C14

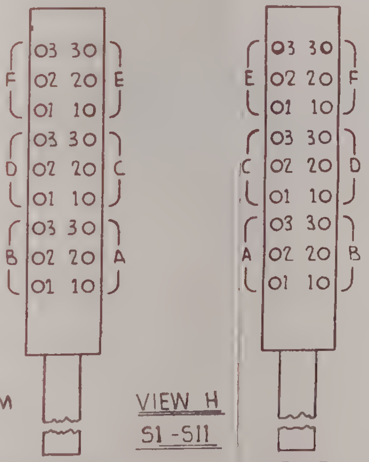
DETAIL



SET OF ONE RESISTOR 020688
E48
R26 9MEG±.01%
R22
E49
E43
R27 JUMPER
E44
FIGURE 1
SET OF TWO RESISTORS 020688
E48
R26 8.99MEG ±.1%
R22
E49
E43
R27
FSV
E44
FIGURE 2
SET OF THREE RESISTORS 020688
E48
R22 4.495M ±.1%
R26 4.495M ±.1%
E49
E43
R27
FSV
E44
FIGURE 3

VIEW K

COMPONENT SIDE SHOWN
(SEE SHEET 1)



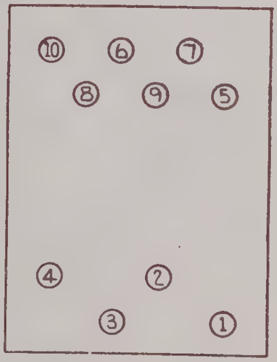
03 30
02 20
01 10
F
E
D
C
B
A

BOTTOM VIEW

TOP VIEW

VIEW H

S1 -S11

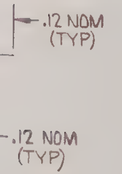


⑩ ⑥ ⑦
⑧ ⑨ ⑤
④ ②
③ ①

BOTTOM VIEW

K1 & K2

VIEW J



.12 NOM (TYP)
.12 NOM (TYP)

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	Z Benson	4/19/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		12 76
PROD ENGR		

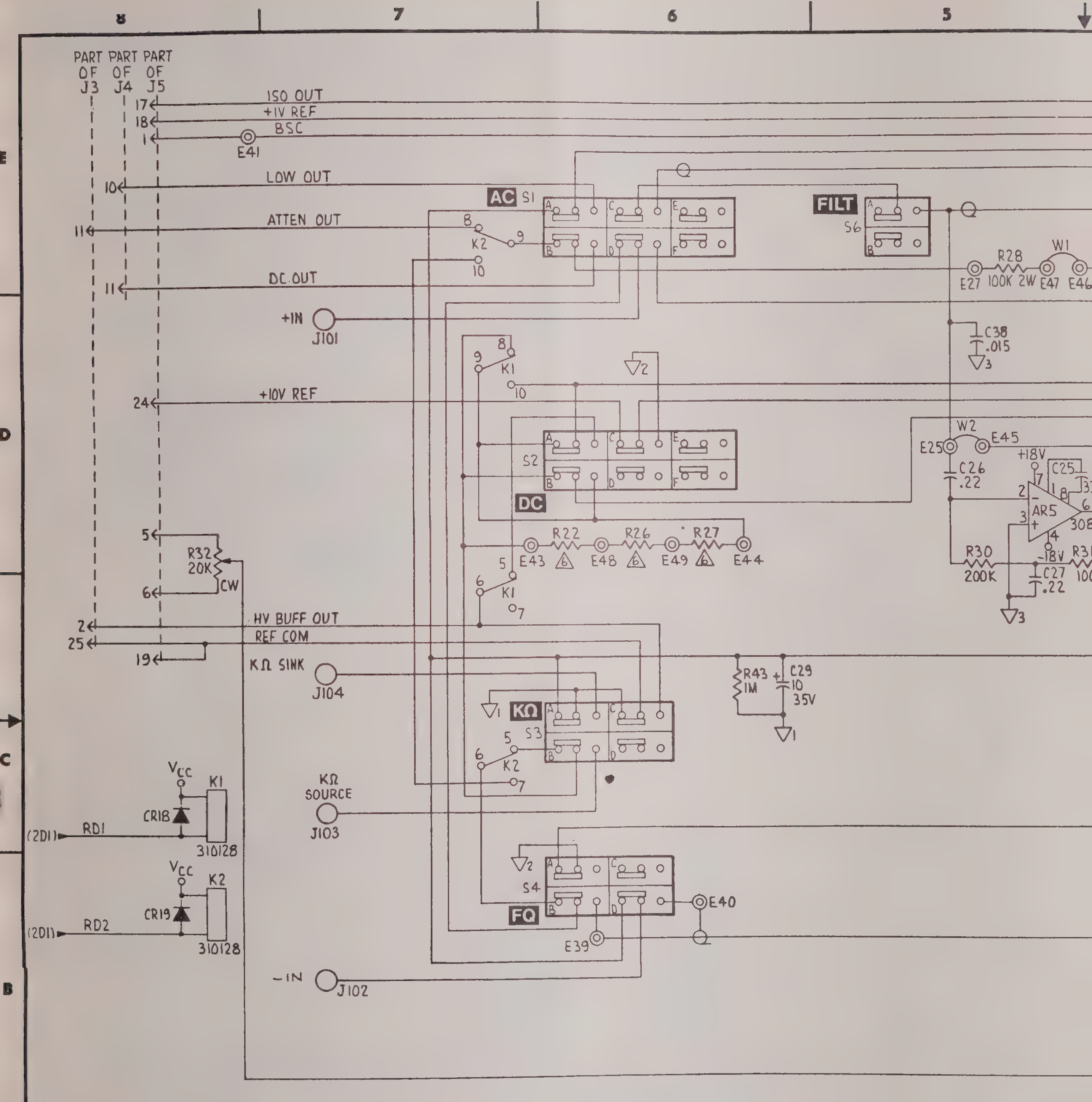
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSEMBLY-
MAIN BOARD LOGIC & INTERCONNECTION
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403907	V

SCALE
SHEET 2 OF 9

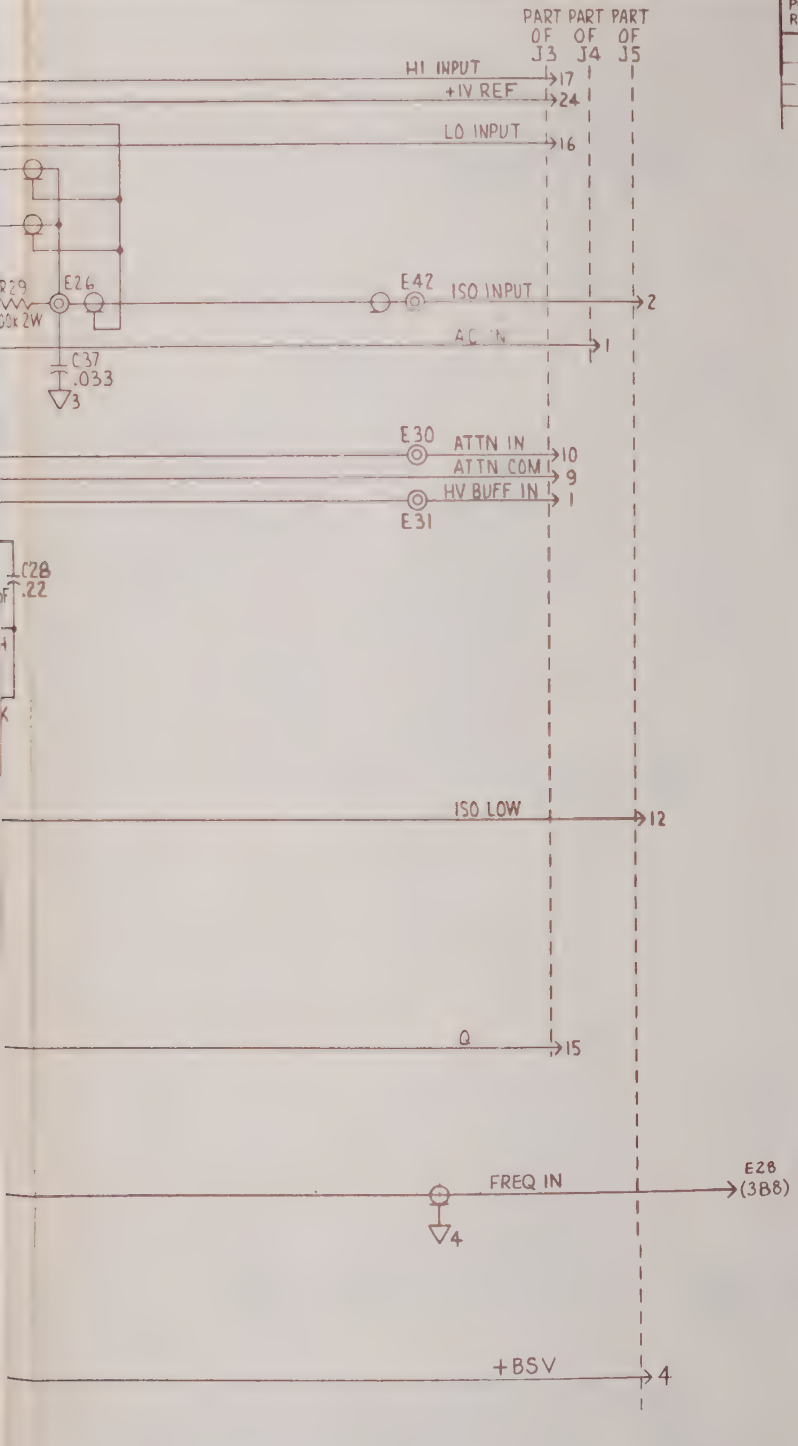
65

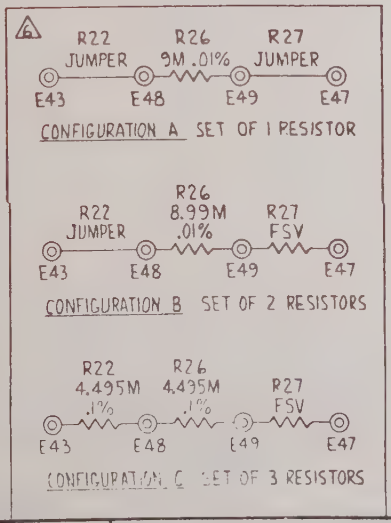

PART OF J3
PART OF J4
PART OF J5
17
18
1
ISO OUT
+1V REF
BSC
E41
10
LOW OUT
AC S1
FILT
S6
11
ATTEN OUT
K2
8
9
10
11
DC OUT
R28
100K 2W
W1
E27
E47
E46
+IN
J101
K1
C38
.015
24
+10V REF
S2
DC
W2
E25
E45
C26
.22
+18V
C25
AR5
308
R22
R26
R27
E43
E48
E49
E44
5
R32
20K
CW
6
R30
200K
-18V
R31
C27
.22
2
HV BUFF OUT
25
REF COM
19
KΩ SINK
J104
R43
1M
C29
10
35V
KΩ
S3
KΩ SOURCE
J103
Vcc
K1
CR18
(2D1)
RD1
310128
Vcc
K2
CR19
(2D1)
RD2
310128
S4
FQ
E40
E39
-IN
J102

NOTES: UNLESS OTHERWISE SPECIFIED

PROPRIE
THIS DOCUMENT AND T
ON DISCLOSED, ARE
LABORATORIES, INC.
EXPRESS WRITTEN PE
RATORIES, INC BE USE
IN WHOLE OR IN PART,
TIONS FROM A COMPET
MANUFACTURE BY AN
LABORATORIES, INC
HAS BEEN DEVELOPED
MAY ONLY BE USED FOR
EVALUATION AND F
TECHNICAL SPECIFICA
MENTS WHICH SPECIFY
FROM DANA LABORATO

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		REVISIONS			
	D	RELEASED PER DRN #			
	—	REDRAWN WITHOUT CHANGE	PA 10 12 77		
	E	REVISED PER EO 10908	PA 10-12-77		
	F	REVISED PER EO 11196	PA 10-12-77		


PART OF J3
PART OF J4
PART OF J5
HI INPUT
17
+1V REF
24
LO INPUT
16
R29
E26
00k 2W
E42
ISO INPUT
2
AC IN
1
C37
.033
3
E30
ATTN IN
10
ATTN COM
9
HV BUFF IN
1
E31
C28
.22
ISO LOW
12
Q
15
FREQ IN
E28
(3B8)
4
+BSV
4


6
R22
JUMPER
R26
9M .01%
R27
JUMPER
E43
E48
E49
E47
CONFIGURATION A SET OF 1 RESISTOR
R22
JUMPER
R26
8.99M
.01%
R27
FSV
E43
E48
E49
E47
CONFIGURATION B SET OF 2 RESISTORS
R22
4.495M
.1%
R26
4.495M
.1%
R27
FSV
E43
E48
E49
E47
CONFIGURATION C SET OF 3 RESISTORS

ARY NOTICE

E TECHNICAL DATA HERE- PROPRIETARY TO DANA ND SHALL NOT, WITHOUT MISSION OF DANA LABO- RELEASED OR DISCLOSED R USED TO SOLICIT QUOTA- IVE SOURCE OR USED FOR ONE OTHER THAN DANA E INFORMATION HEREON T PRIVATE EXPENSE, AND URPOSES OF ENGINEERING INCORPORATION INTO ONS AND OTHER DOCU DCUREMENT OF PRODUCTS ES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403907	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X 030 XX 020 XXX.010	0' 30' FORMED 1° 0'	+ 004 -- .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

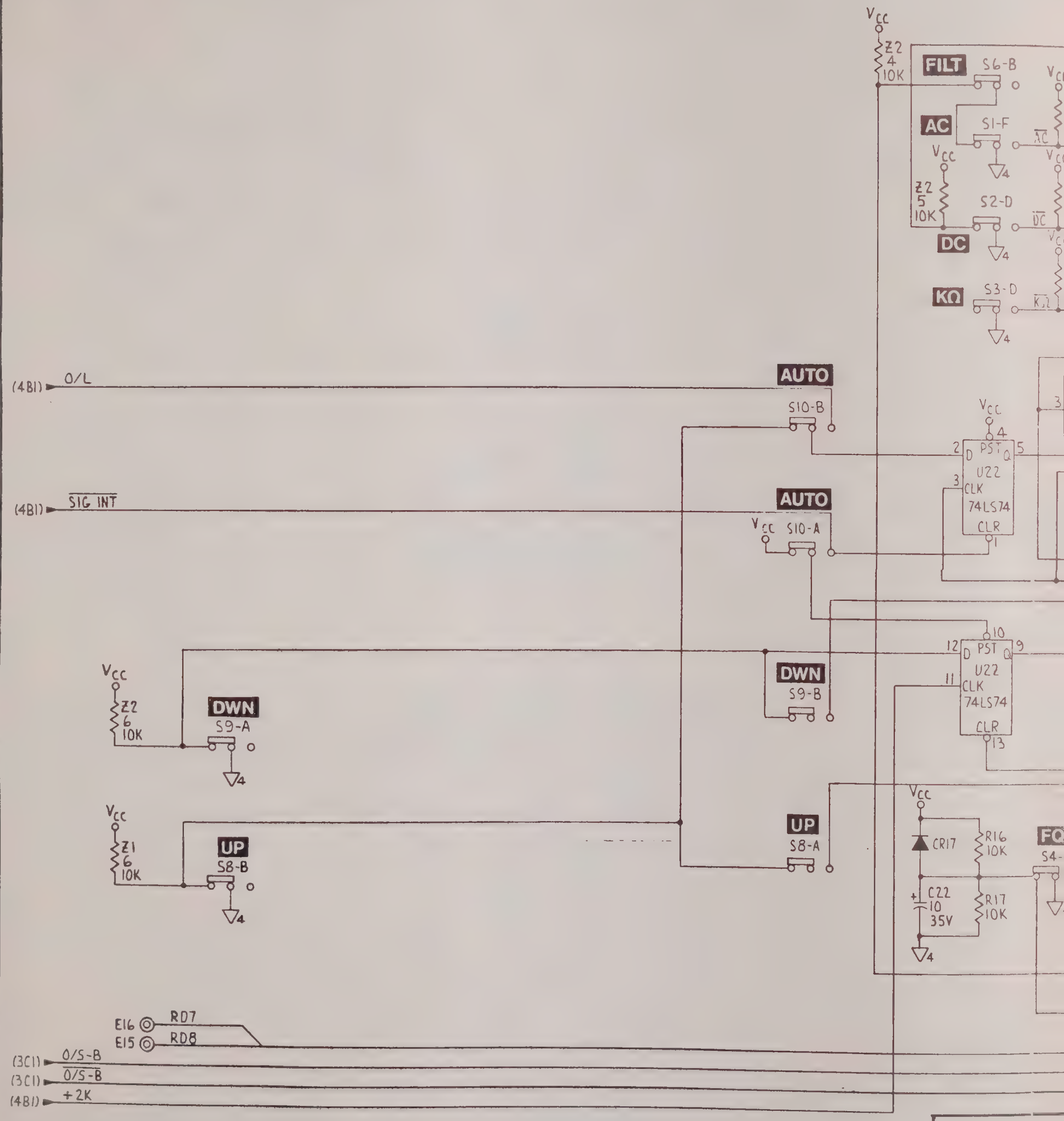
DRAWN		
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC—
MAIN LOGIC & INTERCONNECT
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432095	F
SCALE		SHEET 1 OF 5	


E
D
C
B
A
8
7
6
5
Vcc
Z2 4 10K
FILT
S6-B
AC
S1-F
AC
DC
S2-D
Z2 5 10K
DC
KΩ
S3-D
KΩ
4
(4B1)
O/L
AUTO
S10-B
SIG INT
AUTO
S10-A
2
D
PST
Q
5
U22
3
CLK
74LS74
CLR
1
10
12
9
11
13
DWN
S9-B
DWN
S9-A
Z2 6 10K
Z1 6 10K
UP
S8-B
UP
S8-A
CR17
R16 10K
R17 10K
C22 10 35V
FQ
S4-
E16
E15
RD7
RD8
(3C1)
O/S-B
O/S-B
+2K

NOTES: UNLESS OTHERWISE SPECIFIED

PROPRIET
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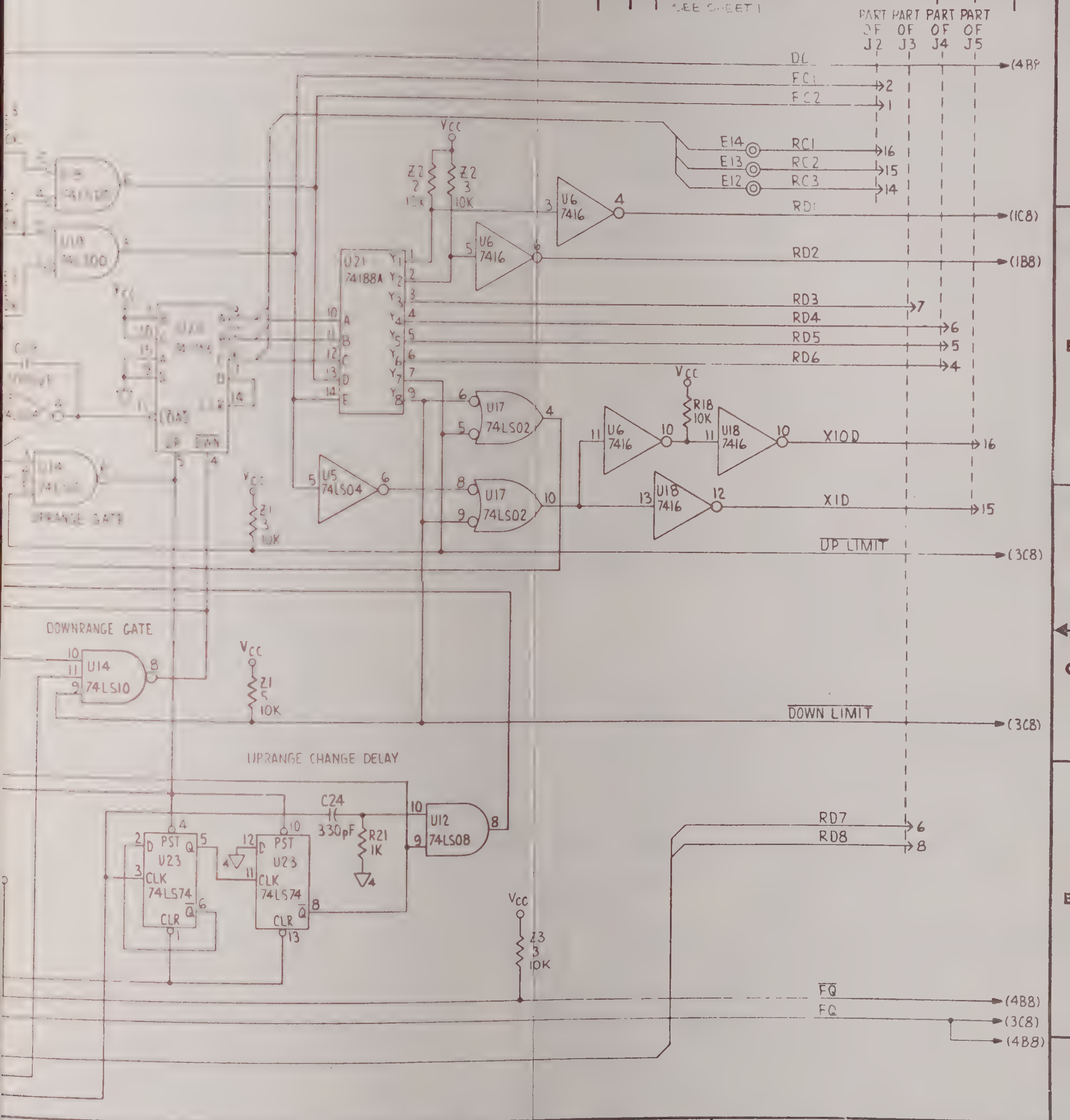
ON DISCLOSED, ARE
LABORATORIES, INC., A
EXPRESS WRITTEN PER
RATORIES, INC. BE USE
IN WHOLE OR IN PART,
TIONS FROM A COMPETI
MANUFACTURE BY AN
LABORATORIES, INC. T
HAS BEEN DEVELOPED
MAY ONLY BE USED FOR
EVALUATION AND FC
TECHNICAL SPECIFICAT
MENTS WHICH SPECIFY P
FROM DANA LABORATOR

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			


PART OF J2
PART OF J3
PART OF J4
PART OF J5
DL
(4B8)
FC1
FC2
E14
E13
E12
RC1
RC2
RC3
RD1
(1C8)
RD2
(1B8)
RD3
RD4
RD5
RD6
VCC
Z2 2 10K
Z2 3 10K
U6 7416
U21 74188A
U5 74LS04
U17 74LS02
R18 10K
U18 7416
X10D
X1D
Z1 3 10K
UP LIMIT
(3C8)
DOWNRANGE GATE
U14 74LS10
Z1 5 10K
DOWN LIMIT
(3C8)
UPRANGE GATE
UPRANGE CHANGE DELAY
C24 330pF
R21 1K
U12 74LS08
U23 74LS74
D PST Q CLK CLR
LOAD
UP DWN
RD7
RD8
Z3 3 10K
FQ
FQ
(4B8)
(3C8)
(4B8)
U18 74LS00

RY NOTICE
E TECHNICAL DATA HERE-
ROPRIETARY TO DANA
ID SHALL NOT, WITHOUT
ISSION OF DANA LABO
RELEASED OR DISCLOSED
USED TO SOLICIT QUOTA
VE SOURCE OR USED FOR
NE OTHER THAN DANA
E INFORMATION HEREON
PRIVATE EXPENSE, AND
URPOSES OF ENGINEERING
INCORPORATION INTO
NS AND OTHER DOCU-
CUREMENT OF PRODUCTS
ES, INC

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403907	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL FINISH

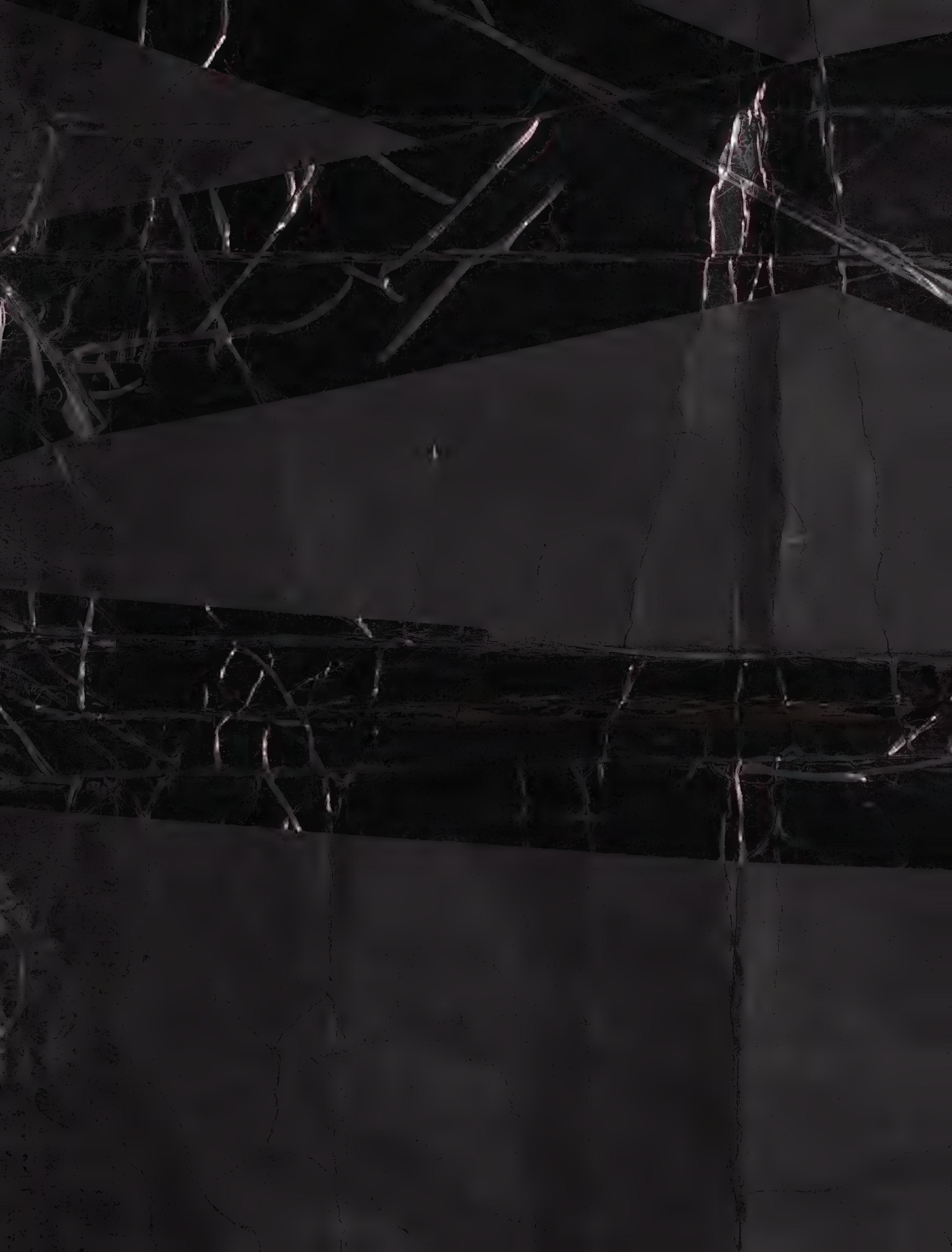
DRAWN	Rich Mays	4-17-77
CHECK	W Stanton	10-12-77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

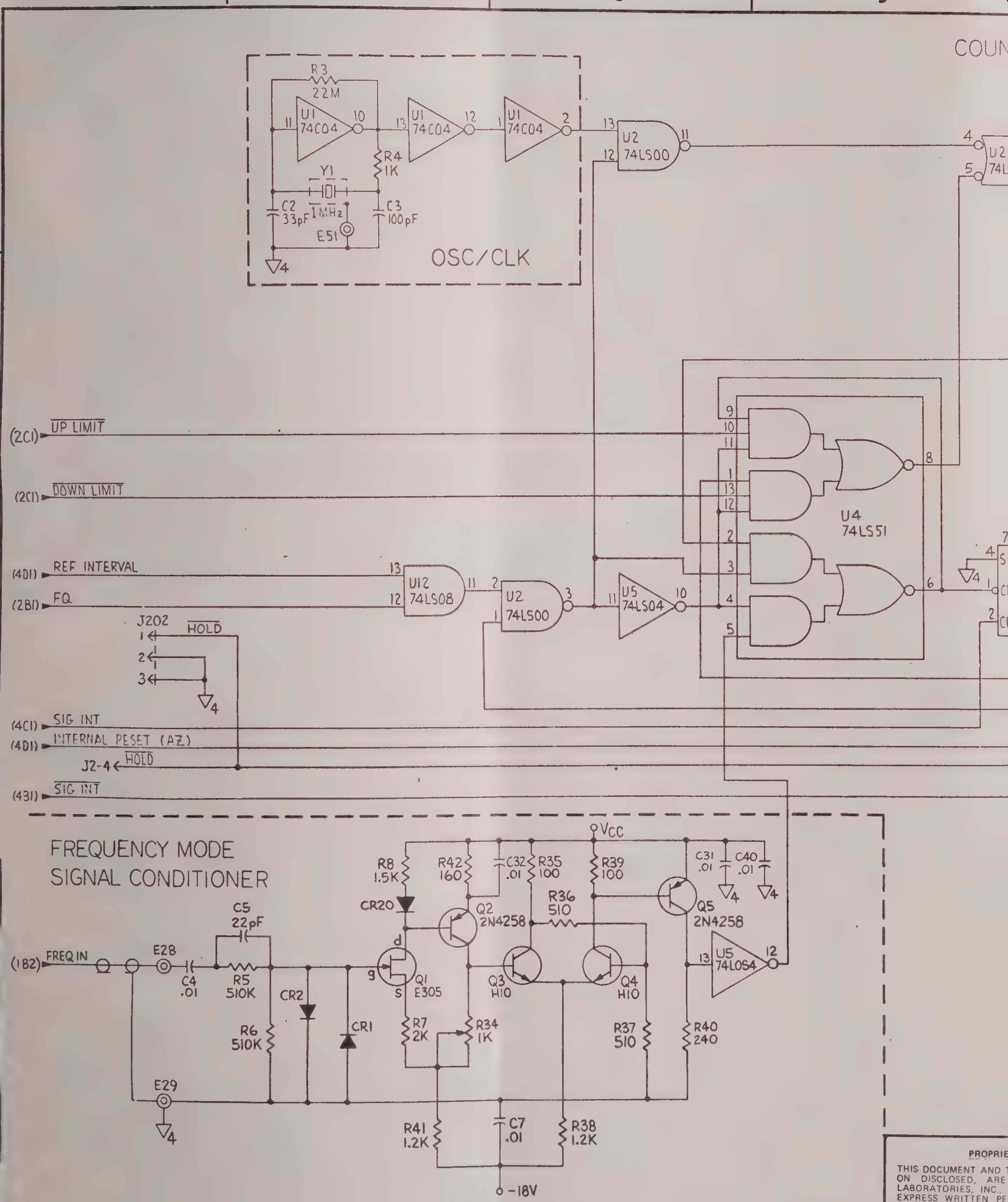
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC-
MAIN LOGIC & INTERCONNECT
5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432095	-

SCALE SHEET 2 OF 5




COUN
R3
22M
U1
74C04
11
10
13
12
1
2
R4
1K
Y1
1MHz
C2
33pF
C3
100pF
E51
OSC/CLK
U2
74LS00
13
12
11
4
5
U2
74L
(2C1) UP LIMIT
(2C1) DOWN LIMIT
(4D1) REF INTERVAL
(2B1) FQ
U12
74LS08
U2
74LS00
U5
74LS04
U4
74LS51
9
10
11
1
13
12
2
3
4
5
8
6
7
J202
1
2
3
HOLD
(4C1) SIG INT
(4D1) INTERNAL PESET (AZ)
J2-4 HOLD
(431) SIG INT
FREQUENCY MODE
SIGNAL CONDITIONER
(1B2) FREQ IN
E28
C5
22pF
C4
.01
R5
510K
R6
510K
CR2
CR1
E29
R8
1.5K
CR20
R42
160
C32
.01
R35
100
R39
100
VCC
C31
.01
C40
.01
Q2
2N4258
R36
510
Q5
2N4258
Q1
E305
d
g
s
Q3
H10
Q4
H10
U5
74LS04
13
12
R7
2K
R34
1K
R37
510
R40
240
R41
1.2K
C7
.01
R38
1.2K
-18V
8
7
6
5

PROPRIE

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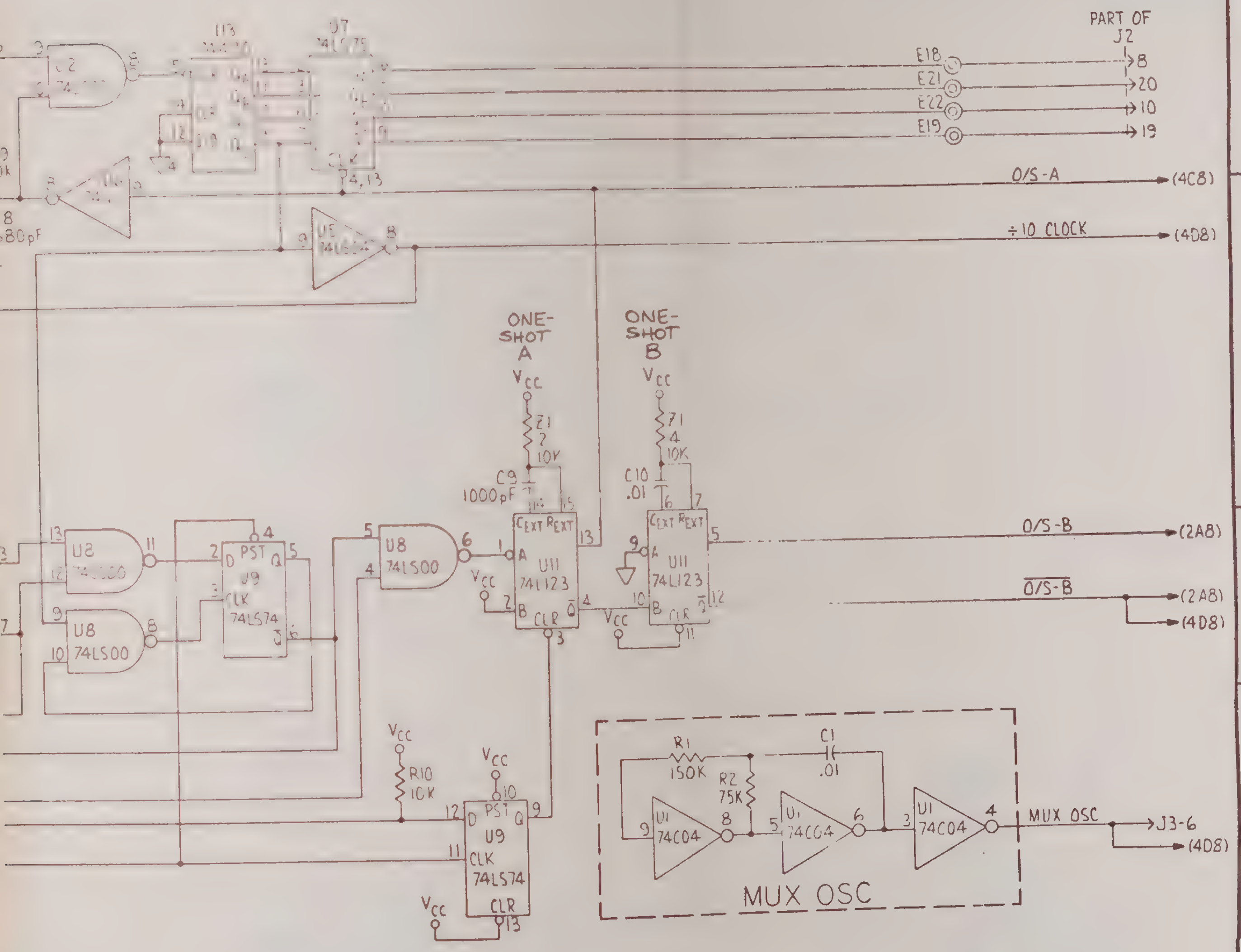
ON DISCLOSED, ARE
LABORATORIES, INC.,
EXPRESS WRITTEN PE
RATORIES, INC. BE USE
IN WHOLE OR IN PART,
TIONS FROM A COMPET
MANUFACTURE BY AN
LABORATORIES, INC.
HAS BEEN DEVELOPED
MAY ONLY BE USED FOR
EVALUATION AND F
TECHNICAL SPECIFICA
MENTS WHICH SPECIFY P
FROM DANA LABORATO

NOTES: UNLESS OTHERWISE SPECIFIED

4 3 2 1

& CONTROL

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			



PART OF J2
E18
E21
E22
E19
8
20
10
19
U2
74LS00
U3
74LS90
U7
74LS75
U4
74LS04
U6
74LS04
CLK
4,13
O/S-A
(4C8)
÷10 CLOCK
(4D8)
ONE-SHOT A
ONE-SHOT B
Vcc
Z1
2
10K
Z1
4
10K
C9
1000pF
C10
.01
CEXT REXT
U11
74LS123
A
B
CLR
Q
$\overline{Q}$
U8
74LS00
U9
74LS74
PST
D
Q
CLK
CLR
$\overline{Q}$
O/S-B
(2A8)
$\overline{O/S-B}$
(2A8)
(4D8)
R10
10K
R1
150K
R2
75K
C1
.01
U1
74C04
MUX OSC
J3-6
(4D8)
680pF

NOTICE

…HNICAL DATA HERE-
…IETARY TO DANA
…ALL NOT, WITHOUT
…N OF DANA LABO
…ASED OR DISCLOSED
… TO SOLICIT QUOTA
…URCE OR USED FOR
…THER THAN DANA
…ORMATION HEREON
…ATE EXPENSE, AND
…IES OF ENGINEERING
…ORPORATION INTO
…ND OTHER DOCU-
…MENT OF PRODUCTS

403907	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X 030 XX.020 XXX.010	0 30' FORMED 1° 0'	+ .004 - .001

DIMENSIONS AND TOLERANCES PER USAS Y14 15

MATERIAL	FINISH

DRAWN	Rich Mays	4-19-77
CHECK	W. STANTON	[illegible] 77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

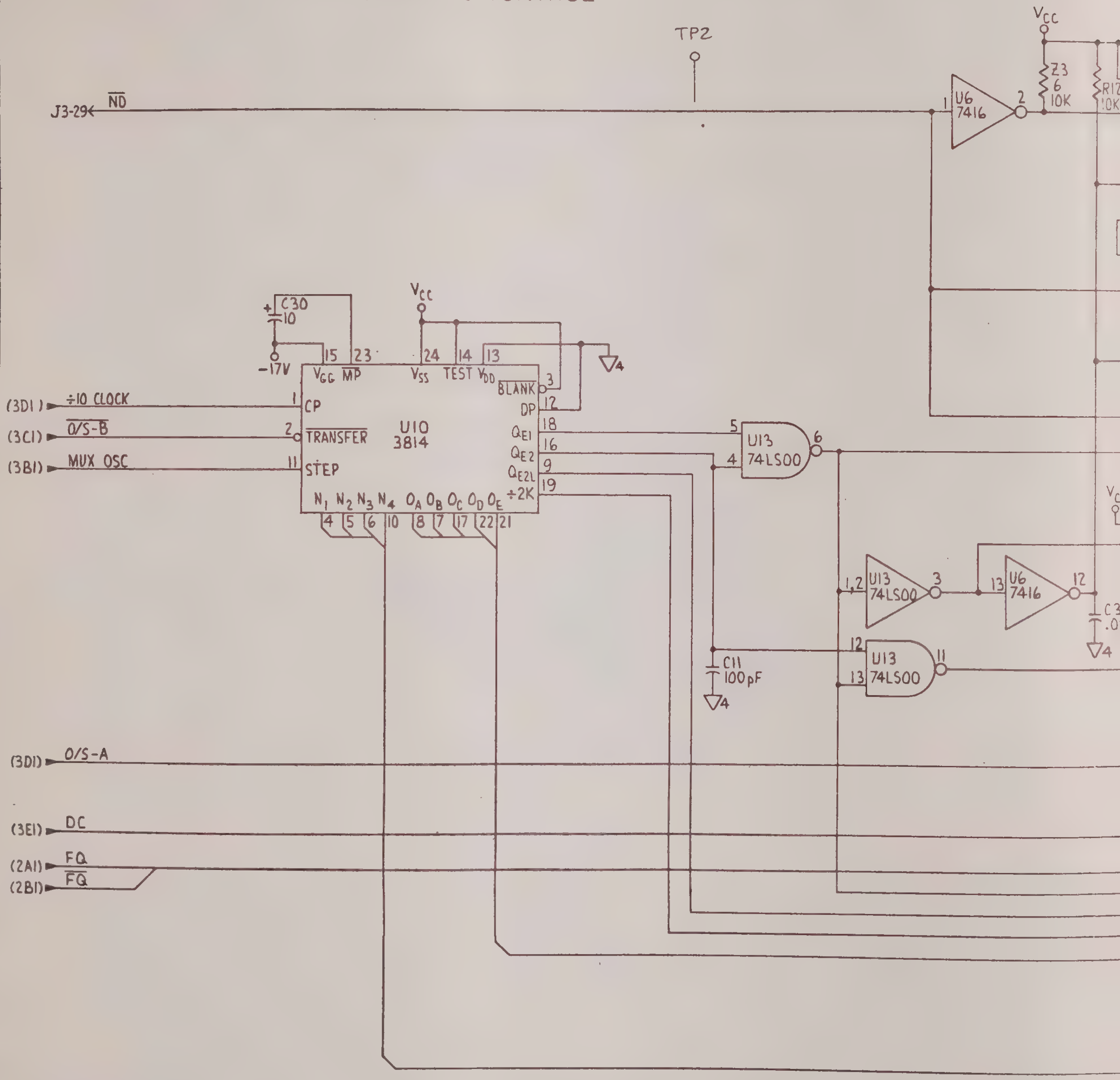
SCHEMATIC -
MAIN LOGIC & INTERCONNECT
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432095	F

SCALE

SHEET 3 OF 5

COUNTER & CONTROL


J3-29
ND
TP2
VCC
U6
7416
Z3
6
10K
R12
10K
C30
10
-17V
VGG
MP
VSS
TEST
VDD
BLANK
DP
(3D1) ÷10 CLOCK
(3C1) O/S-B
(3B1) MUX OSC
CP
TRANSFER
STEP
U10
3814
QE1
QE2
QE2L
÷2K
N1 N2 N3 N4
OA OB OC OD OE
U13
74LS00
C11
100pF
(3D1) O/S-A
(3E1) DC
(2A1) FQ
(2B1) FQ

NOTES: UNLESS OTHERWISE SPECIFIED

PROPR
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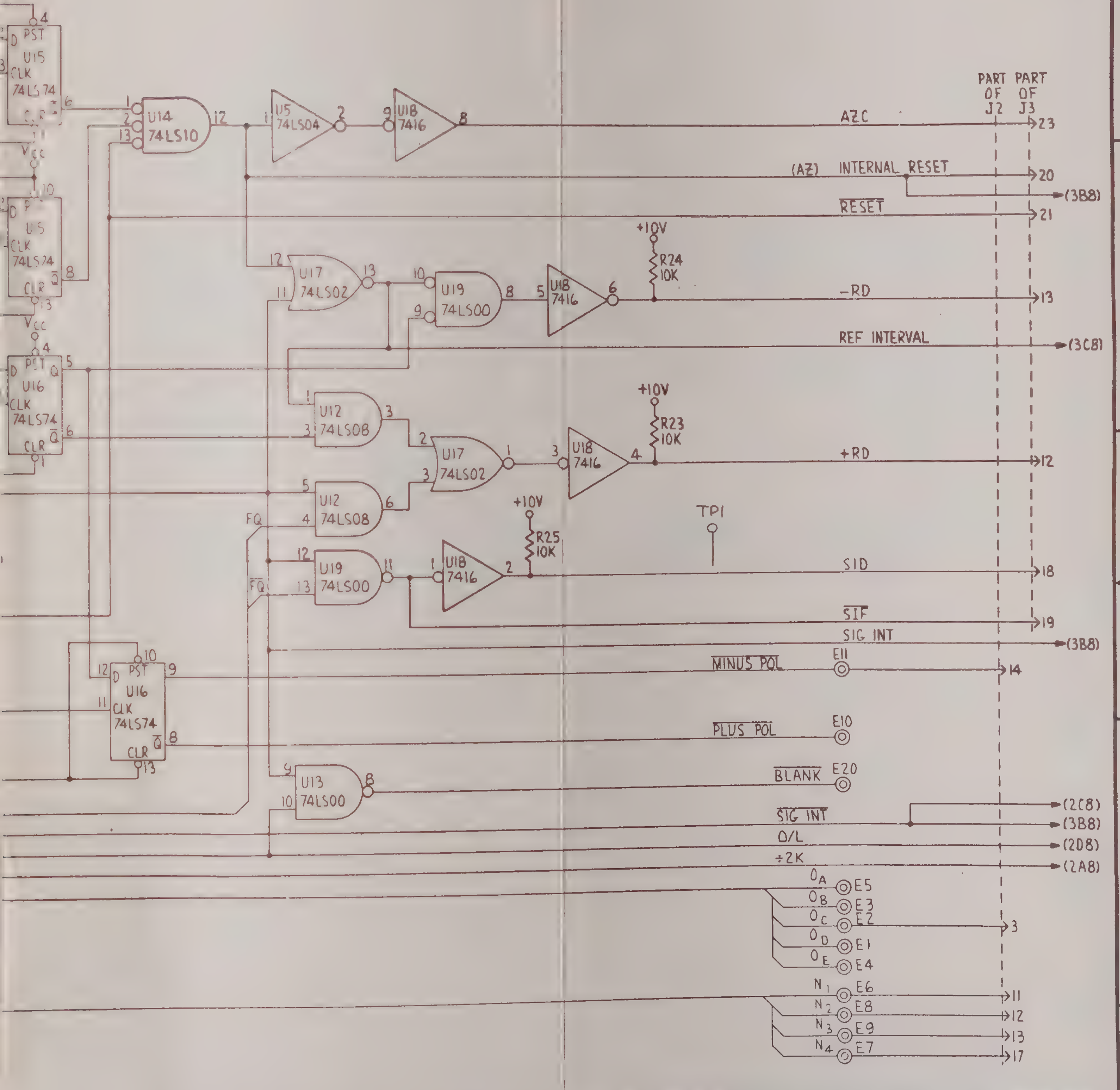
ON DISCLOSED, AR
LABORATORIES, INC
EXPRESS WRITTEN
RATORIES, INC. BE U
IN WHOLE OR IN PAR
TIONS FROM A COMP
MANUFACTURE BY
LABORATORIES, INC.
HAS BEEN DEVELOP
MAY ONLY BE USED F
EVALUATION AND
TECHNICAL SPECIFI
MENTS WHICH SPECIF
FROM DANA LABORA

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			



4
3
2
1
E
D
C
B
A
U15
74LS74
PST
D
CLK
CLR
U14
74LS10
U5
74LS04
U18
7416
AZC
PART OF J2
PART OF J3
23
(AZ) INTERNAL RESET
20
(3B8)
RESET
21
+10V
R24
10K
U17
74LS02
U19
74LS00
-RD
13
REF INTERVAL
(3C8)
U16
74LS74
U12
74LS08
R23
10K
+RD
12
FQ
R25
10K
TP1
SID
18
SIF
19
SIG INT
(3B8)
MINUS POL
E11
14
PLUS POL
E10
U13
74LS00
BLANK
E20
SIG INT
(2C8)
(3B8)
O/L
(2D8)
÷2K
(2A8)
0_A E5
0_B E3
0_C E2
3
0_D E1
0_E E4
N_1 E6
11
N_2 E8
12
N_3 E9
13
N_4 E7
17
VCC

IETARY NOTICE

THE TECHNICAL DATA HERE-
E PROPRIETARY TO DANA
AND SHALL NOT, WITHOUT
ERMISSION OF DANA LABO-
IED, RELEASED OR DISCLOSED
, OR USED TO SOLICIT QUOTA-
TITIVE SOURCE OR USED FOR
NYONE OTHER THAN DANA
THE INFORMATION HEREON
D AT PRIVATE EXPENSE, AND
OR PURPOSES OF ENGINEERING
FOR INCORPORATION INTO
ATIONS AND OTHER DOCU-
PROCUREMENT OF PRODUCTS
ORIES, INC.

403907	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

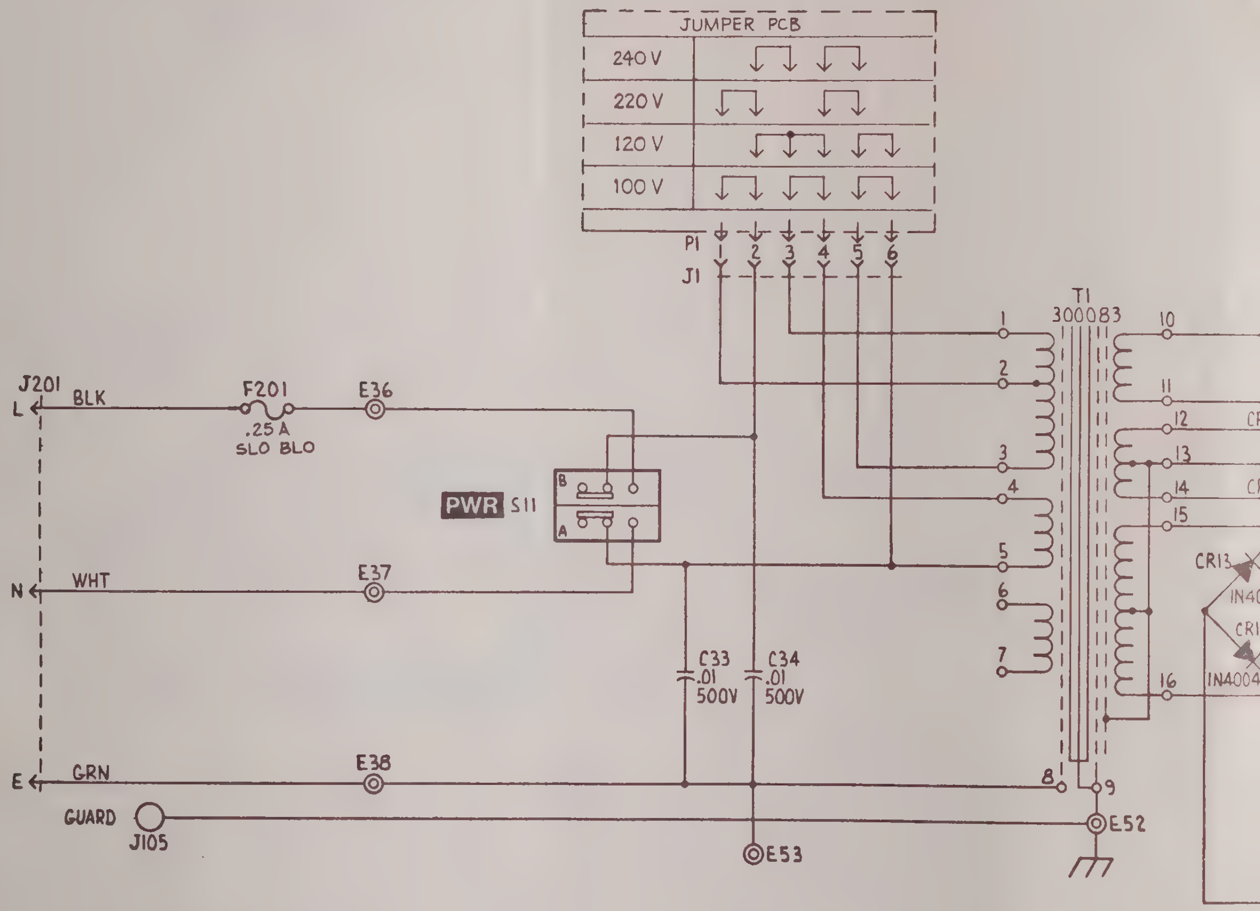
DRAWN	Rich Mays	4-21-77
CHECK	W. STANTON	10-12-77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432095	F

SCALE | SHEET 4 OF 5


JUMPER PCB
240 V
220 V
120 V
100 V
P1
2
3
4
5
6
J1
T1
300083
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
CR13
IN40
CR1
IN4004
J201
L
BLK
F201
.25 A
SLO BLO
E36
PWR S11
B
A
N
WHT
E37
C33
.01
500V
C34
.01
500V
E
GRN
E38
GUARD
J105
E52
E53
E
D
C

POW		
	+18V	+1
J2		
J3	28	1
J4	9	
J5	13	1
E5	50	

B

A

7. SYMBOL ▽1 DENOTES REF GND (MECCA)
   ▽2 ANALOG GND
   ▽3 REF GND
   ▽4 DIGITAL GND

⚠6 R22, R26 AND R27 ARE FSV SET 020688 AND MAY BE CONFIGURED AS SHOW IN AS SHOWN A, B OR C

4. ALL SWITCHES AND RELAYS SHOWN IN DEENERGIZED POSITION
3. DIODES ARE IN916B
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4 W

NOTES: UNLESS OTHERWISE SPECIFIED

PROP

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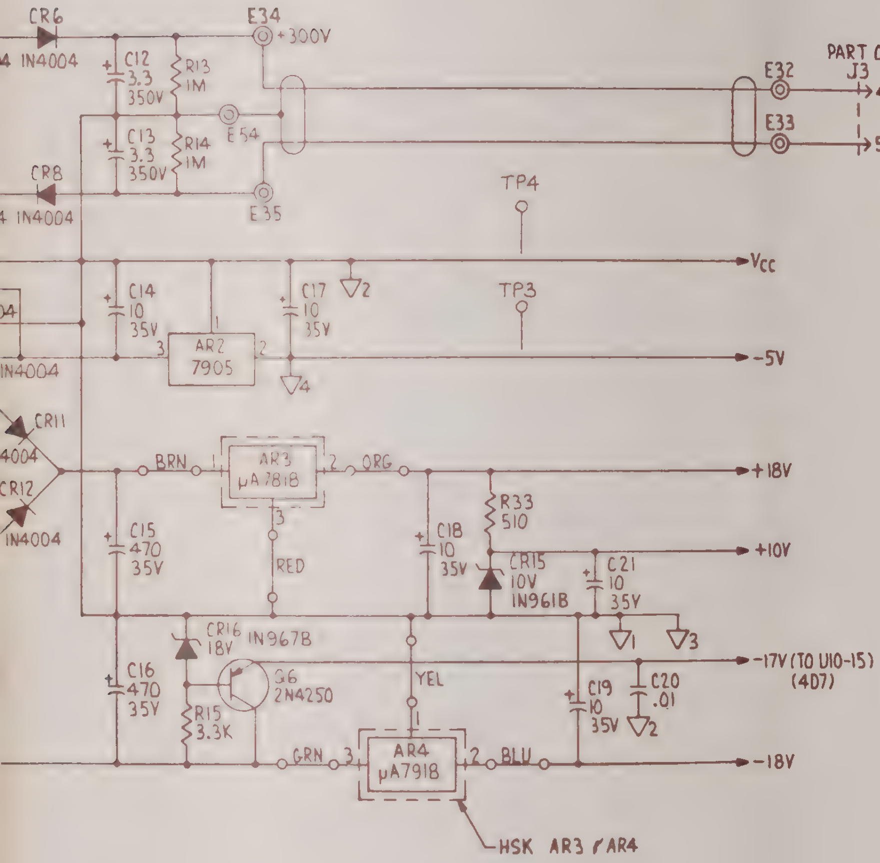
ON DISCLOSED, A
LABORATORIES, INC
EXPRESS WRITTEN
RATORIES, INC. BE
IN WHOLE OR IN PA
TIONS FROM A COM
MANUFACTURE BY
LABORATORIES, INC
HAS BEEN DEVELOP
MAY ONLY BE USED
EVALUATION AND
TECHNICAL SPECIF
MENTS WHICH SPECI
FROM DANA LABORA

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			



CR6
4 IN4004
E34
+300V
C12
3.3
350V
R13
1M
C13
3.3
350V
R14
1M
E54
CR8
4 IN4004
E35
PART OF
J3
E32
4
E33
5
TP4
Vcc
C14
10
35V
C17
10
35V
▽2
TP3
04
AR2
7905
IN4004
▽4
-5V
CR11
4004
CR12
IN4004
BRN
AR3
μA7818
ORG
+18V
R33
510
C15
470
35V
RED
C18
10
35V
CR15
10V
IN961B
C21
10
35V
+10V
▽1
▽3
CR16
18V
IN967B
C16
470
35V
Q6
2N4250
R15
3.3K
YEL
C19
10
35V
C20
.01
▽2
-17V (TO U10-15)
(4D7)
GRN
AR4
μA7918
BLU
-18V
HSK AR3 / AR4

ISTRIBUTION

18V	▽1	▽2	▽3	▽4(-5V)
	9			18
27	3	26	30	22
7	8		3	2
11	14			3
	23			17

Y NOTICE

TECHNICAL DATA HERE-
OPRIETARY TO DANA
SHALL NOT, WITHOUT
SION OF DANA LABO-
ELEASED OR DISCLOSED
JSED TO SOLICIT QUOTA-
E SOURCE OR USED FOR
E OTHER THAN DANA
INFORMATION HEREON
PRIVATE EXPENSE, AND
POSES OF ENGINEERING
INCORPORATION INTO
S AND OTHER DOCU-
UREMENT OF PRODUCTS
, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403907	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL — FINISH

DRAWN	Rich Mays	4-22-77
CHECK	W. STANTON	10-12-77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC–
MAIN LOGIC & INTERCONNECT
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432095	F

SCALE — SHEET 5 OF 5

6-10

PROPRIETARY NOTICE

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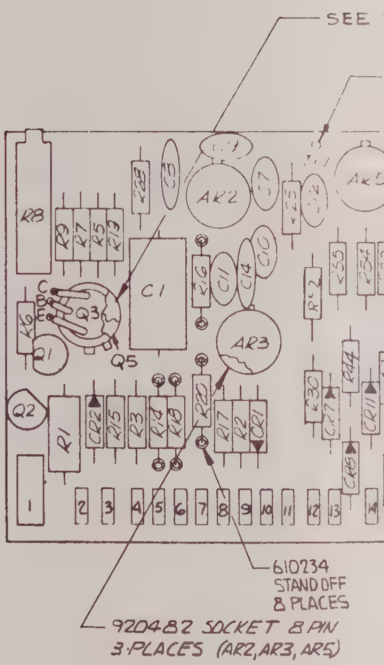
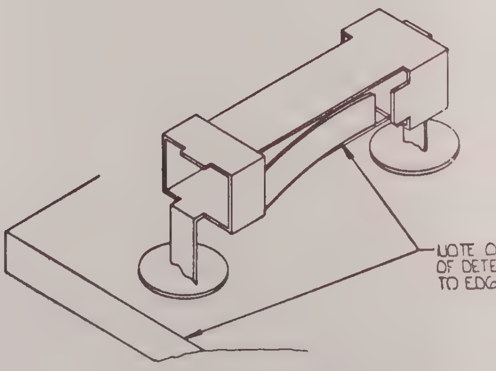

SEE
R8
R9
R7
R5
R13
R28
C3
C4
AR2
C7
R25
C12
AR5
C1
C
B
E
Q3
R16
Q1
Q5
R16
C11
C14
C10
R52
R35
R54
AR3
R44
R30
CR7
CR11
Q2
R1
CR2
R15
R3
R14
R18
R20
R17
R2
CR1
CR6
1
2
3
4
5
6
7
8
9
10
11
12
13
14
610234
STAND OFF
8 PLACES
920482 SOCKET 8 PIN
3 PLACES (AR2, AR3, AR5)


NOTE O
OF DETE
TO EDG

DETAIL "A"

△7 R34, R35 & R37 ARE A MATCHED SET 020678.

△6 R47 & R49 ARE A MATCHED SET 020675.

△5 CEMENT Q3 TO Q5 WITH WASHER 610625 BETWEEN THEM WITH EASTMAN 910 (920008).

△4 CR10, R41, R58 ARE PART OF 403942 ZENER KIT

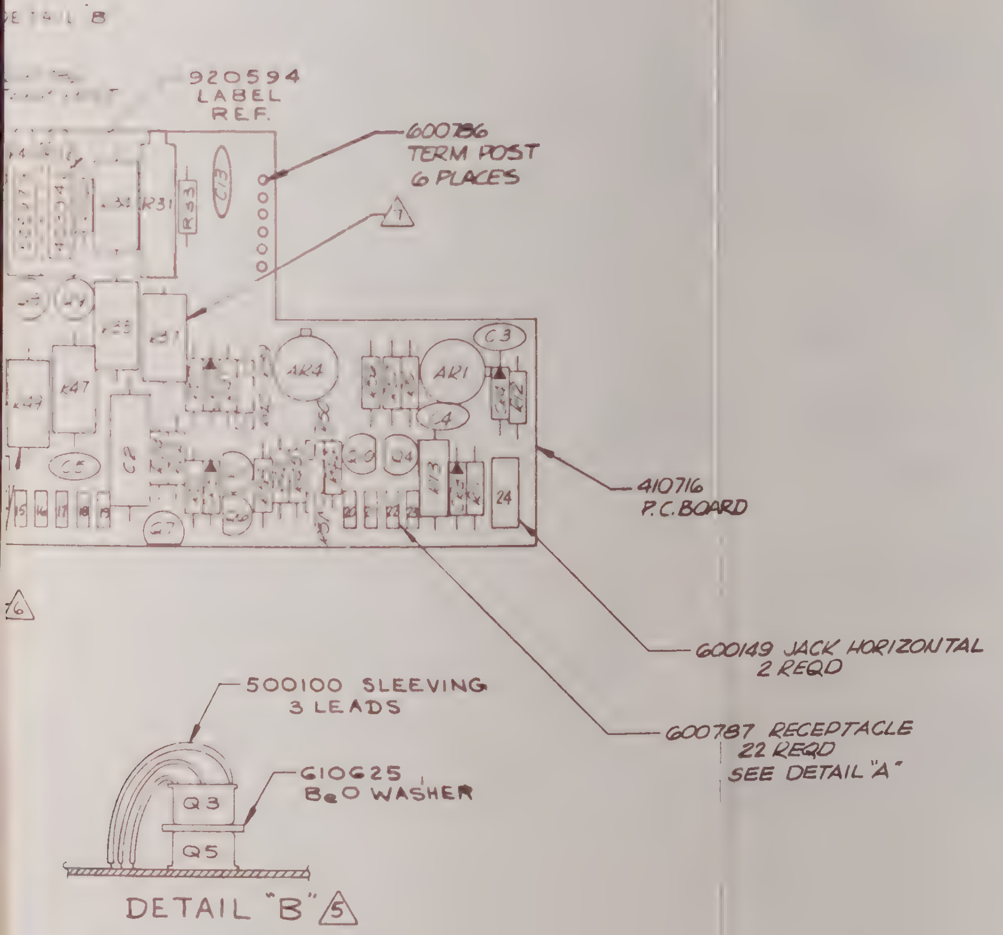
3. SCHEMATIC REF 432074

2. CAPACITORS ARE IN µF

1. RESISTORS ARE IN OHMS, 1/4 W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1121 4/13/76	[illegible]		[illegible]
	B	REVISED PER E.O 10219	KAM 10.11.76		12 [illegible] 76 J Koch
	C	10267	KAM 10.11.76		
	D	10307	KAM 10.11.76		
	E	10378	KAM 10.11.76		
	F	10576	KAM 10.11.76		
	H	10716	KAM 10.11.76		
	J	10772	ZR 12-20-76		12-20-76 J Koch
	K	10788	Z.B 12-23-76		
D	L	REVISED PER EO 10809	ZB 1/10/77	1-10-77	J Koch
	M	REVISED PER EO 10829	ZB 1/10/77	1-10-77	J Koch
F	N	REVISED PER EO 10848	ARING 3/1/77	3-1-77	J Koch
	P	ADDED STANDOFF PER EO 10861	Z.B. 3/1/77	3-7-77	J. Koch
	R	REVISED PER EO 11029			



ETAIL B
920594
LABEL
REF.
600786
TERM POST
6 PLACES
7
R31
R33
C13
R33
R31
AR4
AR1
C3
C4
R47
R49
C5
C2
C7
Q3
Q4
R13
R12
24
15
16
17
18
19
20
21
22
23
410716
P.C. BOARD
6
600149 JACK HORIZONTAL
2 REQD
500100 SLEEVING
3 LEADS
600787 RECEPTACLE
22 REQD
SEE DETAIL "A"
610625
BeO WASHER
Q3
Q5
DETAIL "B" 5

ENTATION
T IN REF.
OF BOARD

403908	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X 030 XX.020 XXX 010	ANGLES 0° 30′ FORMED 1°.0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

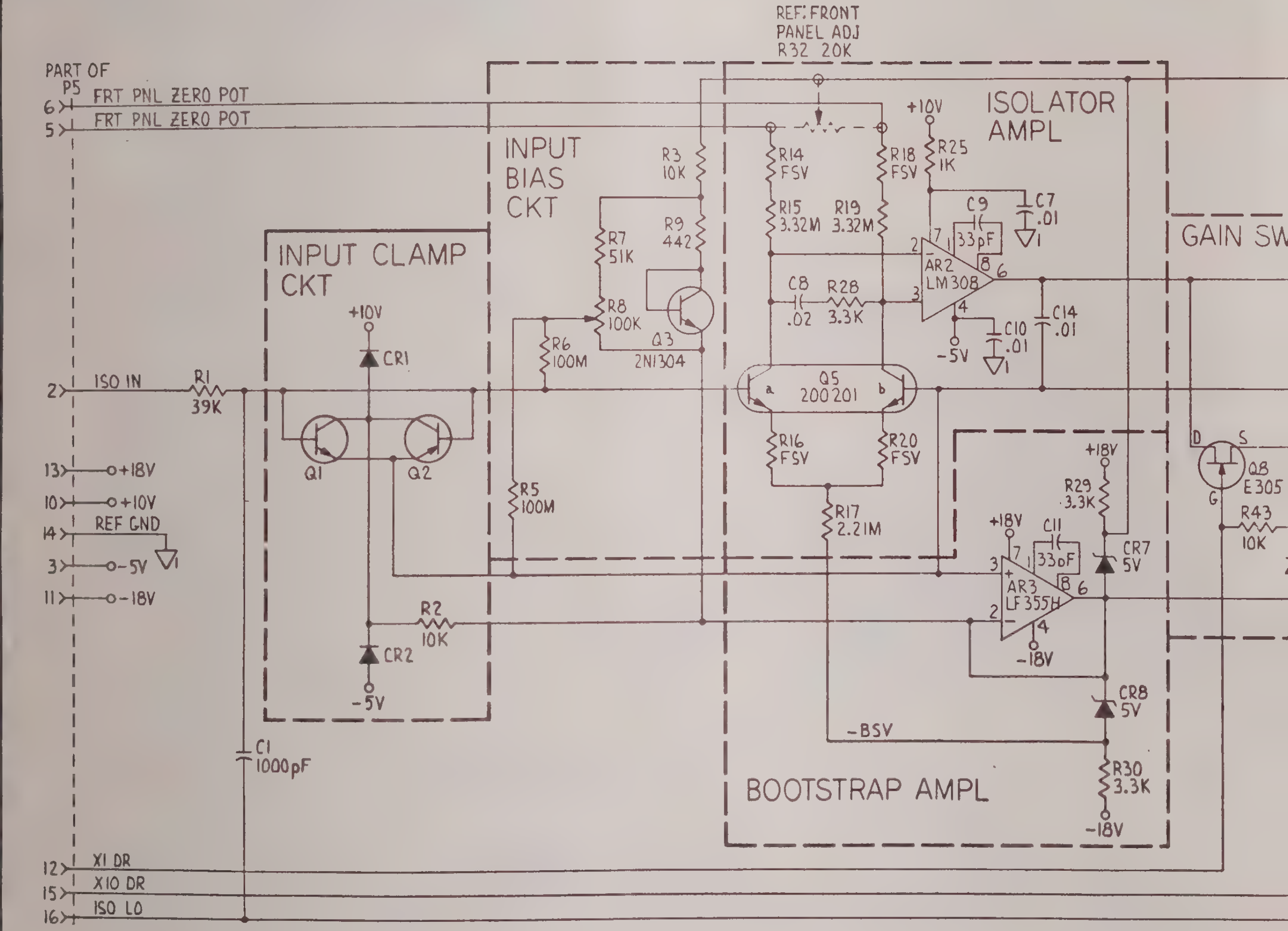
DRAWN	[illegible]	1/20/76
CHECK		
DESIGN	[illegible]	3/2 76
MECH ENGR		
PROJ ENGR	[illegible]	4/13/76
PROD ENGR		4/13/[illegible]

DANA ®
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PC BOARD ASSY
REFERENCE-ISOLATOR
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403847	R

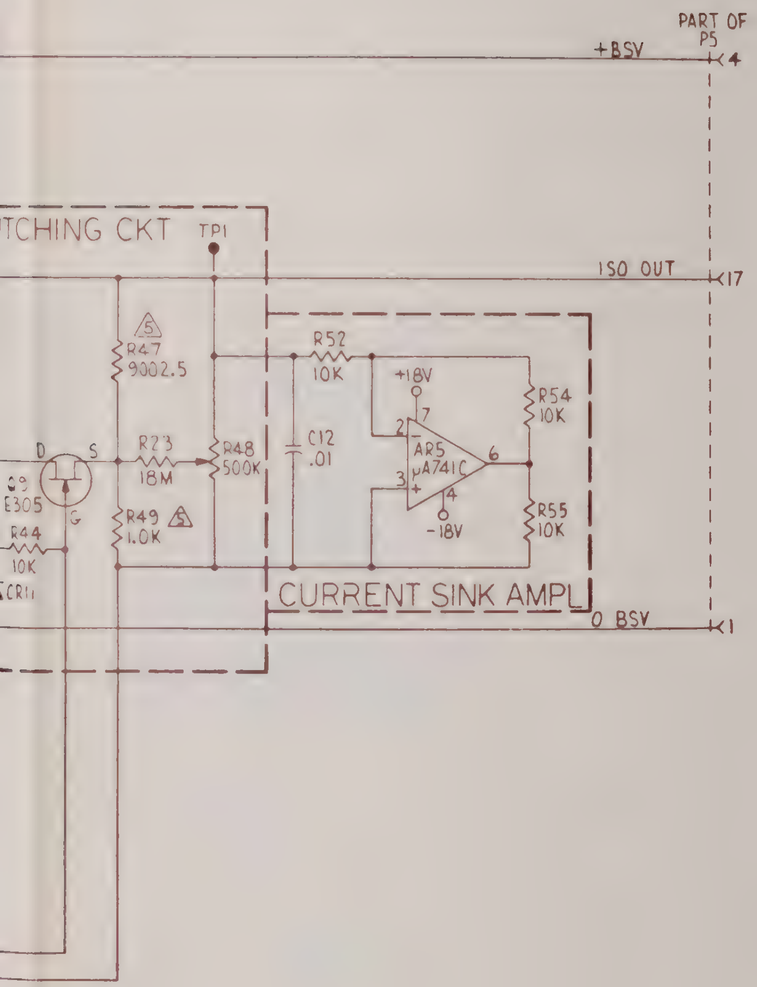
SCALE 2/1 SHEET 1 OF 6


REF: FRONT PANEL ADJ R32 20K
PART OF P5
6 FRT PNL ZERO POT
5 FRT PNL ZERO POT
2 ISO IN
R1 39K
13 +18V
10 +10V
14 REF GND
3 -5V
11 -18V
12 X1 DR
15 X10 DR
16 ISO LO
C1 1000pF
INPUT CLAMP CKT
+10V
CR1
Q1
Q2
R2 10K
CR2
-5V
INPUT BIAS CKT
R3 10K
R9 442
R7 51K
R8 100K
Q3 2N1304
R6 100M
R5 100M
ISOLATOR AMPL
R14 FSV
R15 3.32M
R18 FSV
R19 3.32M
+10V
R25 1K
C9 33pF
C7 .01
AR2 LM308
C8 .02
R28 3.3K
C10 .01
C14 .01
-5V
Q5 200201
a
b
R16 FSV
R20 FSV
R17 2.21M
+18V
R29 3.3K
C11 33pF
AR3 LF355H
CR7 5V
CR8 5V
-18V
-BSV
R30 3.3K
-18V
BOOTSTRAP AMPL
GAIN SW
D S G
Q8 E305
R43 10K

7△ ZENER REF KIT 403942
6△ MATCHED RESISTOR SET 020678
5△ MATCHED RESISTOR SET 020675
4. TRANSISTORS ARE 200200
3. DIODES ARE IN916B
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

PROP
THIS DOCUMENT AND
ON DISCLOSED, ARE
LABORATORIES, INC.,
EXPRESS WRITTEN P
RATORIES, INC. BE US
IN WHOLE OR IN PART
TIONS FROM A COMPE
MANUFACTURE BY A
LABORATORIES, INC.
HAS BEEN DEVELOPE
MAY ONLY BE USED FO
EVALUATION AND
TECHNICAL SPECIFIC
MENTS WHICH SPECIFY
FROM DANA LABORAT

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	C	RELEASED PER DRN #			
	—	PEDRAWN WITHOUT CHANGE	PA 10-12-77		
	D	REVISED PER EO 11029	PA 10-12-77		
	E	REVISED PER EO 11350	PA 10-12-77		


PART OF P5
+BSV
4
TCHING CKT
TP1
ISO OUT
17
5
R47
9002.5
R52
10K
+18V
R54
10K
7
2
AR5
μA741C
6
3
4
-18V
R55
10K
C12
.01
D
S
R23
18M
R48
500K
Q9
E305
G
R44
10K
CR11
R49
1.0K
5
CURRENT SINK AMPL
0 BSV
1

ARY NOTICE

IE TECHNICAL DATA HERE-
PROPRIETARY TO DANA
ND SHALL NOT, WITHOUT
MISSION OF DANA LABO
RELEASED OR DISCLOSED
R USED TO SOLICIT QUOTA-
TIVE SOURCE OR USED FOR
ONE OTHER THAN DANA
HE INFORMATION HEREON
AT PRIVATE EXPENSE, AND
PURPOSES OF ENGINEERING
R INCORPORATION INTO
ONS AND OTHER DOCU-
OCUREMENT OF PRODUCTS
IES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403847	5100		

APPLICATION — QTY REQD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X 030 XX.020 XXX.010	0' 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL — FINISH

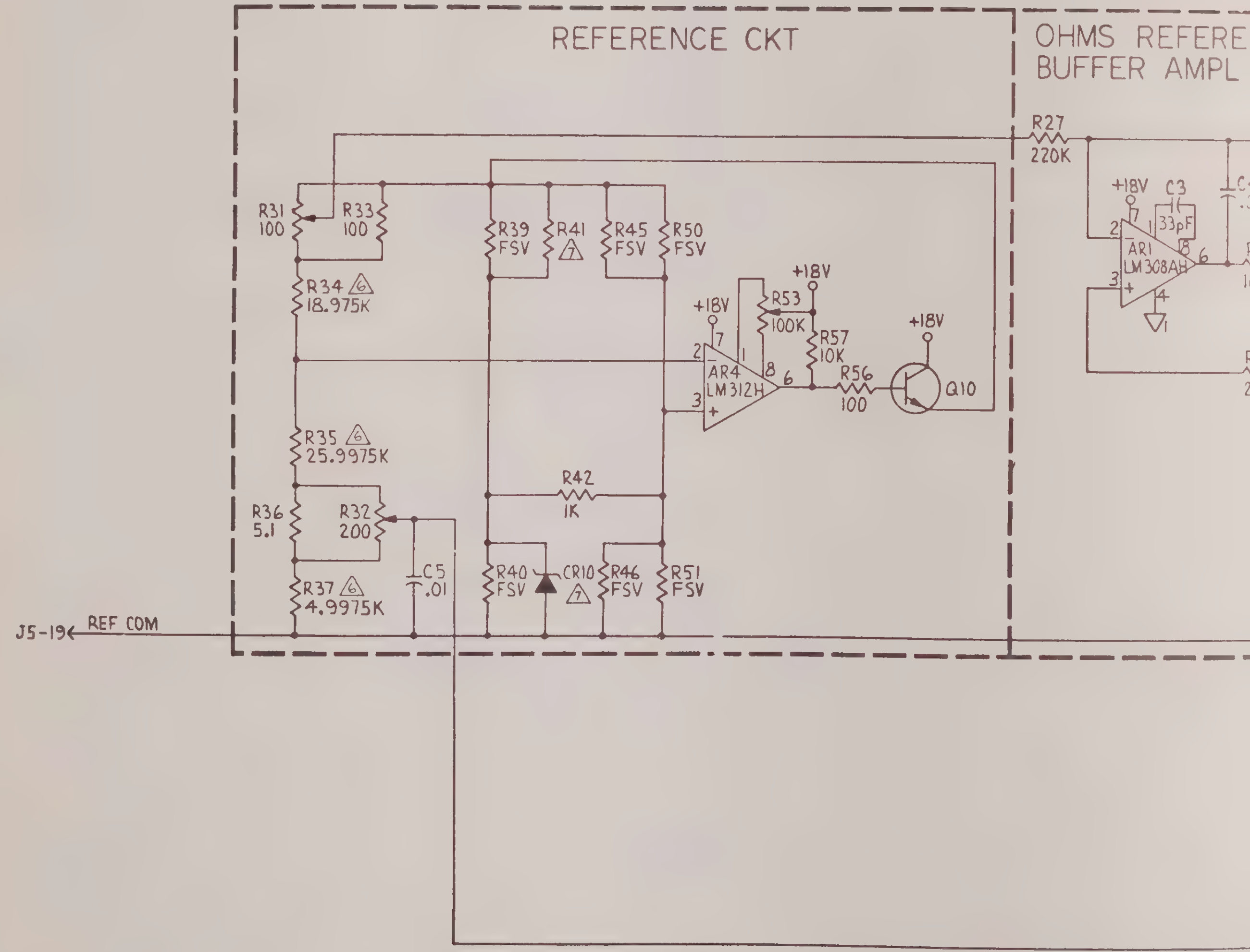
DRAWN	Rich Mays	5-16-77
CHECK	W. Tranter	6-17-77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

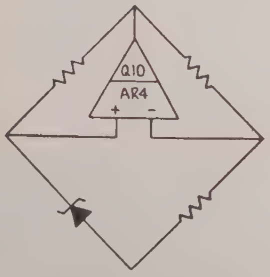
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC–
REFERENCE ISOLATOR
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432074	

SCALE — SHEET 1 OF 7


REFERENCE CKT
OHMS REFERE
BUFFER AMPL
R27
220K
+18V
C3
33pF
AR1
LM308AH
R31
100
R33
100
R39
FSV
R41
7
R45
FSV
R50
FSV
R34 6
18.975K
+18V
R53
100K
R57
10K
AR4
LM312H
R56
100
Q10
R35 6
25.9975K
R42
1K
R36
5.1
R32
200
C5
.01
R37 6
4.9975K
R40
FSV
CR10
7
R46
FSV
R51
FSV
J5-19
REF COM



REF BRIDGE CKT
SIMPLIFIED DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

PROPI
THIS DOCUMENT AN
ON DISCLOSED, AI
LABORATORIES, INC
EXPRESS WRITTEN
RATORIES, INC. BE U
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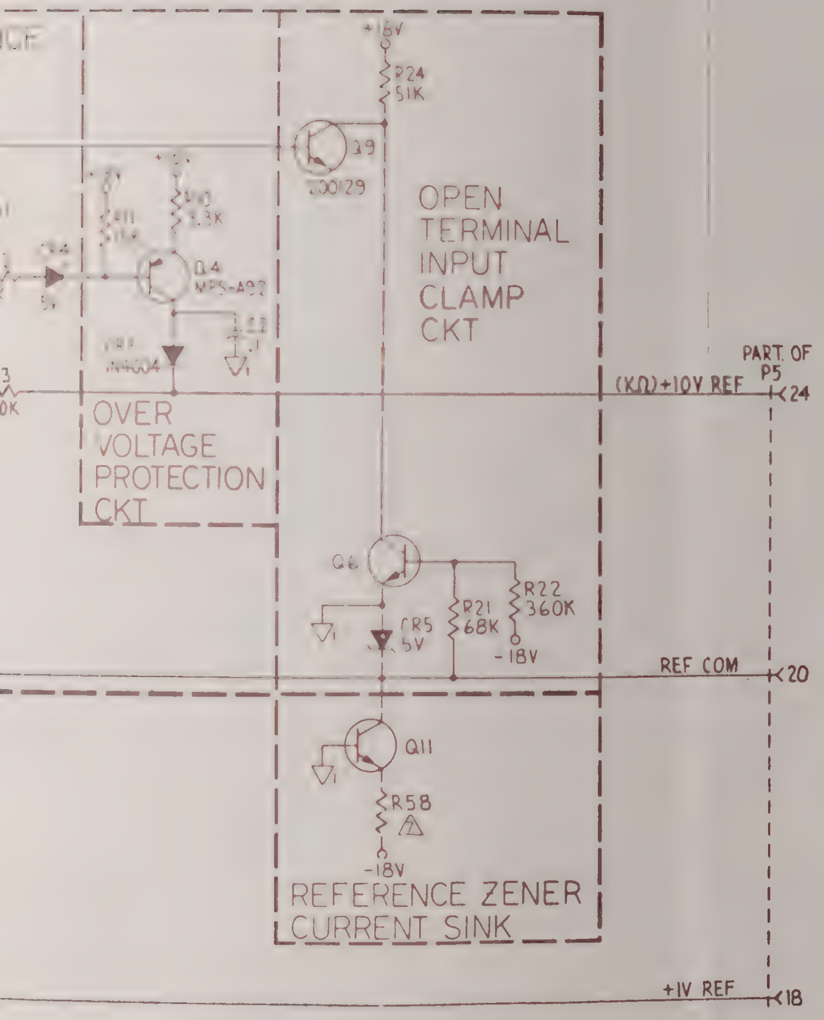
TIONS FROM A COMP
MANUFACTURE BY
LABORATORIES, INC
HAS BEEN DEVELOP
MAY ONLY BE USED F
EVALUATION AND
TECHNICAL SPECIFI
MENTS WHICH SPEC.F
FROM DANA LABORA

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			



+18V
R24
51K
Q9
200129
OPEN
TERMINAL
INPUT
CLAMP
CKT
R11
R10
Q4
MPS-A92
CR4
5V
CR1
1N4004
C22
.1
3
0K
OVER
VOLTAGE
PROTECTION
CKT
PART. OF
P5
(KΩ)+10V REF
24
Q6
R22
360K
R21
68K
CR5
5V
-18V
REF COM
20
Q11
R58
-18V
REFERENCE ZENER
CURRENT SINK
+1V REF
18

ETARY NOTICE

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PROPRIETARY TO DANA
AND SHALL NOT, WITHOUT
ERMISSION OF DANA LABO-
ED, RELEASED OR DISCLOSED
OR USED TO SOLICIT QUOTA
TITIVE SOURCE OR USED FOR
NYONE OTHER THAN DANA
THE INFORMATION HEREON
AT PRIVATE EXPENSE, AND
R PURPOSES OF ENGINEERING
FOR INCORPORATION INTO
ATIONS AND OTHER DOCU
PROCUREMENT OF PRODUCTS
ORIES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403847	5100		

APPLICATION | QTY REQD

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

DRAWN	Rich Mays	5-17-77
CHECK	W. STANTON	10-12-77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC-
REFERENCE ISOLATOR
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432074	E

SCALE | SHEET 2 OF 2

PROPRIETARY NOTICE

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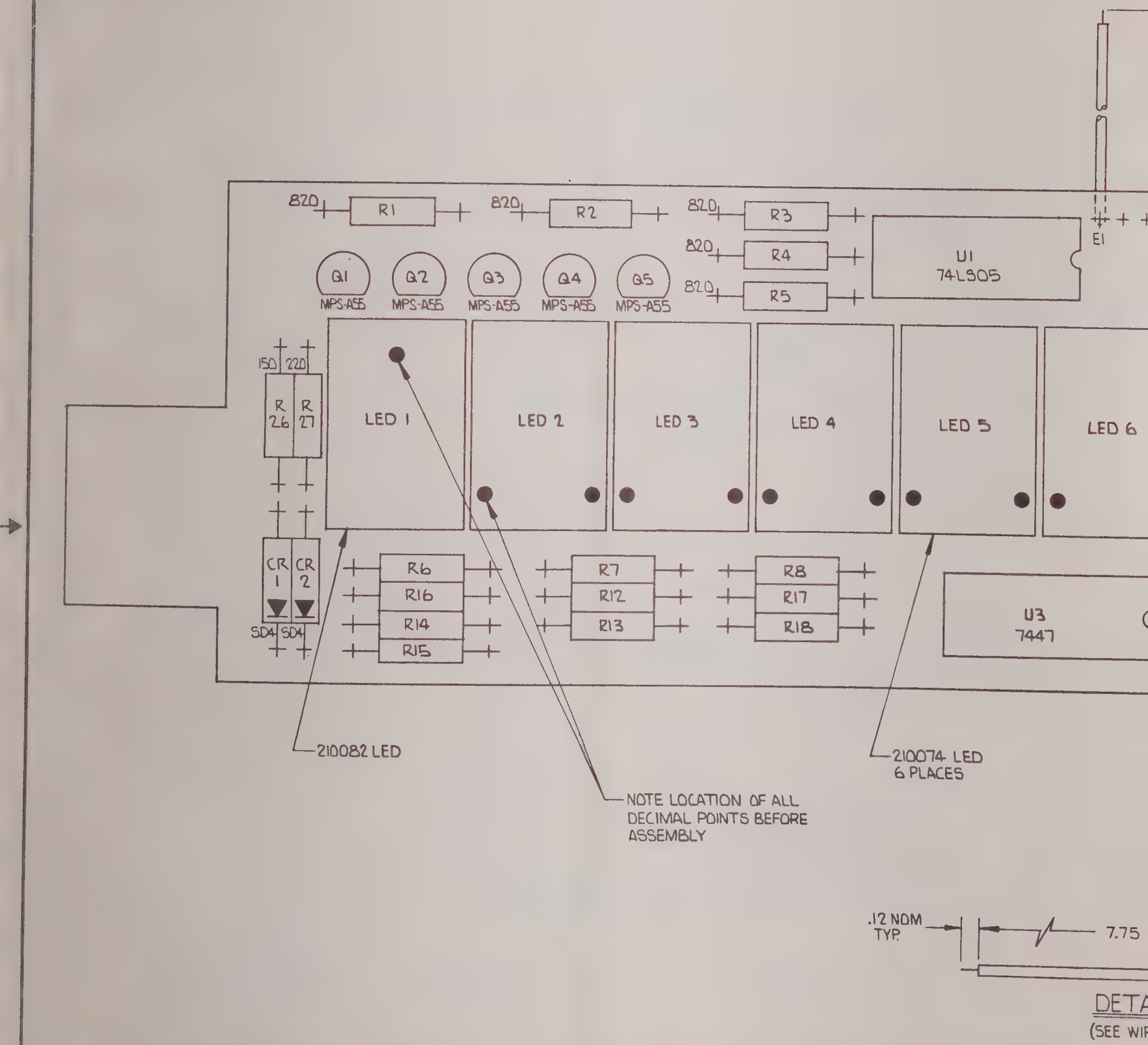
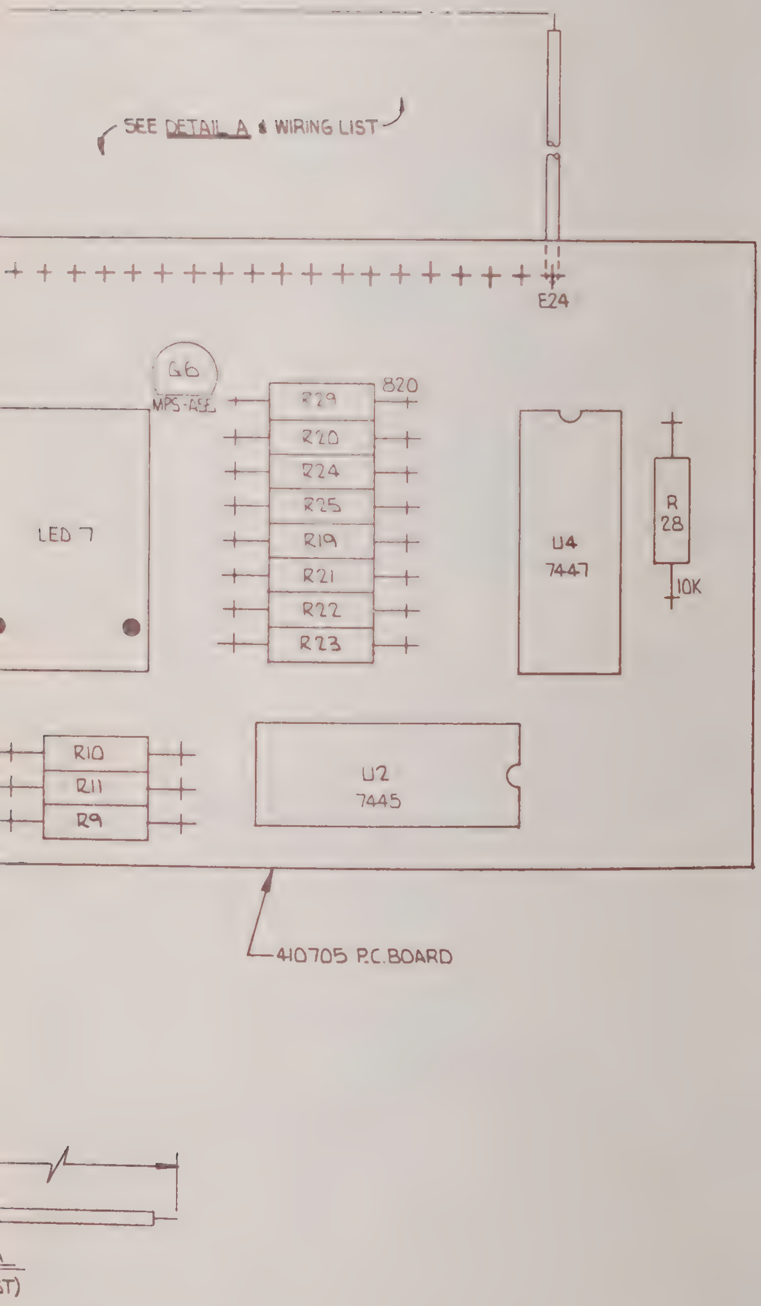

820
R1
820
R2
820
R3
820
R4
820
R5
E1
U1
74LS05
Q1
MPS-A55
Q2
MPS-A55
Q3
MPS-A55
Q4
MPS-A55
Q5
MPS-A55
150
220
R 26
R 27
LED 1
LED 2
LED 3
LED 4
LED 5
LED 6
CR 1
CR 2
SD4
SD4
R6
R16
R14
R15
R7
R12
R13
R8
R17
R18
U3
7447
210082 LED
210074 LED
6 PLACES
NOTE LOCATION OF ALL DECIMAL POINTS BEFORE ASSEMBLY
.12 NOM
TYP.
7.75
DETA
(SEE WIR

6. *FACTORY SELECT VALUE (FSV) OF ALL LED DISPLAYS ON THIS ASSEMBLY TO BE OF THE SAME LUMINOUS INTENSITY CATEGORY. LED 1 MAY BE ±1 CODE LETTER FROM LED 2 THRU LED 6.*
5. *Q1-Q6 TO BE INSTALLED MAX .30 ABOVE P.C. BOARD*
4. R6 THRU R25 ARE 47 Ω.
3. RESISTORS ARE IN OHMS, 5%, ¼W.
2. SCHEMATIC REF. 432076.
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		REVISIONS			
A	A	RELEASED PER DRN #1121 4/13/76	magra		
C	B	NOTCHED BRD. PER ED 10248	ZB 12-17-76		
	C	ADDED WIRE, WIRING LIST & DETAIL A / ED10492			
	D	REVISED NOTE 6 / ED10577			


SEE DETAIL A & WIRING LIST
E24
G6
MPS-A55
820
R29
R20
R24
R25
R19
R21
R22
R23
LED 7
U4
7447
R
28
10K
R10
R11
R9
U2
7445
410705 P.C.BOARD
ST)

403908	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX 020 XXX.010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL | FINISH

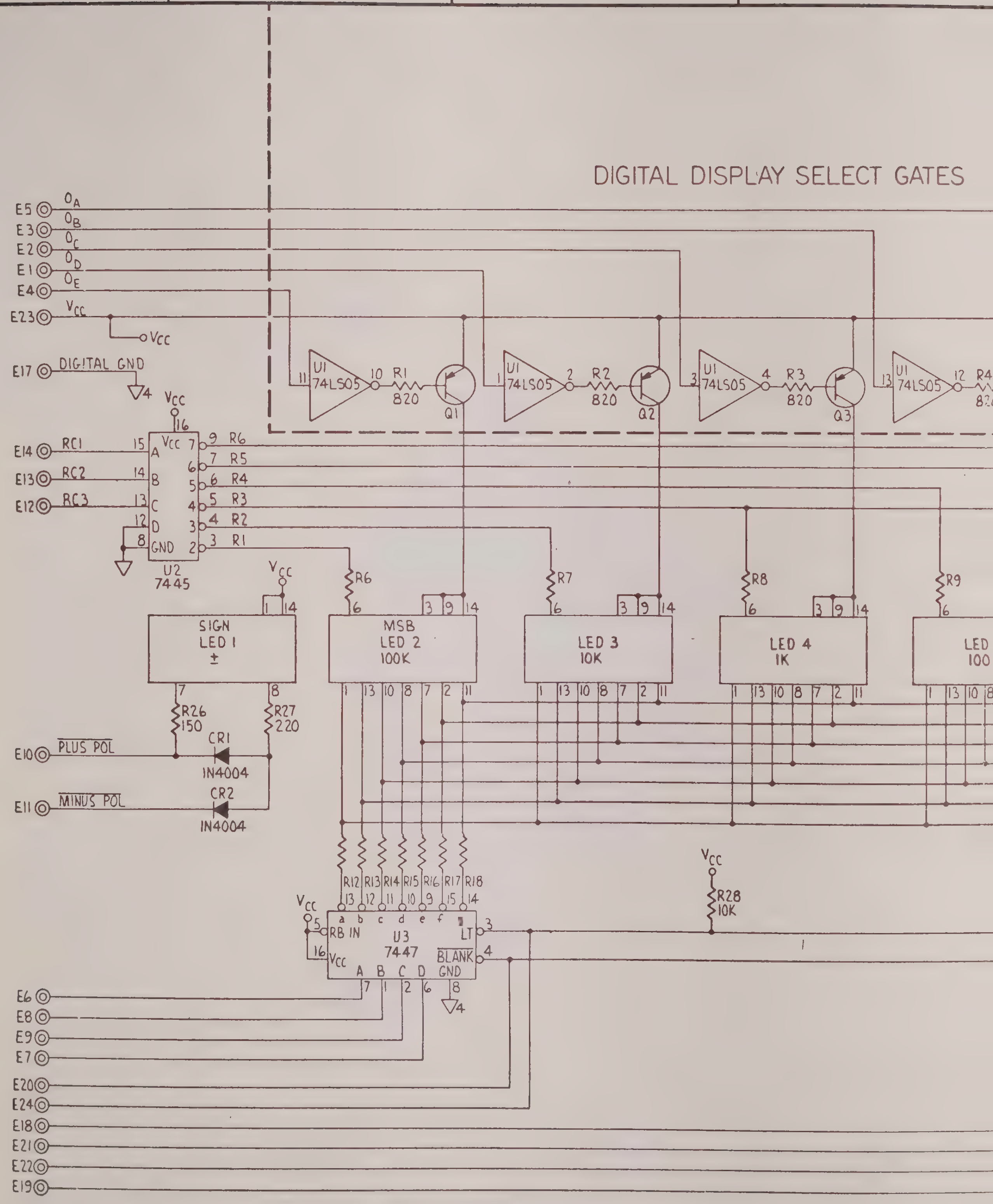
DRAWN	J. Bussow	
CHECK		
DESIGN		
MECH ENGR	Guercio	4.9.76
PROJ ENGR		
PROD ENGR		4.9.76

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DISPLAY BOARD ASSY.
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403855	D

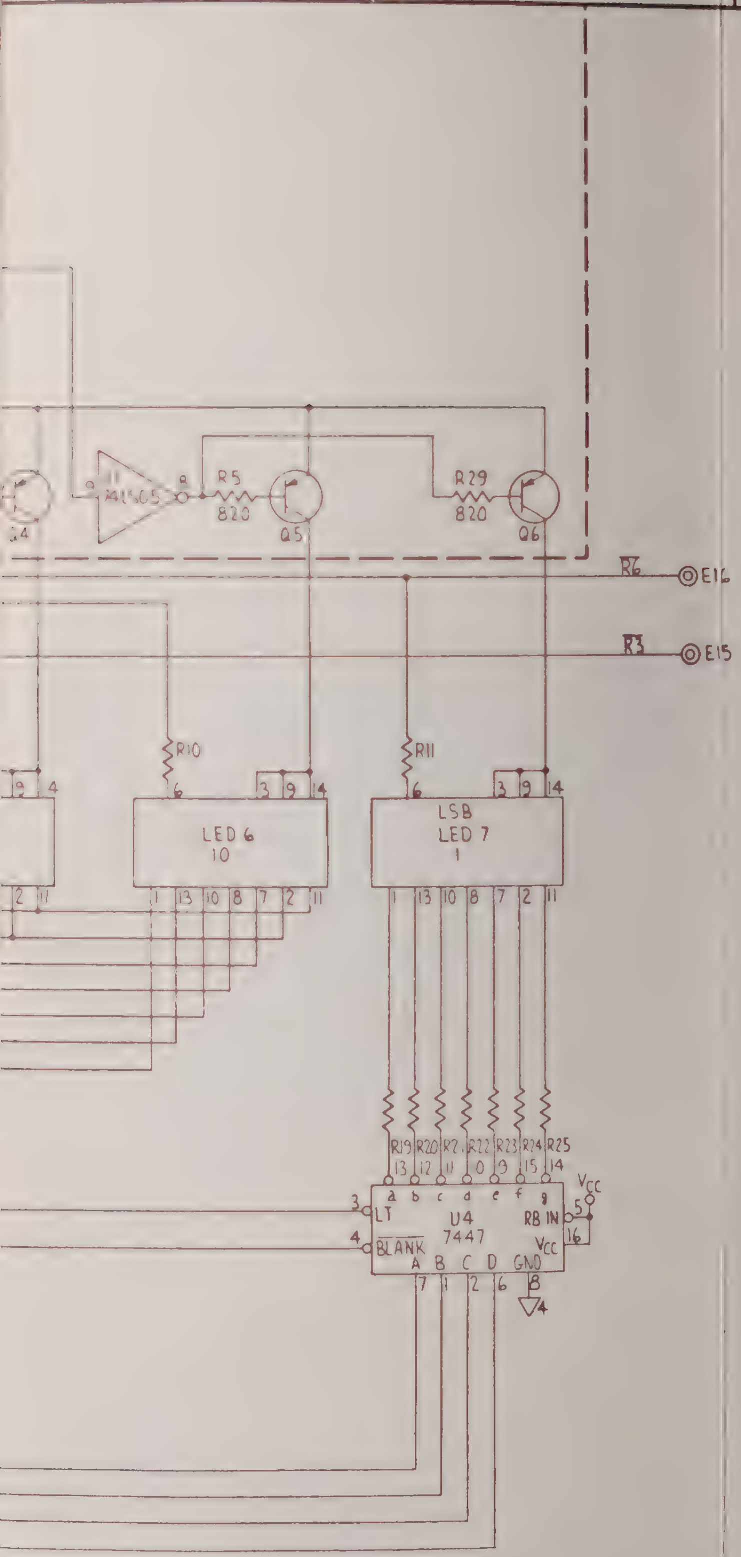
SCALE 4/1 SHEET 1 OF 4


DIGITAL DISPLAY SELECT GATES
E5 O_A
E3 O_B
E2 O_C
E1 O_D
E4 O_E
E23 V_{CC}
V_{CC}
E17 DIGITAL GND
4
U1 74LS05
R1 820
R2 820
R3 820
R4
Q1
Q2
Q3
U2 7445
RC1
RC2
RC3
E14
E13
E12
R6
R5
R4
R3
R2
R1
A B C D GND
R6 R7 R8 R9
SIGN LED 1 ±
MSB LED 2 100K
LED 3 10K
LED 4 1K
LED 100
R26 150
R27 220
CR1 1N4004
CR2 1N4004
E10 PLUS POL
E11 MINUS POL
R12 R13 R14 R15 R16 R17 R18
U3 7447
RB IN
LT
BLANK
GND
a b c d e f g
R28 10K
E6
E8
E9
E7
E20
E24
E18
E21
E22
E19

3. Q1-Q6 ARE MPS-A55
2. R6-R25 ARE 47 OHMS
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

PRO
THIS DOCUMENT A
ON DISCLOSED
LABORATORIES, IN
EXPRESS WRITTEN
RATORIES, INC BE
IN WHOLE OR IN PA
TIONS FROM A CON
MANUFACTURE BY
LABORATORIES, IN
HAS BEEN DEVELO
MAY ONLY BE USED
EVALUATION AND
TECHNICAL SPECIF
MENTS WHICH SPEC
FROM DANA LABOR

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
	B	**RELEASED PER DRN #**			
	—	REDRAWN WITHOUT CHANGE	10-12-77		



4
3
Q4
11
74LS05
8
9
R5
820
Q5
R29
820
Q6
R6
E16
R3
E15
R10
R11
9
4
3
9
14
6
6
3
9
14
LED 6
10
LSB
LED 7
1
2
11
1
13
10
8
7
2
11
1
13
10
8
7
2
11
R19
R20
R21
R22
R23
R24
R25
13
12
11
10
9
15
14
a
b
c
d
e
f
g
U4
7447
LT
BLANK
RB IN
VCC
VCC
GND
A
B
C
D
3
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5
16
7
1
2
6
8
4
E
D
C
B
A

ETARY NOTICE

THE TECHNICAL DATA HERE
PROPRIETARY TO DANA
AND SHALL NOT, WITHOUT
RMISSION OF DANA LABO-
D, RELEASED OR DISCLOSED
OR USED TO SOLICIT QUOTA
ITIVE SOURCE OR USED FOR
NYONE OTHER THAN DANA
THE INFORMATION HEREON
AT PRIVATE EXPENSE, AND
R PURPOSES OF ENGINEERING
OR INCORPORATION INTO
TIONS AND OTHER DOCU-
PROCUREMENT OF PRODUCTS
ORIES, INC.

403855	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND
INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X .030 XX .020 XXX .010	ANGLES 0 30' FORMED 1° 0'	HOLE DIAMETERS + .004 - .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN		
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC-
DISPLAY
5100

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	432076	B
SCALE		SHEET 1 OF 1	

2 1

PROPRIETARY NOTICE

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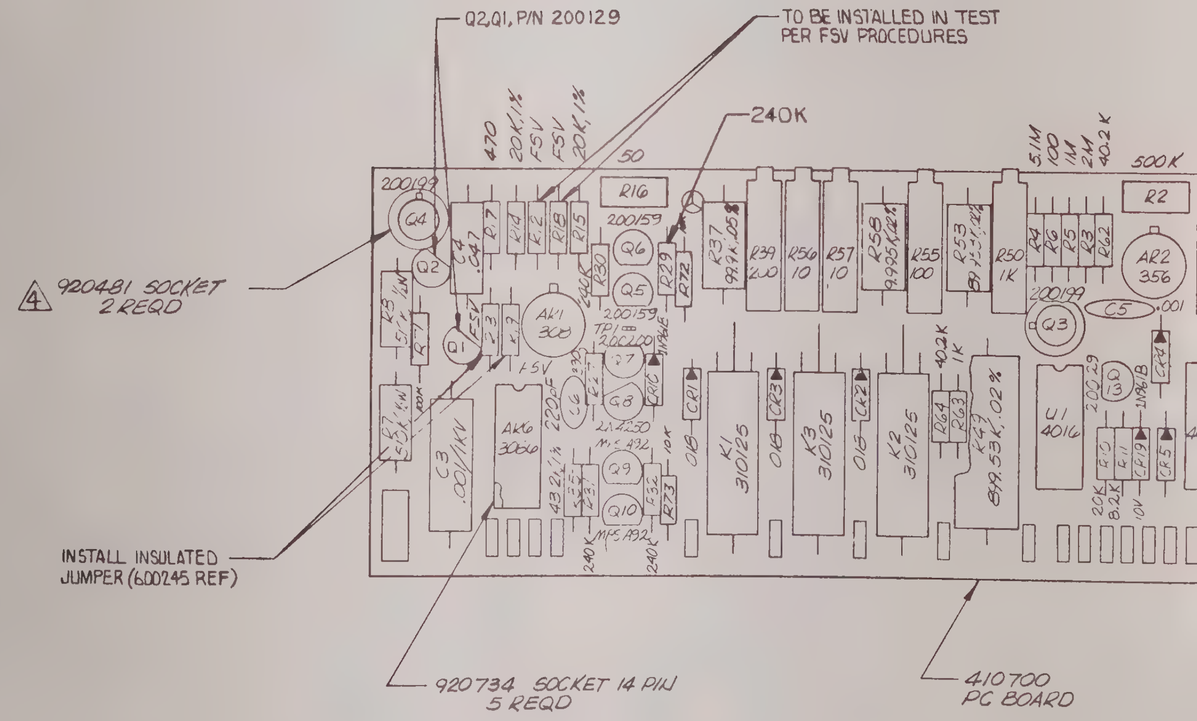
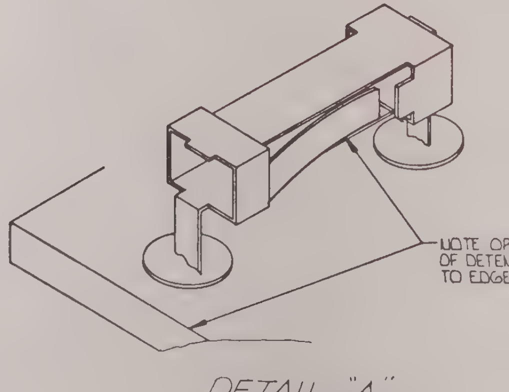

Q2,Q1, P/N 200129
TO BE INSTALLED IN TEST PER FSV PROCEDURES
240K
4 920481 SOCKET 2 REQD
INSTALL INSULATED JUMPER (600245 REF)
920734 SOCKET 14 PIN 5 REQD
410700 PC BOARD
470
20K,1%
FSV
FSV
20K,1%
50
R16
200159
R37 99.9K,.05%
R39 200
R56 10
R57 10
R58 9.995K,.02%
R55 100
R53
R50 1K
5.1M
100
1M
2M
40.2K
500K
R2
AR2 356
200199
Q3
C5 .001
Q4
Q2
C4 .047
Q1
AR1 308
Q6
Q5
Q7
Q8
Q9
Q10
AR6 3066
C3 .001/1KV
220pF
K1 310125
K3 310125
K2 310125
R47 89.53K,.02%
40.2K
1K
U1 4016
20K
8.2K
10V
240K
240K
10K
2N4250
MPS A92


NOTE OP
OF DETEN
TO EDGE

DETAIL "A"

4 MAX. COMPONENT HEIGHT TO BE . (Q3, Q4, AR1, AR2, AR3, AR4 & AR5)

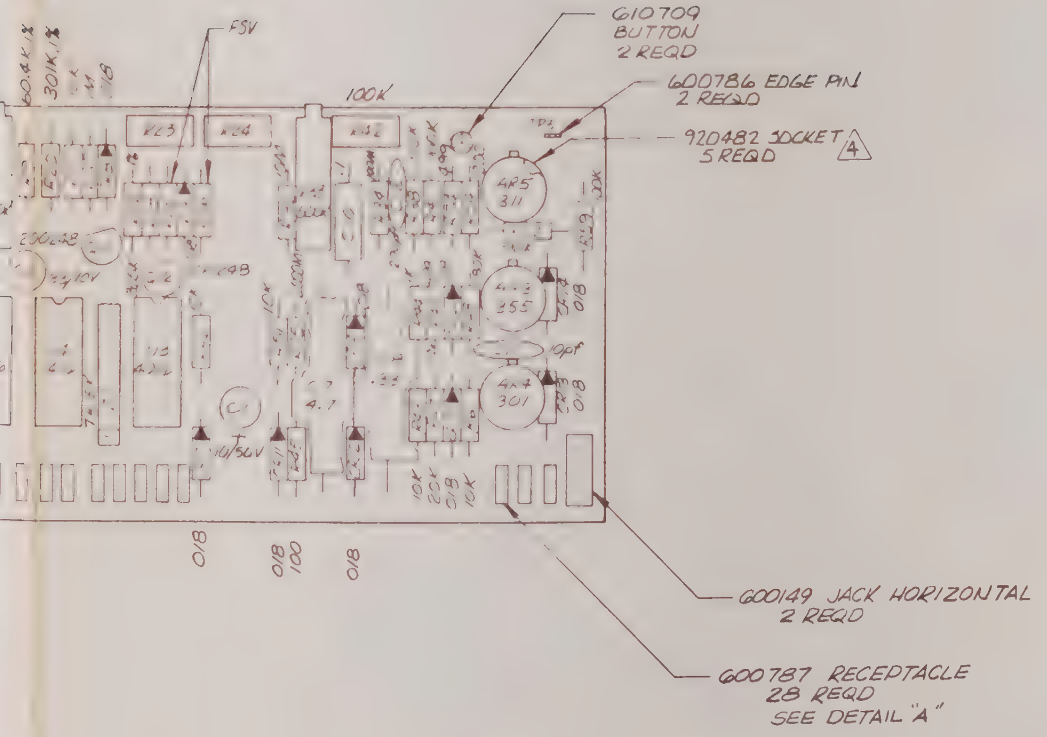
3. SCHEMATIC REF 432094

2. CAPACITORS ARE IN µF

1. RESISTORS ARE IN OHMS, 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

PCB KEY	LTR	DESCRIPTION	DR	CHK	APPD
		REVISIONS			
A	A	RELEASED PER DRN # 1121 4/13/7-			
	B	REVISED PER EO # 10223	RLH 11-4-76		
	C	# 10314			
	D	# 10392			
	E	# 10426			
	F	# 10537			
	H	# 10619			
D	J	REVISED PER EO # 10652	RLH 11-4-76		
	K	R10 WAS 010105, CR19 WAS IN961A, REVISED FSV CAL CUT FOR R12,R13,R18,R19,R25,R26 / EO10752	GB 1/5/77		
	L	Z1 WAS 08/005, C6 WAS .001µF R16 WAS 1K / EO 10789	↓		
	M	REVISED PER E O # 10849	B.KING 4 7 77		
F	N	REVISED PER E.O. # 10957	B.KING 4-7-77		
H	P	REVISED PER EO # 11004	CB 5-10 77		
J	R	REVISED PER EO # 11013			J KN H 6-3-77
	S	EO- 11194			
	T	EO- 11233			
	U	EO- 11250			


60.4K 1%
301K 1%
018
FSV
100K
R23
R24
R32
200248
10V
2.48
4R5
311
555
10pf
4A4
301
4.7
.33
10/50V
10K
20K
018
10K
018
018
100
018
610709
BUTTON
2 REQD
600786 EDGE PIN
2 REQD
920482 SOCKET
5 REQD
4
600149 JACK HORIZONTAL
2 REQD
600787 RECEPTACLE
28 REQD
SEE DETAIL "A"

JTATION
IN REF
F BOARD

403908	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X 030 XX 020 XXX 010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14 15

MATERIAL
FINISH

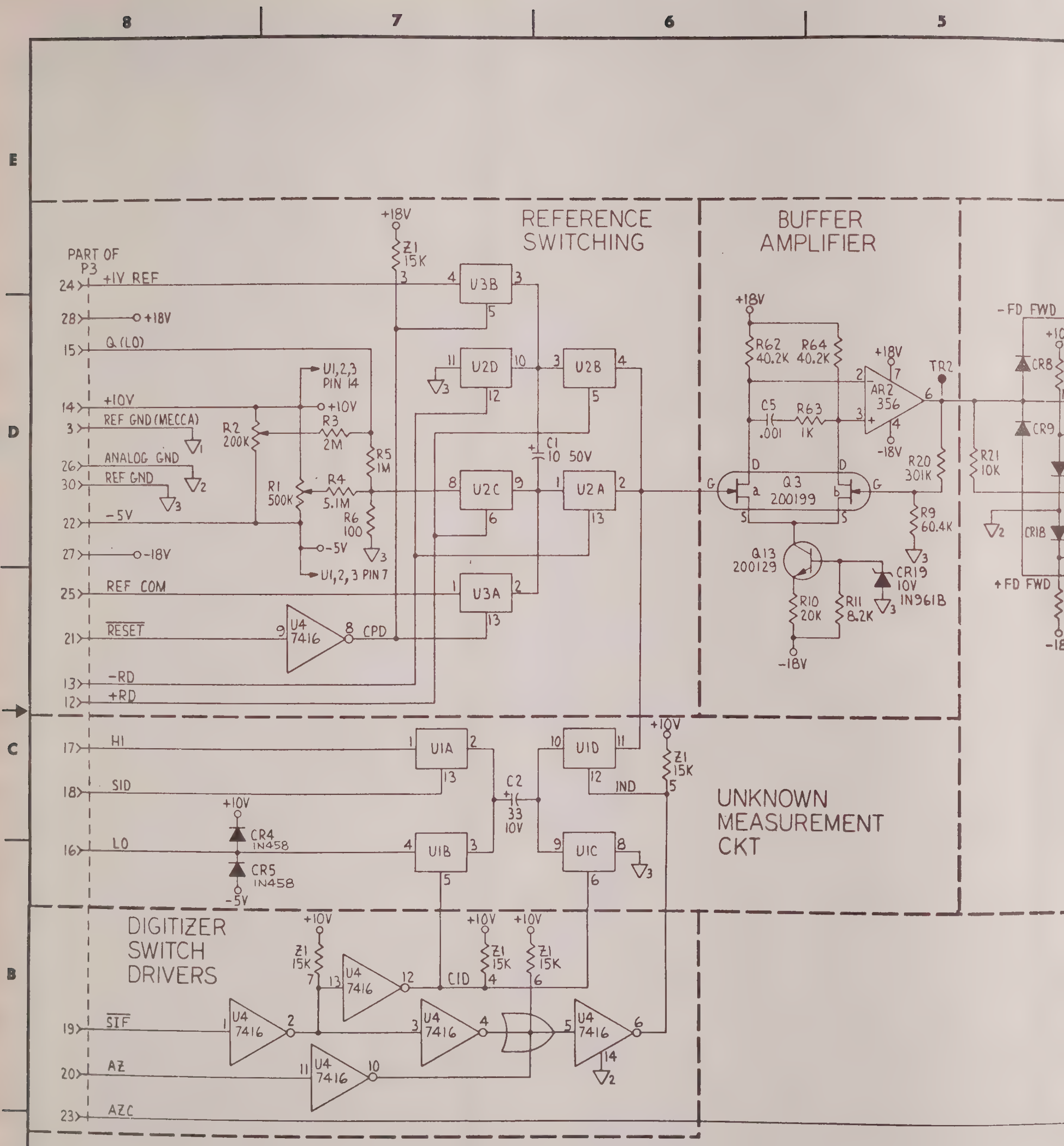
DRAWN		1/15/
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PC BOARD ASSY
DIGITIZER

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	403906	U

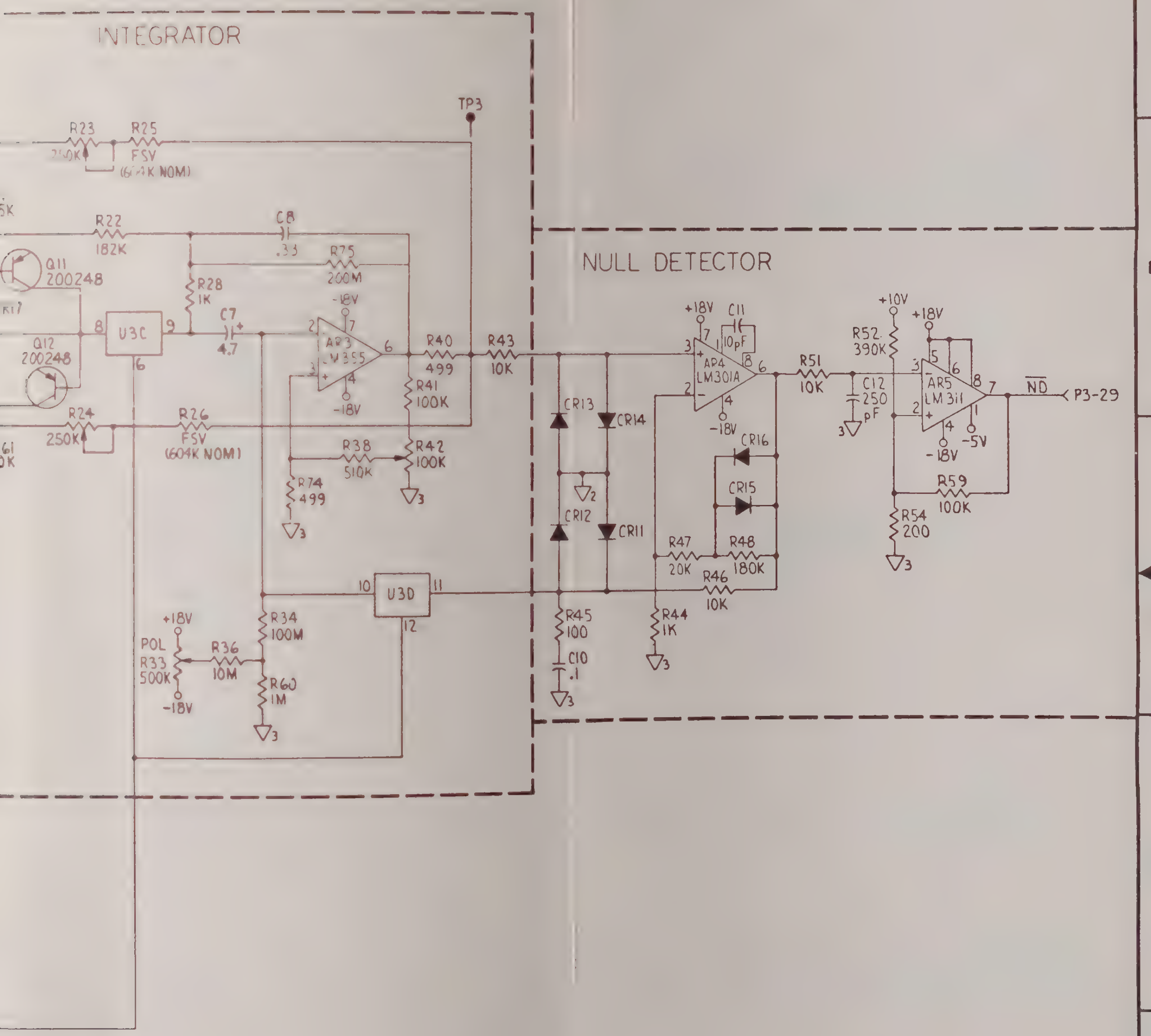
SCALE 2/1 SHEET 1 OF 2


8
7
6
5
E
D
C
B
REFERENCE SWITCHING
BUFFER AMPLIFIER
UNKNOWN MEASUREMENT CKT
DIGITIZER SWITCH DRIVERS
PART OF P3
24 +1V REF
28 +18V
15 Q (LO)
14 +10V
3 REF GND (MECCA)
26 ANALOG GND
30 REF GND
22 -5V
27 -18V
25 REF COM
21 RESET
13 -RD
12 +RD
17 HI
18 SID
16 LO
19 SIF
20 AZ
23 AZC
+18V
Z1 15K
U3B
U2D
U2B
U2C
U2A
U3A
U1,2,3 PIN 14
U1,2,3 PIN 7
+10V
-5V
R2 200K
R3 2M
R5 1M
R1 500K
R4 5.1M
R6 100
C1 10 50V
U4 7416
CPD
R62 40.2K
R64 40.2K
AR2 356
C5 .001
R63 1K
TR2
-18V
R20 301K
R21 10K
Q3 200199
R9 60.4K
Q13 200129
R10 20K
R11 8.2K
CR19 10V 1N961B
-FD FWD
+FD FWD
CR8
CR9
CR18
U1A
U1D
U1B
U1C
C2 33 10V
IND
CR4 1N458
CR5 1N458
CID

4. U1, U2 & U3 ARE CA4016AE BILATERAL SWITCHES
3. DIODES ARE 018
2. CAPACITORS ARE IN µF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

PROPRI
THIS DOCUMENT AND
ON DISCLOSED, ARE
LABORATORIES, INC.,
EXPRESS WRITTEN P
RATORIES, INC BE US
IN WHOLE OR IN PART
TIONS FROM A COMPE
MANUFACTURE BY A
LABORATORIES, INC
HAS BEEN DEVELOPED
MAY ONLY BE USED FO
EVALUATION AND
TECHNICAL SPECIFICA
MENTS WHICH SPECIFY
FROM DANA LABORAT

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	E	RELEASED PER DRN *			
	–	REDRAWN WITHOUT CHANGE	PA 10-12-77		
	F	REVISED PER EO 11194	PA 10-12-77		
	H	REVISED PER EO 11250	PA 10-12-77		


INTEGRATOR
TP3
R23
250K
R25
FSV
(604K NOM)
5K
R22
182K
C8
.33
R75
200M
Q11
200248
R28
1K
C7
4.7
-18V
AR3
LM355
R17
Q12
200248
8
U3C
9
6
2
7
3
4
6
-18V
R40
499
R43
10K
R41
100K
R24
250K
R26
FSV
(604K NOM)
R38
510K
R42
100K
R74
499
61
0K
10
U3D
11
12
+18V
POL
R33
500K
-18V
R36
10M
R34
100M
R60
1M
NULL DETECTOR
CR13
CR14
CR12
CR11
R45
100
C10
.1
+18V
C11
10pF
AR4
LM301A
1
8
6
3
2
4
-18V
CR16
CR15
R47
20K
R48
180K
R46
10K
R44
1K
+10V
R52
390K
R51
10K
C12
250
pF
+18V
AR5
LM 311
5
6
8
7
3
2
4
1
-18V
-5V
R59
100K
R54
200
ND
P3-29

TARY NOTICE

HE TECHNICAL DATA HERE PROPRIETARY TO DANA AND SHALL NOT, WITHOUT RMISSION OF DANA LABO D RELEASED OR DISCLOSED OR USED TO SOLICIT QUOTA TIVE SOURCE OR USED FOR YONE OTHER THAN DANA THE INFORMATION HEREON AT PRIVATE EXPENSE, AND PURPOSES OF ENGINEERING OR INCORPORATION INTO IONS AND OTHER DOCU ROCUREMENT OF PRODUCTS RIES, INC.

403906	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30′ FORMED 1° 0′	+ .004 – .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

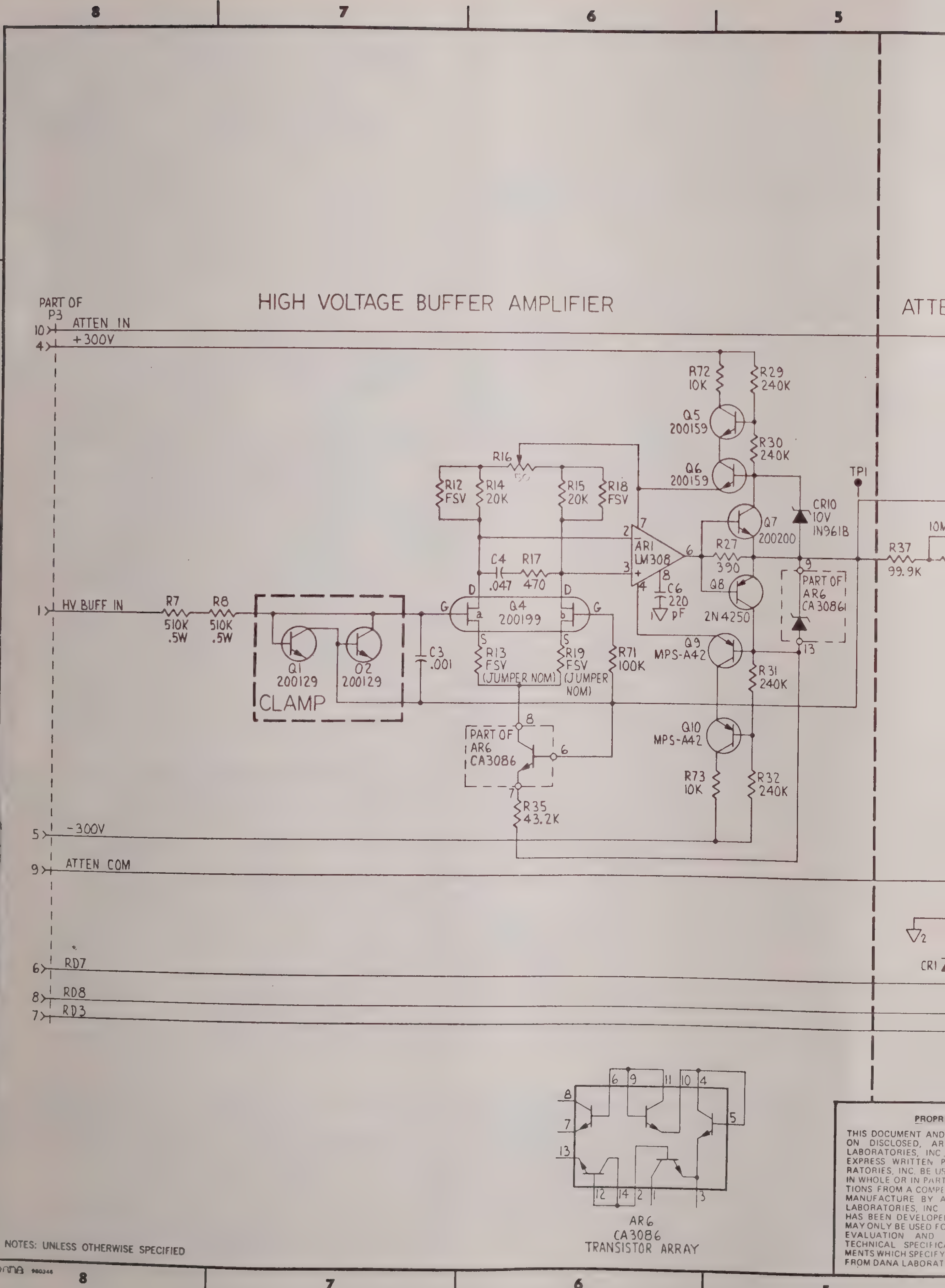
DRAWN	Rich Mays	5-13-7
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC –
DIGITIZER
5100

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432094	H

SCALE SHEET 1 OF 2

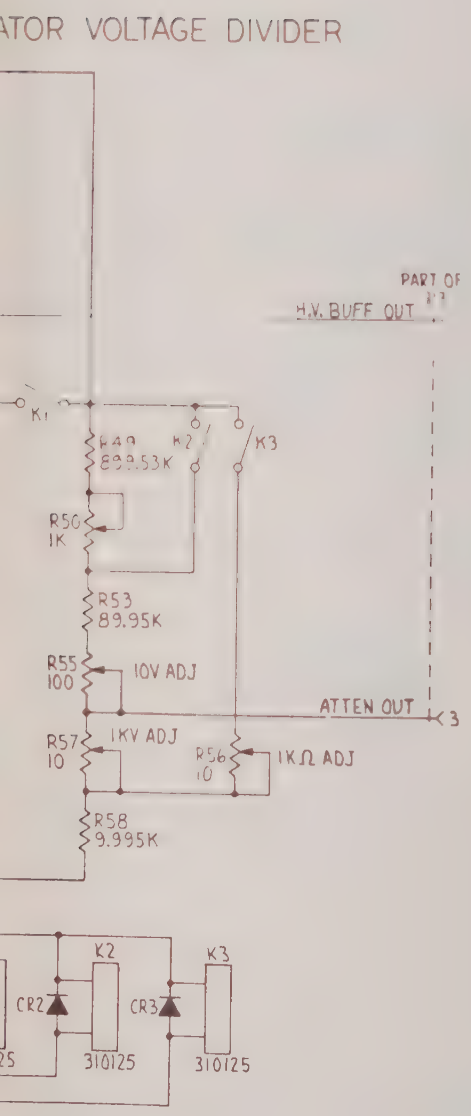

8
7
6
5
HIGH VOLTAGE BUFFER AMPLIFIER
ATTE
PART OF P3
10 ATTEN IN
4 +300V
1 HV BUFF IN
5 -300V
9 ATTEN COM
6 RD7
8 RD8
7 RD3
R7 510K .5W
R8 510K .5W
Q1 200129
Q2 200129
CLAMP
C3 .001
R12 FSV
R14 20K
R16 50
R15 20K
R18 FSV
C4 .047
R17 470
Q4 200199
D
G
S
a
b
R13 FSV (JUMPER NOM)
R19 FSV (JUMPER NOM)
R71 100K
PART OF AR6 CA3086
8
6
7
R35 43.2K
AR1 LM308
2
3
7
6
4
8
C6 220 pF
R72 10K
R29 240K
Q5 200159
R30 240K
Q6 200159
Q7 200200
R27 390
Q8 2N4250
Q9 MPS-A42
R31 240K
Q10 MPS-A42
R73 10K
R32 240K
CR10 10V 1N961B
PART OF AR6 CA3086
9
13
TP1
R37 99.9K
10M
CR1
2
AR6 CA3086 TRANSISTOR ARRAY
6
9
11
10
4
5
3
12
14
2
1
13
7
8

NOTES: UNLESS OTHERWISE SPECIFIED

PROPR
THIS DOCUMENT AND
ON DISCLOSED, AR
LABORATORIES, INC.
EXPRESS WRITTEN P
RATORIES, INC. BE US
IN WHOLE OR IN PART
TIONS FROM A COMPE
MANUFACTURE BY A
LABORATORIES, INC
HAS BEEN DEVELOPE
MAY ONLY BE USED FO
EVALUATION AND
TECHNICAL SPECIFICA
MENTS WHICH SPECIFY
FROM DANA LABORAT

DANA 980346

PCB REV	REVISIONS				
	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET 1			



ATOR VOLTAGE DIVIDER
PART OF
H.V. BUFF OUT
K1
K2
K3
R49
899.53K
R50
1K
R53
89.95K
R55
100
10V ADJ
ATTEN OUT
3
R57
10
1KV ADJ
R56
10
1KΩ ADJ
R58
9.995K
CR2
CR3
K2
K3
25
310125
310125

OTICE

CHNICAL DATA HERE
RIETARY TO DANA
HALL NOT, WITHOUT
N OF DANA LABO
ASED OR DISCLOSED
D TO SOLICIT QUOTA
OURCE OR USED FOR
OTHER THAN DANA
ORMATION HEREON
VATE EXPENSE, AND
SES OF ENGINEERING
CORPORATION INTO
AND OTHER DOCU
EMENT OF PRODUCTS
C.

403906	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X .030 XX .020 XXX .010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	Rich Mays	
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC–
DIGITIZER
5100

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	432094	H
SCALE —		SHEET 2 OF 2	

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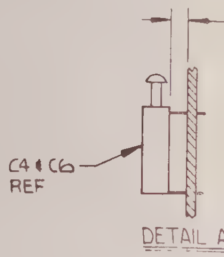
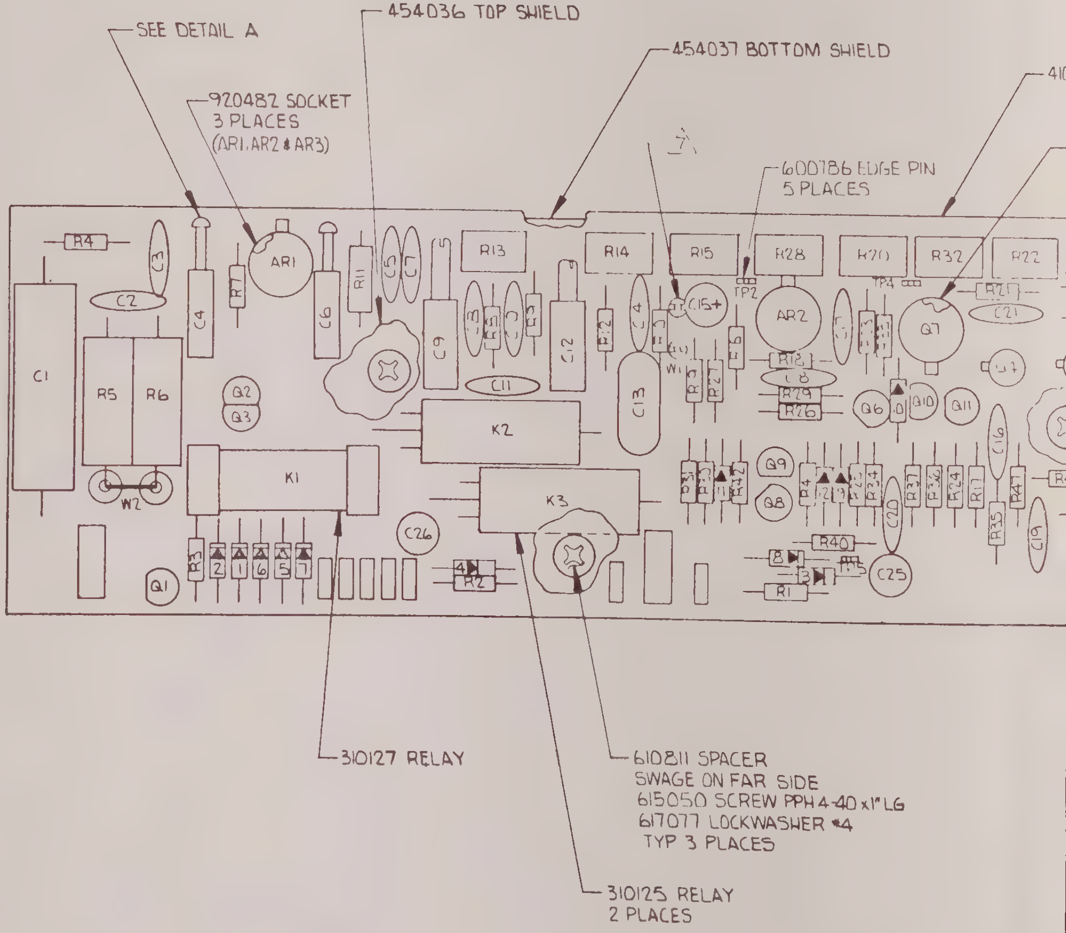

C4 ⧫ C6
REF
DETAIL A


SEE DETAIL A
454036 TOP SHIELD
454037 BOTTOM SHIELD
920482 SOCKET
3 PLACES
(AR1, AR2 ⧫ AR3)
600786 EDGE PIN
5 PLACES
7
R4
C3
C2
C4
R7
AR1
C6
R11
C5
C7
C9
R13
C11
C12
R14
C13
R15
C15+
W1
TP2
R28
AR2
R18
R29
R26
R20
TP4
R32
Q7
R22
R21
C21
Q6
Q10
Q11
C1
R5
R6
Q2
Q3
K2
K1
K3
W2
Q9
Q8
C16
C20
R40
C25
R1
R2
R3
R35
R41
C19
R37
R24
R17
C26
Q1
310127 RELAY
610811 SPACER
SWAGE ON FAR SIDE
615050 SCREW PPH 4-40 x 1" LG
617077 LOCKWASHER #4
TYP 3 PLACES
310125 RELAY
2 PLACES

△7 W-1 IS TO BE INSTALLED IN TEST, W-1 IS P/N 500023 WIRE.

△6 MAX HEIGHT FOR AR1, AR2, AR3 ⧫ Q7.

5. Q4, Q5, R17 ⧫ R47 ARE A LOG TRANSISTOR SET 403865.

4. CUT CENTER (EMITTER) LEAD OFF ON Q2 ⧫ Q3.

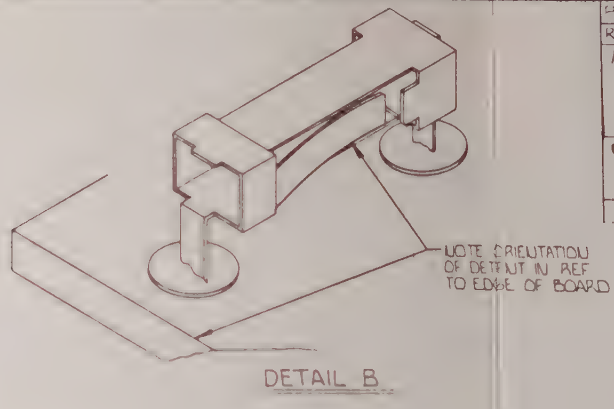
3. RESISTORS ARE IN OHMS, ±5%, 1/4W.

2. SCHEMATIC REF. 432092.

1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

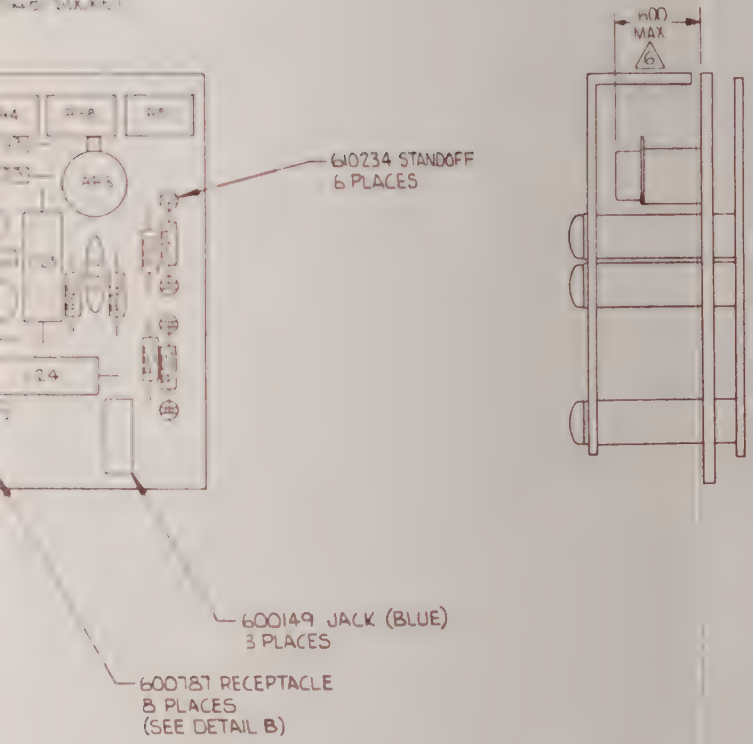
DANA 980346 DIETERICH POST CLEARPRINT 1000



…s25
NOTE ORIENTATION OF DETENT IN REF TO EDGE OF BOARD

DETAIL B

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
A	A	RELEASED PER DRN # 1123 4/1/76	mayes		
	B	REVISED PER E.O 10270	KAM 9 13 76	RLH 11 18-76	
	C	REVISED PER E.O 10292	KAM 9 13 76	RLH 11 5-76	
	D	REVISED PER E.O 10355	KAM	RLH	
C	E	REVISED PER EO 10618	12-8-76		
	F	REVISED PER EO 10750		1/10/77	
	H	R32 WAS 100Ω / R51 WAS 040193 / EO 10774			
	J	REVISED PER EO 10906	DRNG 4-27-77	KAM 5-4-77	



… BOARD
… SOCKET
.00 MAX
6
610234 STANDOFF 6 PLACES
600149 JACK (BLUE) 3 PLACES
600787 RECEPTACLE 8 PLACES (SEE DETAIL B)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X 030 XX 020 XXX 010	ANGLES 0 30' FORMED 1' 0'	HOLE DIAMETERS + 004 001

DIMENSIONS AND TOLERANCES PER USAS Y14 15

MATERIAL

FINISH

403908	5100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

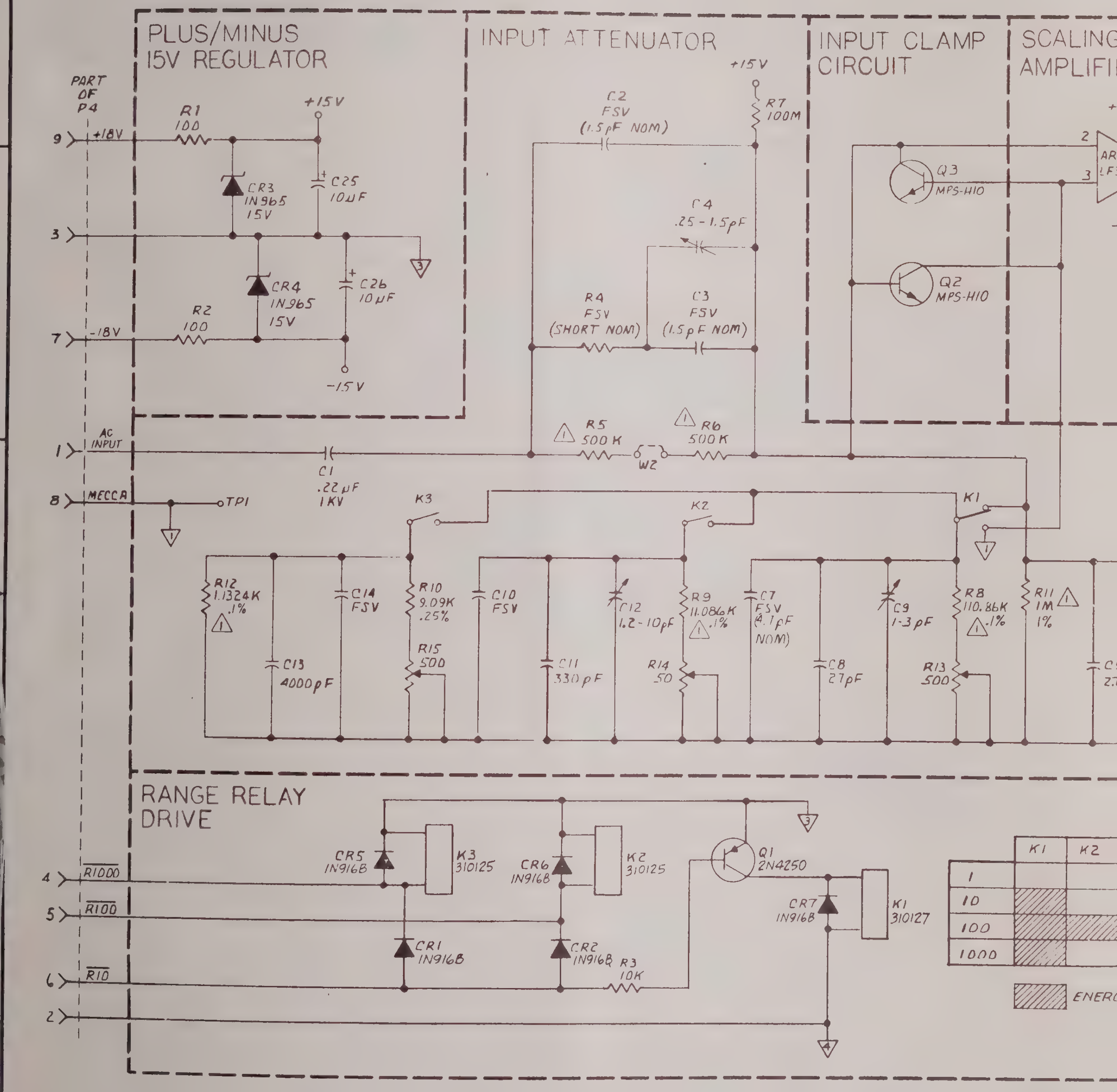
DRAWN		9/4/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	Rh Roland	6/7/76
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSEMBLY
RMS CONVERTER
MODEL 5100

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	403904	J

SCALE NONE SHEET OF 3


PLUS/MINUS 15V REGULATOR
INPUT ATTENUATOR
INPUT CLAMP CIRCUIT
SCALING
AMPLIFI
RANGE RELAY DRIVE
PART OF P4
9 +18V
3
7 -18V
1 AC INPUT
8 MECCA
4 R1000
5 R100
6 R10
2
R1 100
+15V
CR3 1N965 15V
C25 10µF
CR4 1N965 15V
C26 10µF
R2 100
-15V
C2 FSV (1.5pF NOM)
+15V
R7 100M
C4 .25 - 1.5pF
R4 FSV (SHORT NOM)
C3 FSV (1.5pF NOM)
R5 500K
R6 500K
W2
C1 .22µF 1KV
TP1
K3
K2
K1
Q3 MPS-H10
Q2 MPS-H10
2
3
AR
LF
R12 1.1324K .1%
C14 FSV
C13 4000pF
R10 9.09K .25%
R15 500
C10 FSV
C11 330pF
C12 1.2-10pF
R9 11.086K .1%
R14 50
C7 FSV (4.7pF NOM)
C8 27pF
C9 1-3pF
R8 110.86K .1%
R13 500
R11 1M 1%
CR5 1N916B
K3 310125
CR6 1N916B
K2 310125
Q1 2N4250
CR7 1N916B
K1 310127
CR1 1N916B
CR2 1N916B
R3 10K
ENERG

	K1	K2
1		
10	▨	
100	▨	▨
1000	▨	

6. ALL RESISTORS ARE IN OHMS, ±5% ¼W

5 403865 LOG TRANS SET (Q4, Q5, R17, R47)

4 012018 RESISTOR SET (R19, R26)

3 012017 RESISTOR SET (R18, R23, R46)

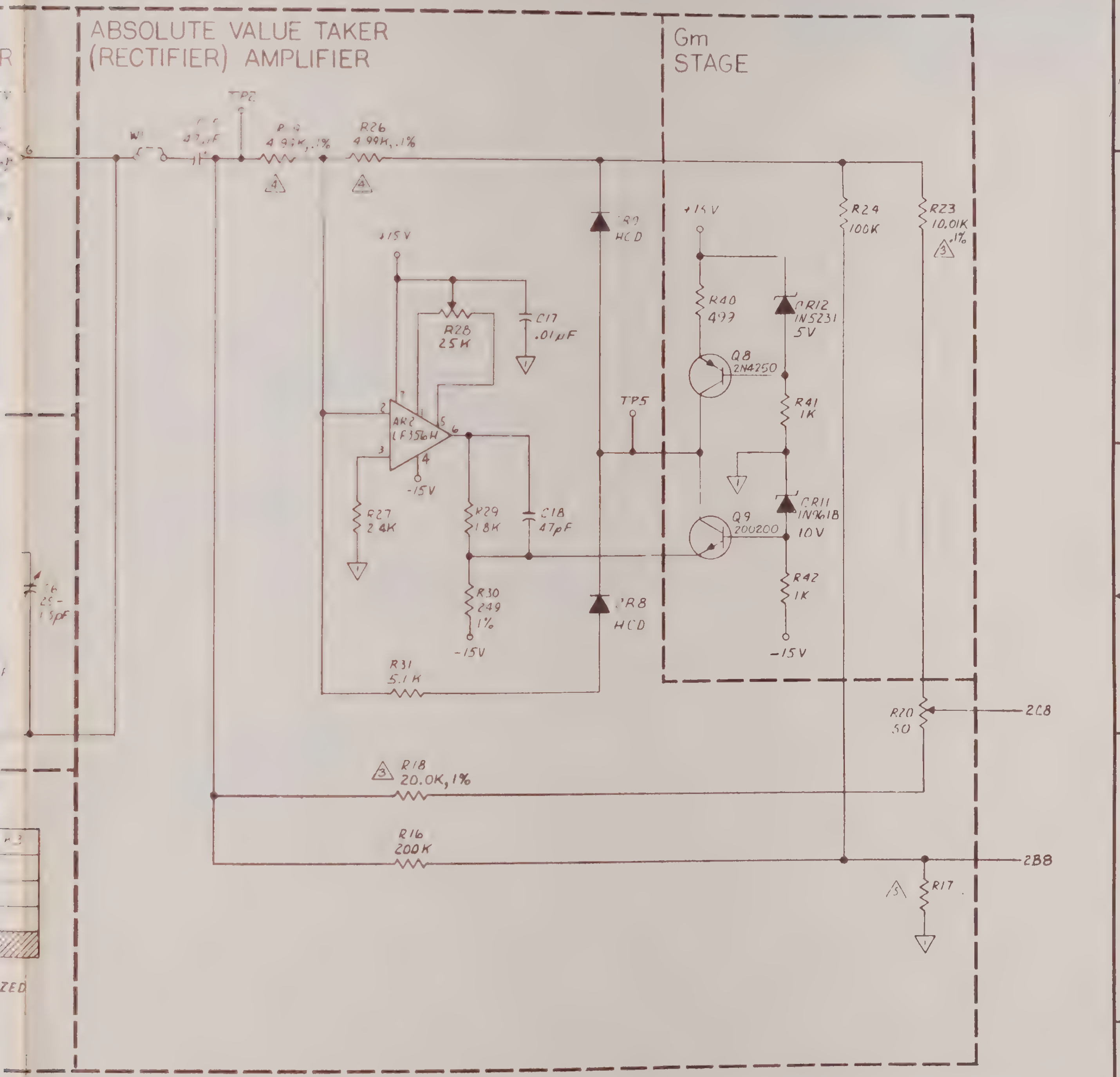
2 012016 RESISTOR SET (R50, R52)

1 012015 RESISTOR SET (R5, R6, R8, R9, R11, R12)

NOTES: UNLESS OTHERWISE SPECIFIED

PROPRI
THIS DOCUMENT AND
ON DISCLOSED, ARE
LABORATORIES, INC.,
EXPRESS WRITTEN P
RATORIES, INC. BE US
IN WHOLE OR IN PART
TIONS FROM A COMPE
MANUFACTURE BY A
LABORATORIES, INC
HAS BEEN DEVELOPED
MAY ONLY BE USED FO
EVALUATION AND
TECHNICAL SPECIFICA
MENTS WHICH SPECIFY
FROM DANA LABORATO

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
	B	RELEASED PER DRN #			
	—	REDRAWN WITHOUT CHANGE	ROBIN 11 24 77		
	C	REVISED PER EC	SA 10 24-77		


ABSOLUTE VALUE TAKER (RECTIFIER) AMPLIFIER
Gm STAGE
6
W1
47μF
TP2
4.99K, .1%
R26
4.99K, .1%
4
4
+15V
R28
25K
C17
.01μF
AR2
LF356H
2
3
4
5
6
7
-15V
R27
2.4K
R29
1.8K
C18
47pF
R30
249
1%
-15V
R31
5.1K
CR7
HCD
CR8
HCD
TP5
+15V
R40
499
CR12
1N5231
5V
Q8
2N4250
R41
1K
CR11
1N961B
10V
Q9
2N2200
R42
1K
-15V
R24
100K
R23
10.01K
.1%
3
R20
50
2C8
3
R18
20.0K, 1%
R16
200K
2B8
3
R17
25-
15pF
ZED

ARY NOTICE

HE TECHNICAL DATA HERE- PROPRIETARY TO DANA ND SHALL NOT, WITHOUT MISSION OF DANA LABO , RELEASED OR DISCLOSED R USED TO SOLICIT QUOTA TIVE SOURCE OR USED FOR ONE OTHER THAN DANA HE INFORMATION HEREON AT PRIVATE EXPENSE, AND PURPOSES OF ENGINEERING R INCORPORATION INTO ONS AND OTHER DOCU- OCUREMENT OF PRODUCTS IES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX 020 XXX 010	0° 30′ FORMED 1° 0′	+ 004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN		4/7/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R KOLUVAK	5/7/76
PROD ENGR		

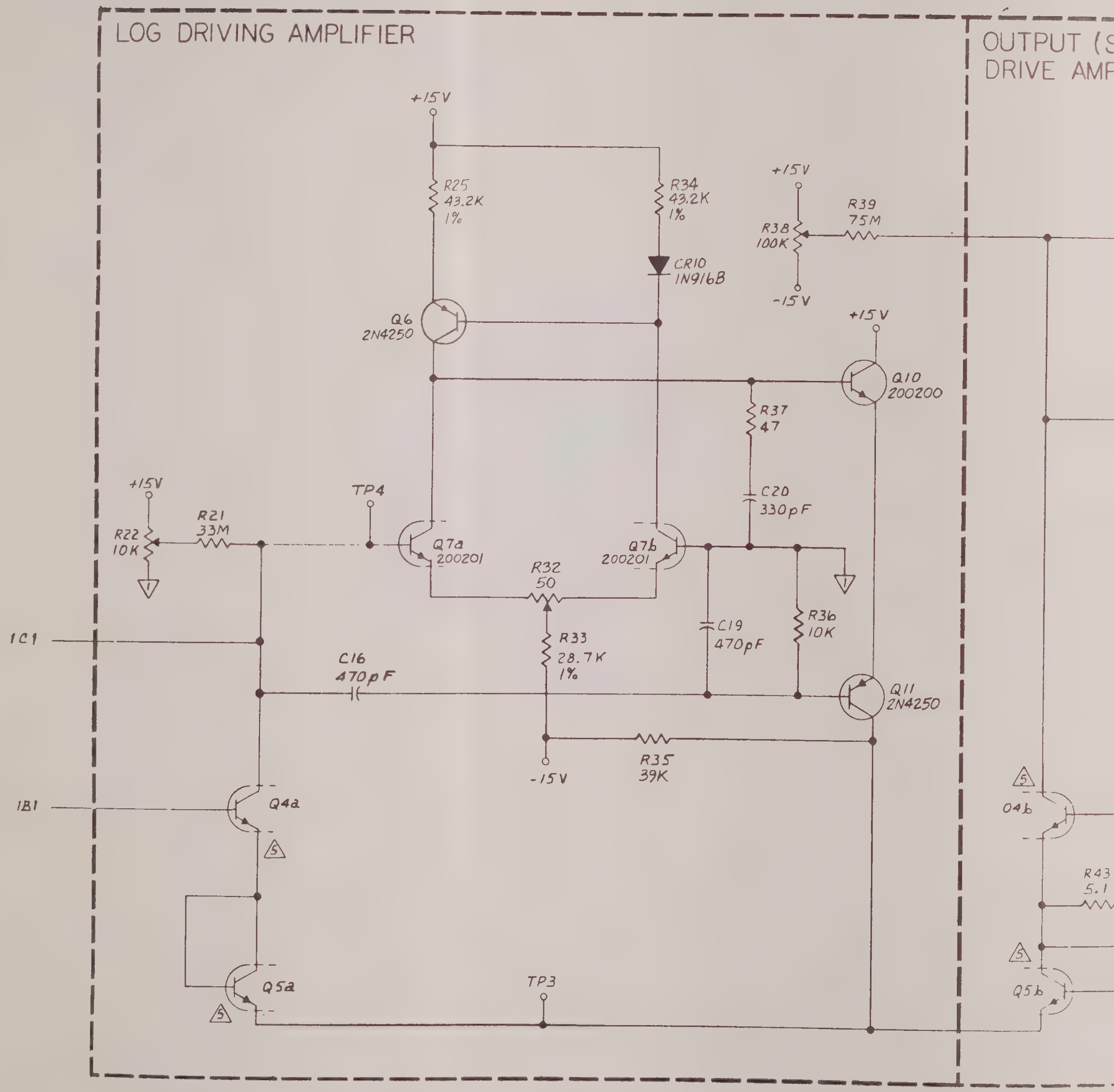
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC -
RMS AC CONVERTER
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432092	C

SCALE

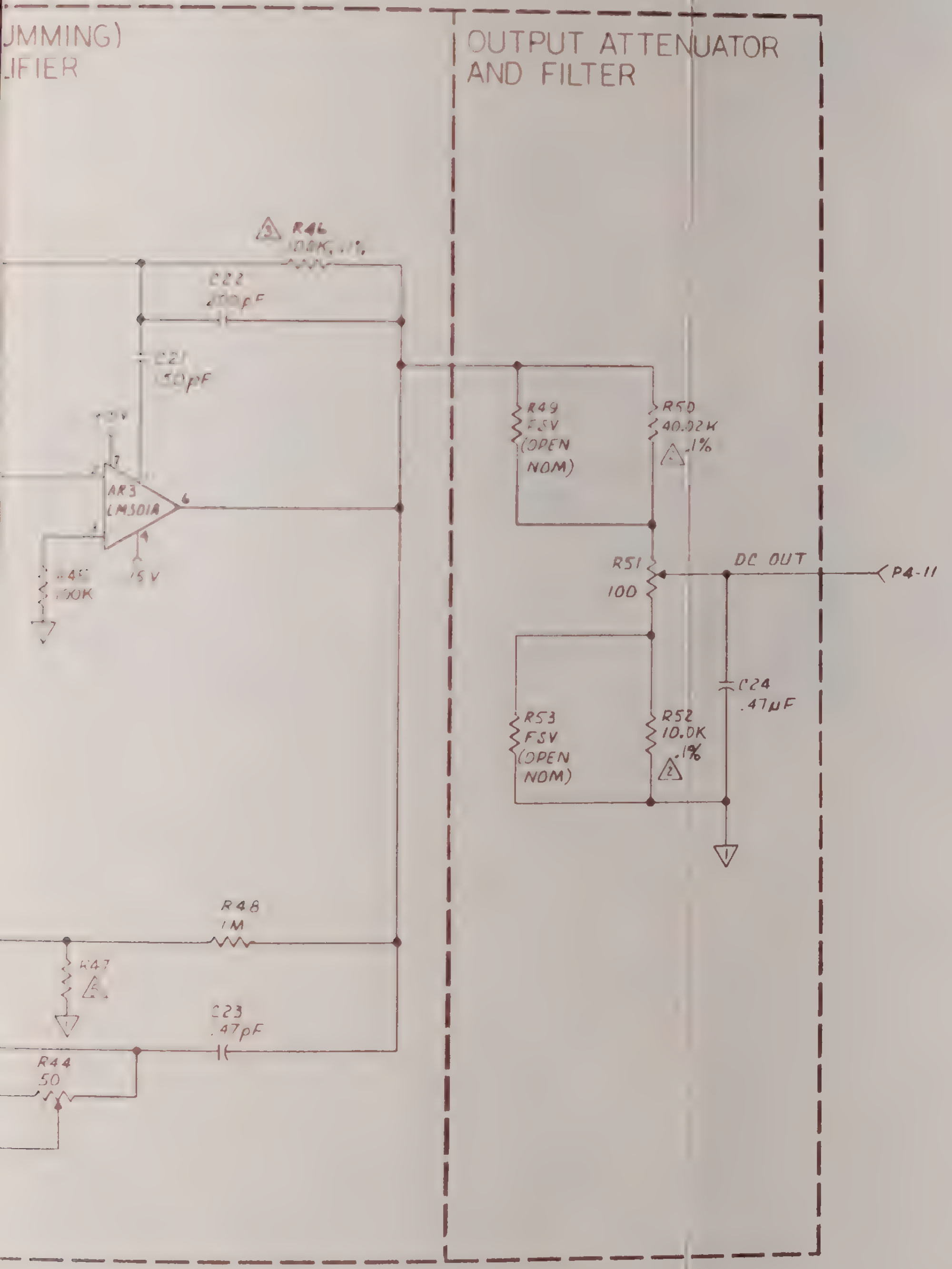
SHEET 1 OF 2


LOG DRIVING AMPLIFIER
OUTPUT (S
DRIVE AMP
+15V
R25
43.2K
1%
R34
43.2K
1%
CR10
1N916B
Q6
2N4250
+15V
R38
100K
-15V
R39
75M
+15V
Q10
200200
R37
47
C20
330pF
+15V
R22
10K
R21
33M
TP4
Q7a
200201
Q7b
200201
R32
50
R36
10K
1C1
R33
28.7K
1%
C19
470pF
C16
470pF
Q11
2N4250
-15V
R35
39K
1B1
Q4a
5
Q5a
5
TP3
5
Q4b
R43
5.1
5
Q5b

PROPRIETAI
THIS DOCUMENT AND THE
ON DISCLOSED, ARE PF
LABORATORIES, INC., ANI
EXPRESS WRITTEN PERMI
RATORIES, INC. BE USED, F
IN WHOLE OR IN PART, OR
TIONS FROM A COMPETITIV
MANUFACTURE BY ANYOI
LABORATORIES, INC. THE
HAS BEEN DEVELOPED AT
MAY ONLY BE USED FOR PU
EVALUATION AND FOR
TECHNICAL SPECIFICATION
MENTS WHICH SPECIFY PROC
FROM DANA LABORATORIES

NOTES: UNLESS OTHERWISE SPECIFIED

PCB REV	LTR	REVISIONS DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # SEE SHEET ONE			



UMMING)
IFIER
OUTPUT ATTENUATOR
AND FILTER
3 R46
100K, .1%
C22
100pF
C21
150pF
+15V
7
AR3
LM301A
6
4
-15V
R45
100K
R49
FSV
(OPEN
NOM)
R50
40.02K
.1%
R51
100
DC OUT
P4-11
C24
.47μF
R53
FSV
(OPEN
NOM)
R52
10.0K
.1%
2
R48
1M
R47
C23
.47pF
R44
50

Y NOTICE

TECHNICAL DATA HERE- PRIETARY TO DANA SHALL NOT, WITHOUT SION OF DANA LABO- LEASED OR DISCLOSED SED TO SOLICIT QUOTA SOURCE OR USED FOR E OTHER THAN DANA INFORMATION HEREON RIVATE EXPENSE, AND POSES OF ENGINEERING NCORPORATION INTO S AND OTHER DOCU- UREMENT OF PRODUCTS INC

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX 010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

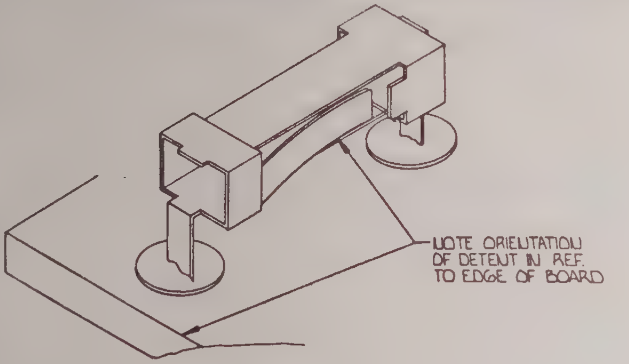
DRAWN	Z [illegible]	
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R KOLUVAK	5/7/[illegible]
PROD ENGR	[illegible]	

DANA DANA LABORATORIES INC.
IRVINE, CALIFORNIA

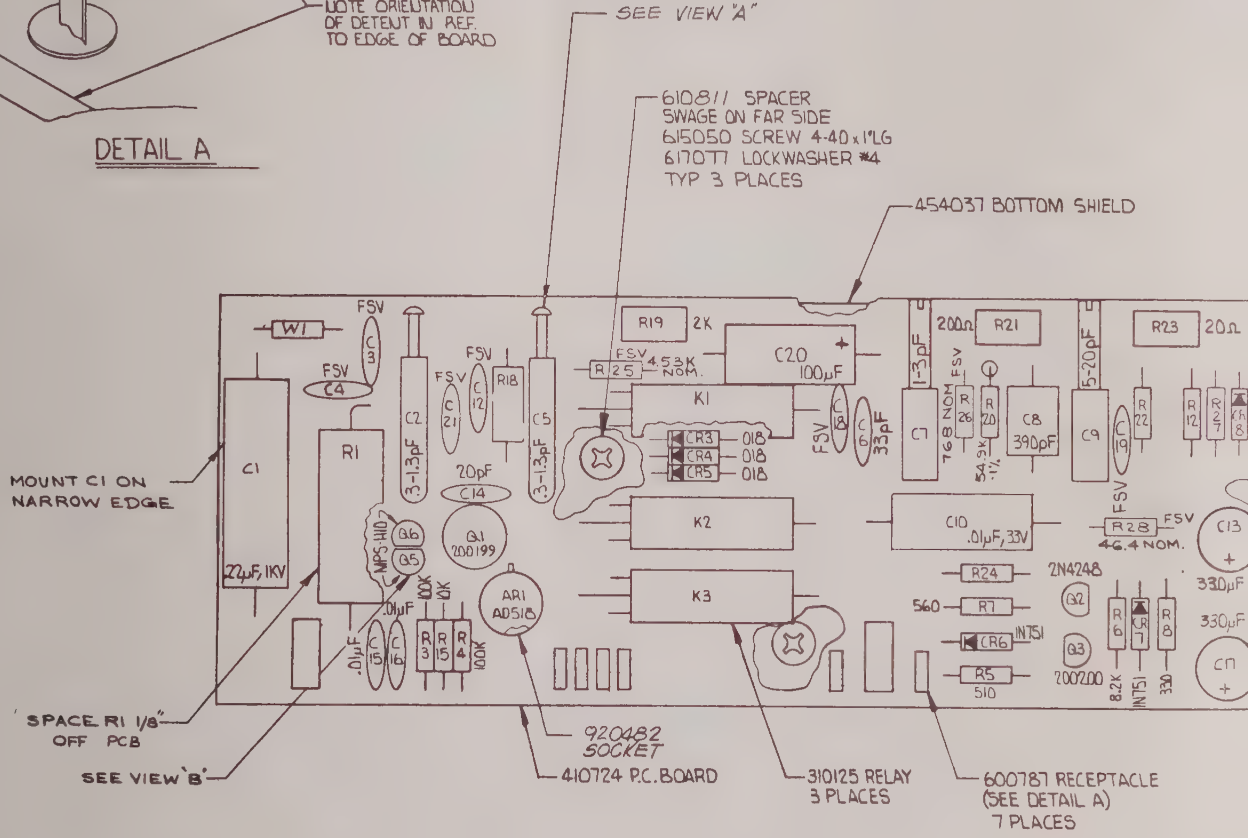
SCHEMATIC
RMS AC CONVERTER
MODEL 5100

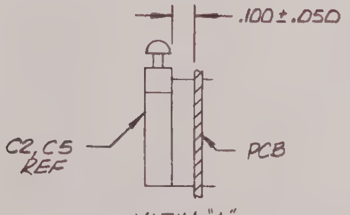
SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	432092	C

SCALE SHEET 2 OF 2

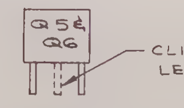

NOTE ORIENTATION
OF DETENT IN REF.
TO EDGE OF BOARD

DETAIL A


SEE VIEW "A"
610811 SPACER
SWAGE ON FAR SIDE
615050 SCREW 4-40 x 1"LG
617077 LOCKWASHER #4
TYP 3 PLACES
454037 BOTTOM SHIELD
W1
FSV
C3
FSV
C4
C1
22μF, 1KV
MOUNT C1 ON
NARROW EDGE
R1
C2
3-1.3pF
FSV
C21
FSV
C12
R18
C5
3-1.3pF
20pF
C14
MPS-H10
Q6
Q5
Q1
200199
AR1
AD518
.01μF
.01μF
C15
C16
10K
10K
R3
R15
R4
100K
R19
2K
FSV
R25
4.53K NOM.
C20
100μF
+
K1
CR3
CR4
CR5
018
018
018
FSV
C18
C6
33pF
K2
K3
1-3pF
200Ω
R21
FSV
R26
768 NOM
R20
54.9K 1%
C7
C8
390pF
5-20pF
C9
C19
R22
R23
20Ω
R12
R27
CR8
FSV
C10
.01μF, 33V
FSV
R28
46.4 NOM.
C13
+
330μF
R24
2N4248
Q2
560
R7
CR6
IN751
Q3
200200
R5
510
R6
8.2K
CR7
IN751
R8
330
330μF
C11
+
SPACE R1 1/8"
OFF PCB
SEE VIEW 'B'
920482
SOCKET
410724 P.C. BOARD
310125 RELAY
3 PLACES
600787 RECEPTACLE
(SEE DETAIL A)
7 PLACES


.100 ± .050
C2, C5
REF
PCB

VIEW "A"



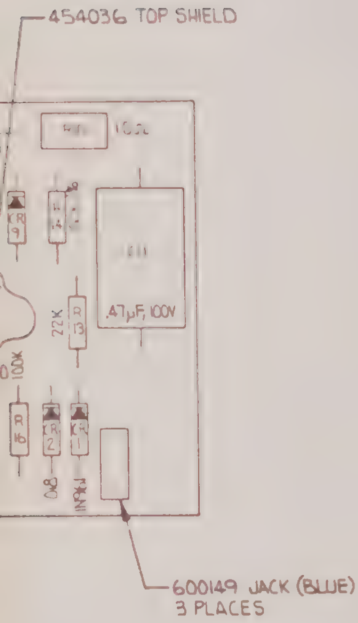
VIEW "B"

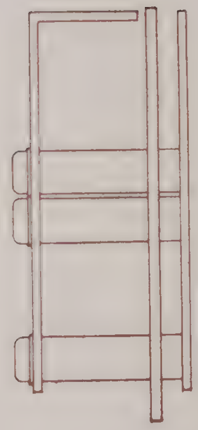
4. *CUT CENTER (EMITTER) LEAD OFF ON Q5 & Q6*
3. RESISTORS ARE IN OHMS, ±5%, 1/4W.
2. SCHEMATIC REF. 432093.
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

THIS D
DISCLO
INC A
MISSIO
LEASED
SOLICIT
USED
DANA
HAS BE
ONLY B
TION A
FICATIO
CURSOR
INC

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		REVISIONS			
A	A	RELEASED PER DRN # 1121 4/13/76			
	B	REVISED PER E.O 10271	KAM	RLH 11-9-76	TJD
	C	REVISED PER E.O 10313	KAM 10.16.76	RLH 11-19-76	TJD
C	D	REVISED PER E.O 10513	KAM 10.16.76	RLH 11-19-76	TJD
	E	CHANGED VIEW A PER EO 10751			
	F	C10 WAS 9100 pF PER EO 10813			
	H	EO 11124			
	J	EO 11193			





E MIDDLE
FF

PRIETARY NOTICE

AND THE TECHNICAL DATA HEREON
ROPRIETARY TO DANA LABORATORIES
NOT WITHOUT EXPRESS WRITTEN PER
LABORATORIES, INC BE USED RE
SED IN WHOLE OR IN PART, OR USED TO
NG FROM A COMPETITIVE SOURCE OR
FACTURE BY ANYONE OTHER THAN
IES, INC. THE INFORMATION HEREON
PED AT PRIVATE EXPENSE AND MAY
PURPOSES OF ENGINEERING EVALUA
CORPORATION INTO TECHNICAL SPECI
HER DOCUMENTS WHICH SPECIFY PRO
ODUCTS FROM DANA LABORATORIES

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403908	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND
INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES
PER USAS Y14.15

MATERIAL
FINISH

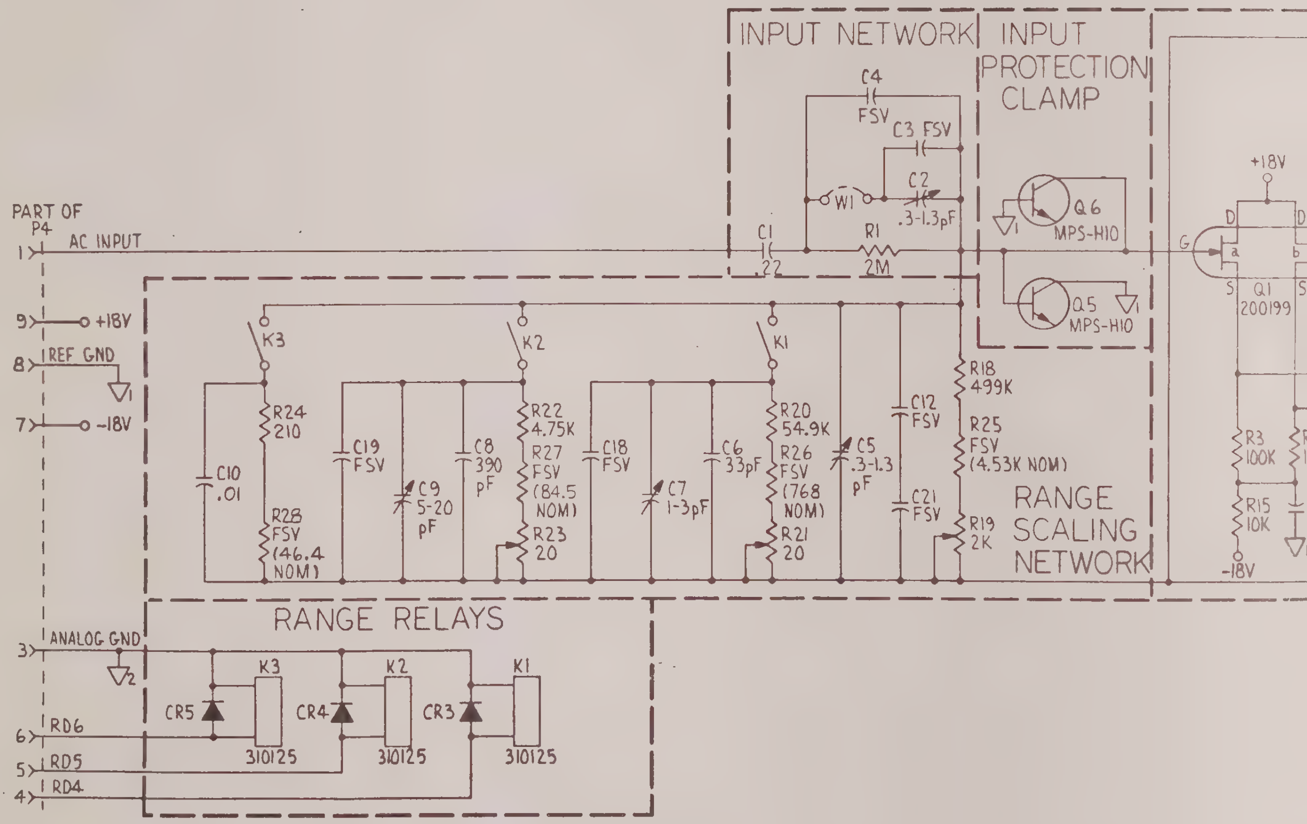
DRAWN	Zimmerman	
CHECK		
DESIGN		
MECH ENGR	Guercio	4-9-76
PROJ ENGR	P. Kolmerz	4-9-76
PROD ENGR		4-9-76

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P.C. BOARD ASSEMBLY
A C AVERAGING CONVERTER
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403905	J

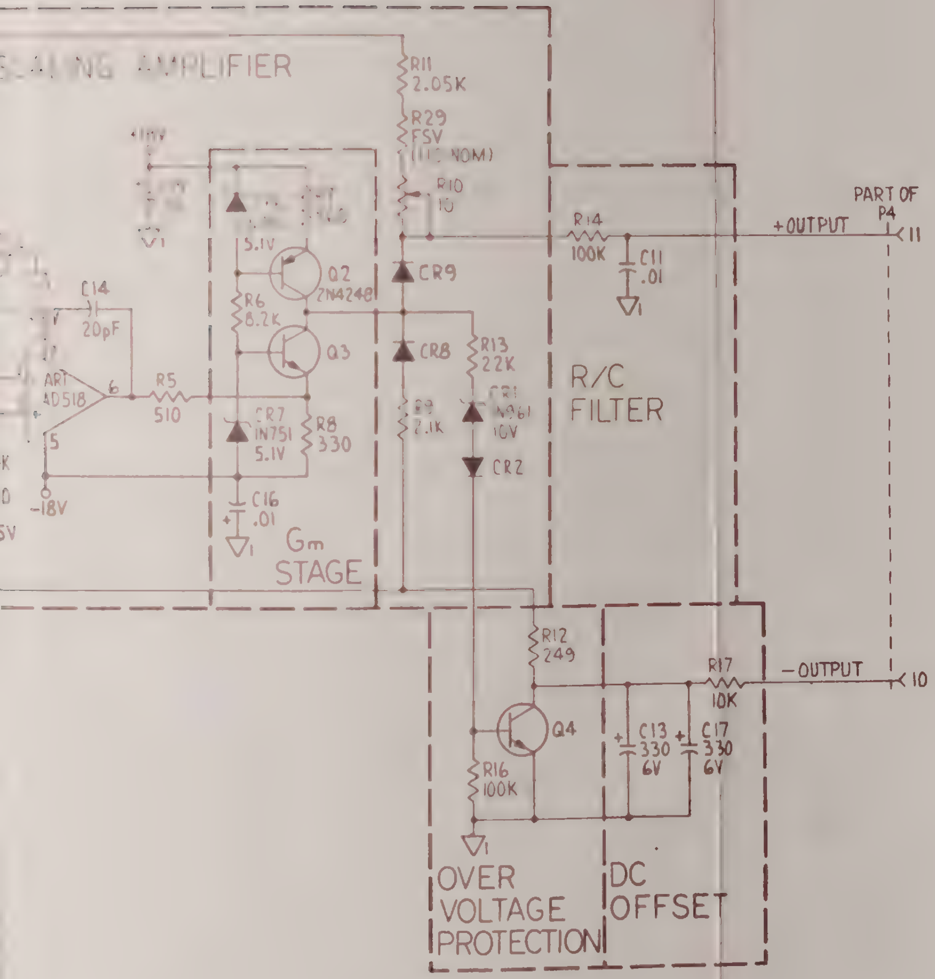
SCALE 2/1
SHEET 1 OF 5


PART OF P4
AC INPUT
1
9 +18V
8 REF GND
7 -18V
3 ANALOG GND
6 RD6
5 RD5
4 RD4
INPUT NETWORK
C4 FSV
C3 FSV
C2 .3-1.3pF
W1
C1 .22
R1 2M
INPUT PROTECTION CLAMP
Q6 MPS-H10
Q5 MPS-H10
+18V
D
G
a
b
S
Q1 200199
R3 100K
R15 10K
-18V
K3
K2
K1
C10 .01
R24 210
R28 FSV (46.4 NOM)
C19 FSV
C9 5-20 pF
C8 390 pF
R22 4.75K
R27 FSV (84.5 NOM)
R23 20
C18 FSV
C7 1-3pF
C6 33pF
R20 54.9K
R26 FSV (768 NOM)
R21 20
C5 .3-1.3 pF
C12 FSV
C21 FSV
R18 499K
R25 FSV (4.53K NOM)
R19 2K
RANGE SCALING NETWORK
RANGE RELAYS
CR5
CR4
CR3
310125
310125
310125

4. TRANSISTORS ARE 200200.
3. DIODES ARE IN916B
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W
NOTES: UNLESS OTHERWISE SPECIFIED

PROP
THIS DOCUMENT AN
ON DISCLOSED, A
LABORATORIES, INC
EXPRESS WRITTEN
RATORIES, INC. BE U
IN WHOLE OR IN PAR
TIONS FROM A COMP
MANUFACTURE BY
LABORATORIES, INC
HAS BEEN DEVELOP
MAY ONLY BE USED
EVALUATION AND
TECHNICAL SPECIFI
MENTS WHICH SPECIF
FROM DANA LABORA

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		REVISIONS			
	B	RELEASED PER DRN #			
	—	REDRAWN WITHOUT CHANGE	PA 10-12 77		
	C	REVISED PER EO 10813	PA 10-12 77		
	D	REVISED PER EO 11193	PA 10-12 77		


SCALING AMPLIFIER
R11
2.05K
R29
FSV
(11Ω NOM)
R10
10
+18V
V1
5.1V
Q2
2N4248
C14
20pF
R6
8.2K
Q3
ART
AD518
6
5
R5
510
CR7
IN751
5.1V
R8
330
-18V
C16
.01
Gm
STAGE
CR9
CR8
R13
22K
R9
2.1K
CR1
IN961
10V
CR2
R14
100K
C11
.01
R/C
FILTER
+OUTPUT
PART OF
P4
11
R12
249
R17
10K
-OUTPUT
10
Q4
R16
100K
C13
330
6V
C17
330
6V
OVER
VOLTAGE
PROTECTION
DC
OFFSET

TARY NOTICE

THE TECHNICAL DATA HERE- PROPRIETARY TO DANA AND SHALL NOT, WITHOUT RMISSION OF DANA LABO- D, RELEASED OR DISCLOSED OR USED TO SOLICIT QUOTA- ITIVE SOURCE OR USED FOR YONE OTHER THAN DANA THE INFORMATION HEREON AT PRIVATE EXPENSE, AND PURPOSES OF ENGINEERING OR INCORPORATION INTO TIONS AND OTHER DOCU PROCUREMENT OF PRODUCTS RIES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403905	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL
FINISH

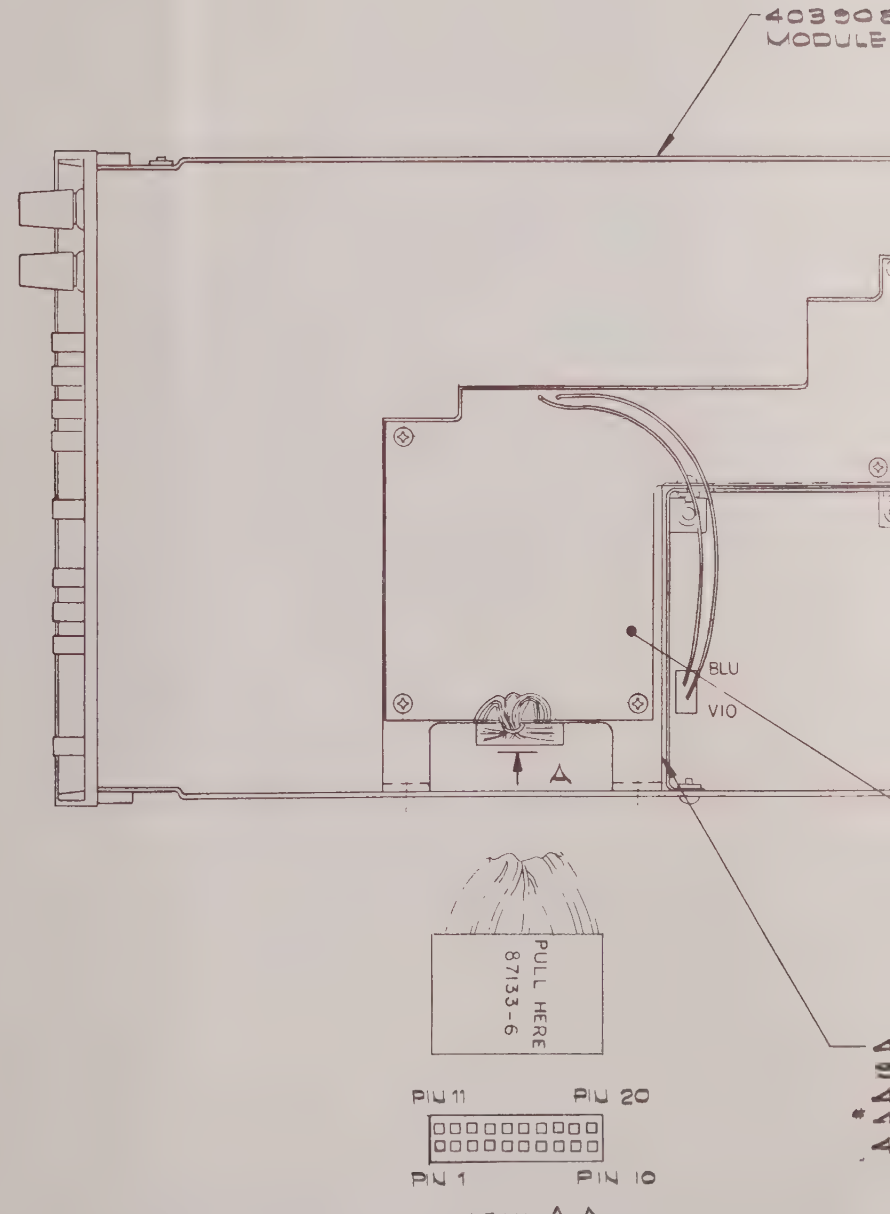
DRAWN	Rich Mays	5-13-77
CHECK	W. Stanton	10-12 77
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC –
AC (AVERAGING) CONVERTER
5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432093	D

SCALE
SHEET 1 OF 1


40390
MODULE
BLU
VIO
A
PULL HERE
87133-6
PIN 11
PIN 20
PIN 1
PIN 10

VIEW A A
SCALE NONE

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN #1121 4/13/76			
B	EO 10312			
C	EO 10381			

SY
403902
P.C.B. ASSY
4-40 PAN HD SCR x 3/16 LG
5. REQ'D
984
LD
D PAN HD SCR x 3/16 LG
CK WASHER
D FLAT HD SCR 3/16 LG
2 REQ'D

	F100		
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

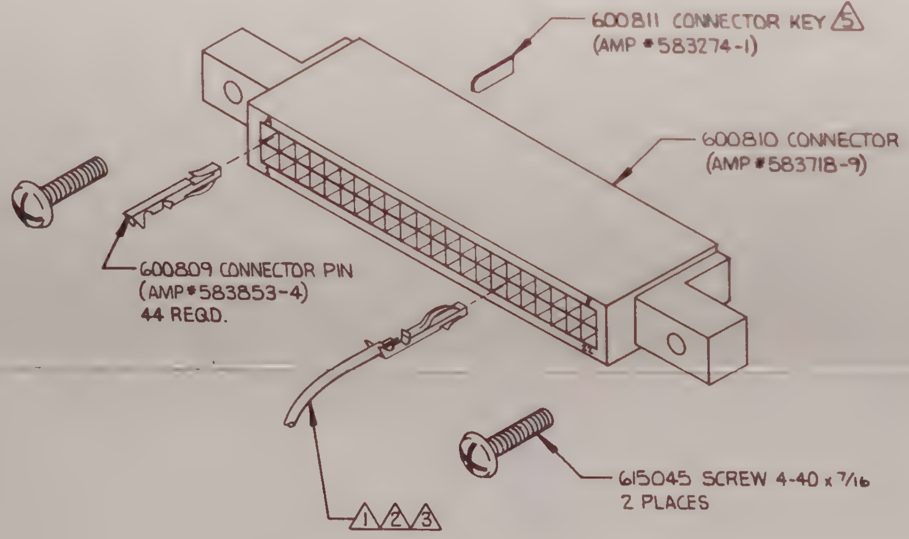
DRAWN		3/15
CHECK		
DESIGN		2/10/76
MECH ENGR		
PROJ ENGR		4.13.76
PROD ENGR		4.13.76

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DATA OUTPUT OPTION

SIZE	CODE IDENT NO.	DWG NO	REV
D	21793	403903	C
SCALE 1/1		SHEET OF 2	

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
	RELEASED PER DRN # [illegible]			


600811 CONNECTOR KEY △5
(AMP #583274-1)
600810 CONNECTOR
(AMP #583718-9)
600809 CONNECTOR PIN
(AMP #583853-4)
44 REQD.
615045 SCREW 4-40 x 7/16
2 PLACES
△1 △2 △3

6. PACKAGE ALL ITEMS IN A 5"x 7" POLY BAG.
△5 INSERT KEY 600811 BETWEEN CONNECTOR POSITIONS D & E.
4 FOR EXTRACTING CONNECTOR PINS USE TOOL NO. 453997 SUPPLIED.
△3 WIRE MAY BE ATTACHED TO CONNECTOR PIN USING AMP HAND TOOL NO. 90272-1 NOT SUPPLIED WITH KIT.
△2 SOLDER WIRE TO CONNECTOR PIN (600809), TABS MUST BE EITHER STRAIGHT UP OR CRIMPED OVER BEFORE INSERTING INTO CONNECTOR (WIRE NOT SUPPLIED).
△1 WIRE RANGE OF CONNECTOR PIN (600809) IS 24-20 AWG.
NOTES: UNLESS OTHERWISE SPECIFIED

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403894	4600		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS	ANGLES	HOLE DIAMETERS
X .030 XX .020 XXX .010	0° 30' FORMED 1° 0'	+.004 -.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

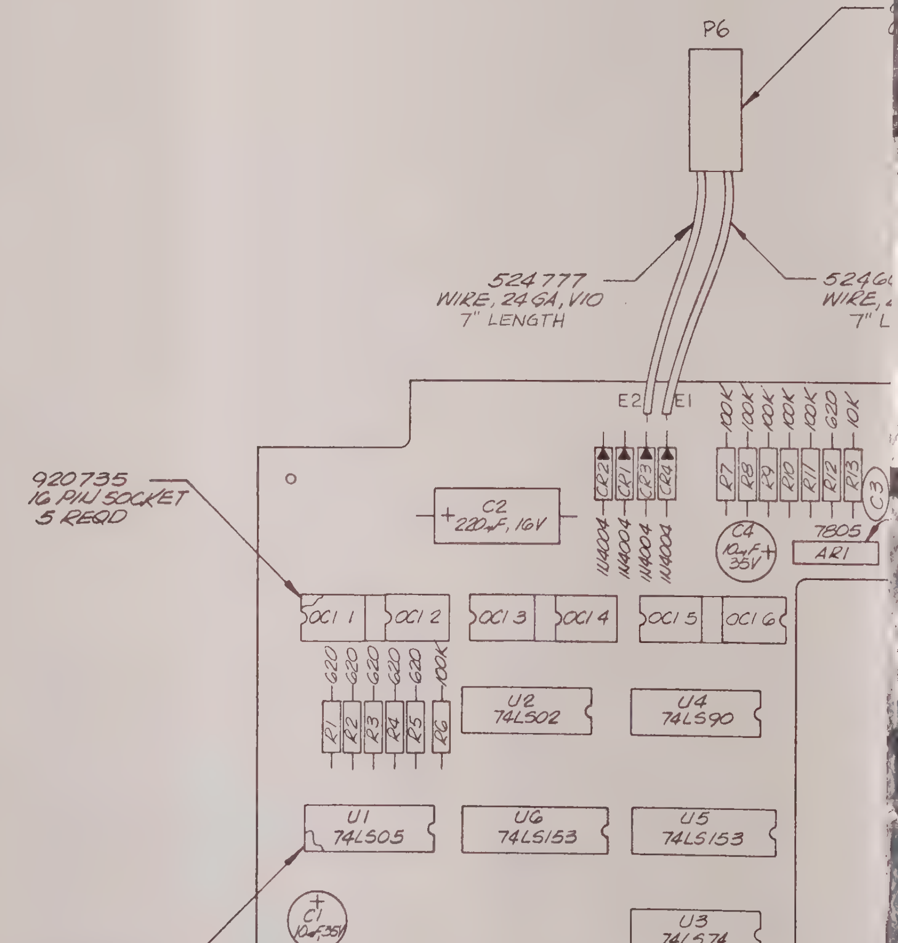
DRAWN	J. Benson	11/4/75
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		11/12/75
PROD ENGR		11/13/75

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SHIPPING KIT-DATA OUTPUT
4600

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	403920	A
SCALE NONE		SHEET 1 OF 2	

DANA 980337 DIETERICH POST CLEARPRINT 1080


P6
524777
WIRE, 24 GA, VIO
7" LENGTH
5246
WIRE,
7" L
E2
E1
920735
16 PIN SOCKET
5 REQD
C2
220µF, 16V
CR2
CR1
CR3
CR4
1N4004
1N4004
1N4004
1N4004
R7
R8
R9
R10
R11
R12
R13
100K
100K
100K
100K
100K
620
10K
C3
C4
10µF
35V
7805
AR1
OC1 1
OC1 2
OC1 3
OC1 4
OC1 5
OC1 6
R1
R2
R3
R4
R5
R6
620
620
620
620
620
100K
U2
74LS02
U4
74LS90
U1
74LS05
U6
74LS153
U5
74LS153
C1
10µF, 35V
U3
74LS74
920734
14 PIN SOCKET
10 REQD
410
PC B
J1
PULL HERE
87133-6
600859 CONNECTOR
600828 CONN PIN - 20 REQD
4
PIN 11
PIN 20
PIN 1
PIN 10

4 NOTE ORIENTATION OF PART NO. AND PIN LOCATION ON CONNECTOR

3. RESISTORS ARE IN OHMS, 5%, 1/4 W

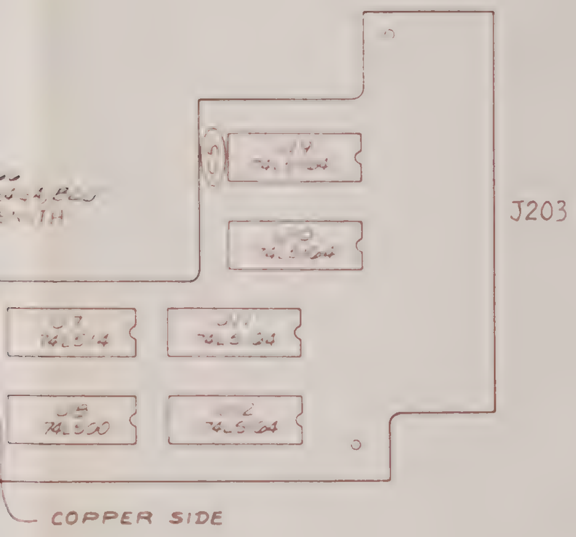
2. SCHEMATIC REF. 432091

1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL

NOTES: UNLESS OTHERWISE SPECIFIED

PCB REV	LTR	DESCRIPTION		DR	CHK	APPD
		REVISIONS				
	A	RELEASED PER DRN # 1120	4/9/76			
C	B	REVISED PER E.O 10311		KAM 8.24.76	RLH 9.24.76	
	C	REVISED PER E.O. 10578				
	D	REVISED PER E.O. 10666				

600860 CONNECTOR
600828 CONN PIN - 2 REQD



719
OARD

403903	5100			
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY	
APPLICATION		QTY REQD		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X 030 XX.020 XXX 010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14 15

MATERIAL
FINISH

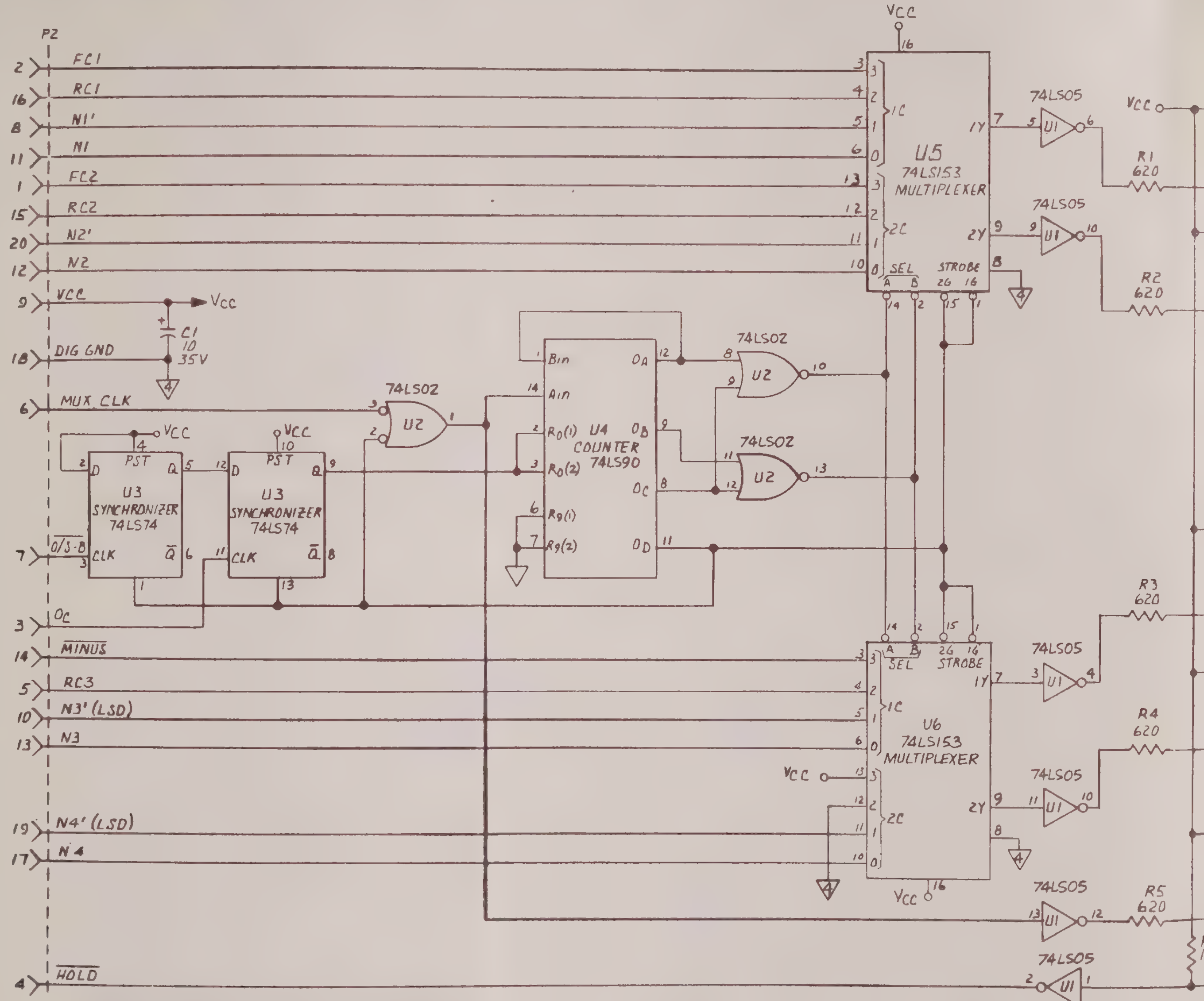
DRAWN		3/15/76
CHECK		
DESIGN		4/9/76
MECH ENGR	Guercio	4-9-76
PROJ ENGR	K Kolinek	4-9-76
PROD ENGR		4-9-76

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY
DATA OUTPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403902	D

SCALE 2/1
SHEET 1 OF 5


P2
2 FC1
16 RC1
8 N1'
11 N1
1 FC2
15 RC2
20 N2'
12 N2
9 VCC
18 DIG GND
6 MUX CLK
7 O/S·B
3 OC
14 MINUS
5 RC3
10 N3' (LSD)
13 N3
19 N4' (LSD)
17 N4
4 HOLD
VCC
C1 10 35V
U5 74LS153 MULTIPLEXER
1C
2C
1Y
2Y
SEL A B
STROBE 2G 1G
U6 74LS153 MULTIPLEXER
74LS05
U1
R1 620
R2 620
R3 620
R4 620
R5 620
74LS02
U2
U4 COUNTER 74LS90
Bin
Ain
R0(1)
R0(2)
R9(1)
R9(2)
QA
QB
QC
QD
U3 SYNCHRONIZER 74LS74
PST
D
Q
CLK
Q̄

REF DESIGNATOR	TYPE	P/N	REMARKS
U1	74LS05	230192	
U2	74LS02	230306	
U3	74LS74	230194	
U4	74LS90	230317	
U5, U6	74LS153	230315	
U7	74LS14	230336	
U8	74LS00	230193	
U9, U10, U11, U12	74LS164	230238	NAT'L ONLY

	POL
+	1
−	0

	FC1	FC2	BINARY WEIGHT
DC	1	1	3
AC	0	1	2
KΩ	1	0	1
KHz	0	0	0

	RC1	RC2	RC3	BINARY WEIGHT
0.2	0	1	0	2
2.0	1	1	0	3
20	0	0	1	4
200	1	0	1	5
2K	0	1	1	6
20K	1	1	1	7

6. PIN 14 ON U1-U3 IS 5 VOLT SUPPLY
5. PIN 7 ON U1-U3 IS COMMON
4. CR1-CR4 1N4004
3. VGG IS A GROUNDED 5 VOLT SUPPLY
2. CAPACITORS ARE IN μF
1. ALL RESISTORS ARE IN OHMS, ±5%, 1/4

NOTES: UNLESS OTHERWISE SPECIFIED

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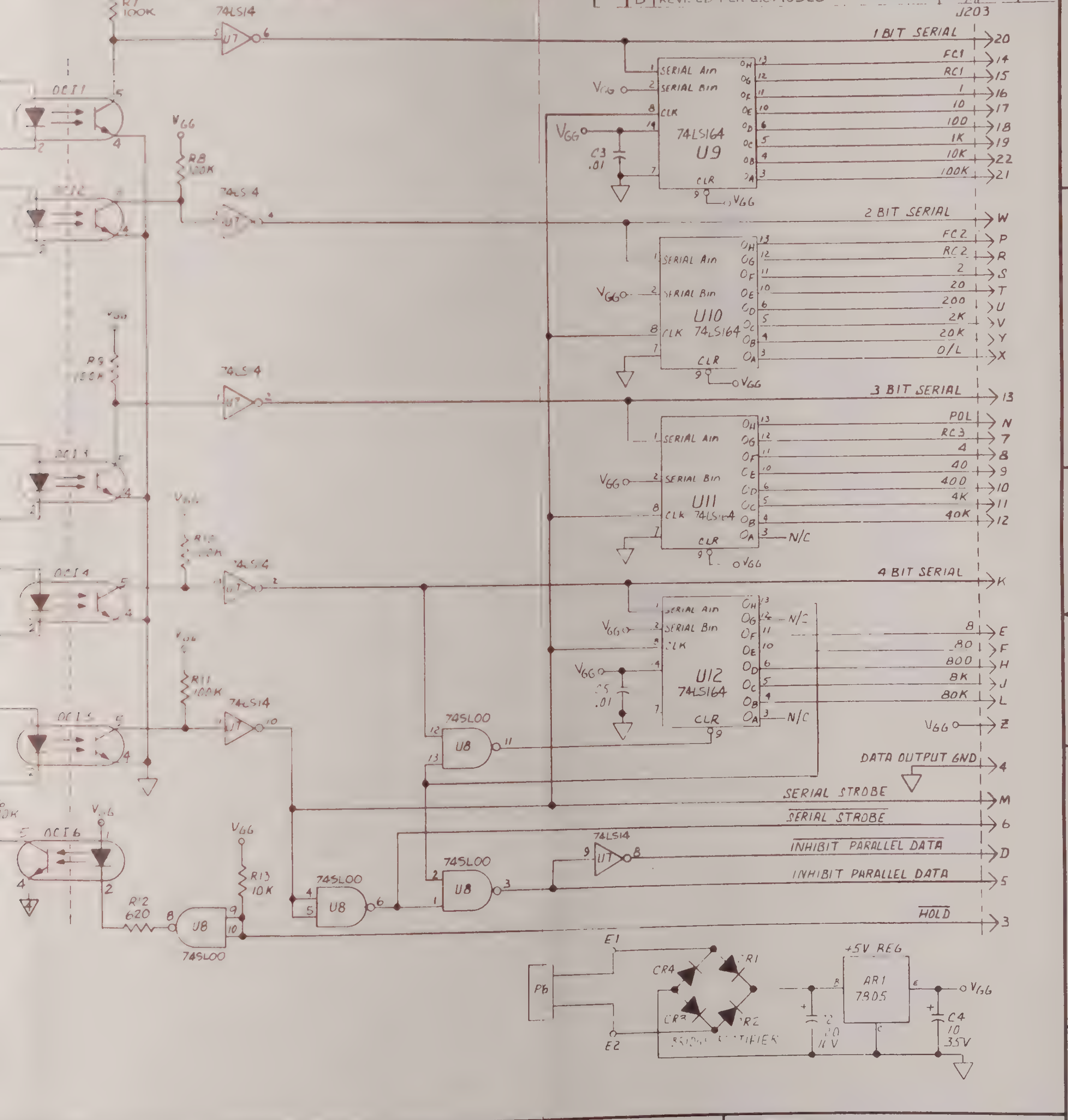
FROM DANA LABORATOR

[illegible]	[illegible] PER E.C. 2666	PA 1/15/77
[illegible]	[illegible]	
E	REVISED PER E.O. 114.5	
F	REVISED PER E.O.	

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN #			
	B	REVISED PER E.O. 10326	PA 11/15/77		


J203
R7 100K
74LS14
U7
1 BIT SERIAL
FC1
RC1
1
10
100
1K
10K
100K
SERIAL Ain
SERIAL Bin
CLK
CLR
74LS164
U9
C3 .01
VGG
OCI1
OCI2
R8 100K
2 BIT SERIAL
FC2
RC2
2
20
200
2K
20K
O/L
U10
74LS164
R9 100K
3 BIT SERIAL
POL
RC3
4
40
400
4K
40K
N/C
U11
OCI3
R10 100K
OCI4
4 BIT SERIAL
8
80
800
8K
80K
U12
C5 .01
R11 100K
OCI5
74S00
U8
DATA OUTPUT GND
SERIAL STROBE
SERIAL STROBE
INHIBIT PARALLEL DATA
INHIBIT PARALLEL DATA
HOLD
OCI6
R12 620
R13 10K
E1
E2
P6
CR1
CR2
CR3
CR4
BRIDGE RECTIFIER
+5V REG
AR1 7805
C2 10 11V
C4 10 35V
20
14
15
16
17
18
19
22
21
W
P
R
S
T
U
V
Y
X
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3

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NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
403902	5100		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	L GREEN	3/12/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR		
PROD ENGR		

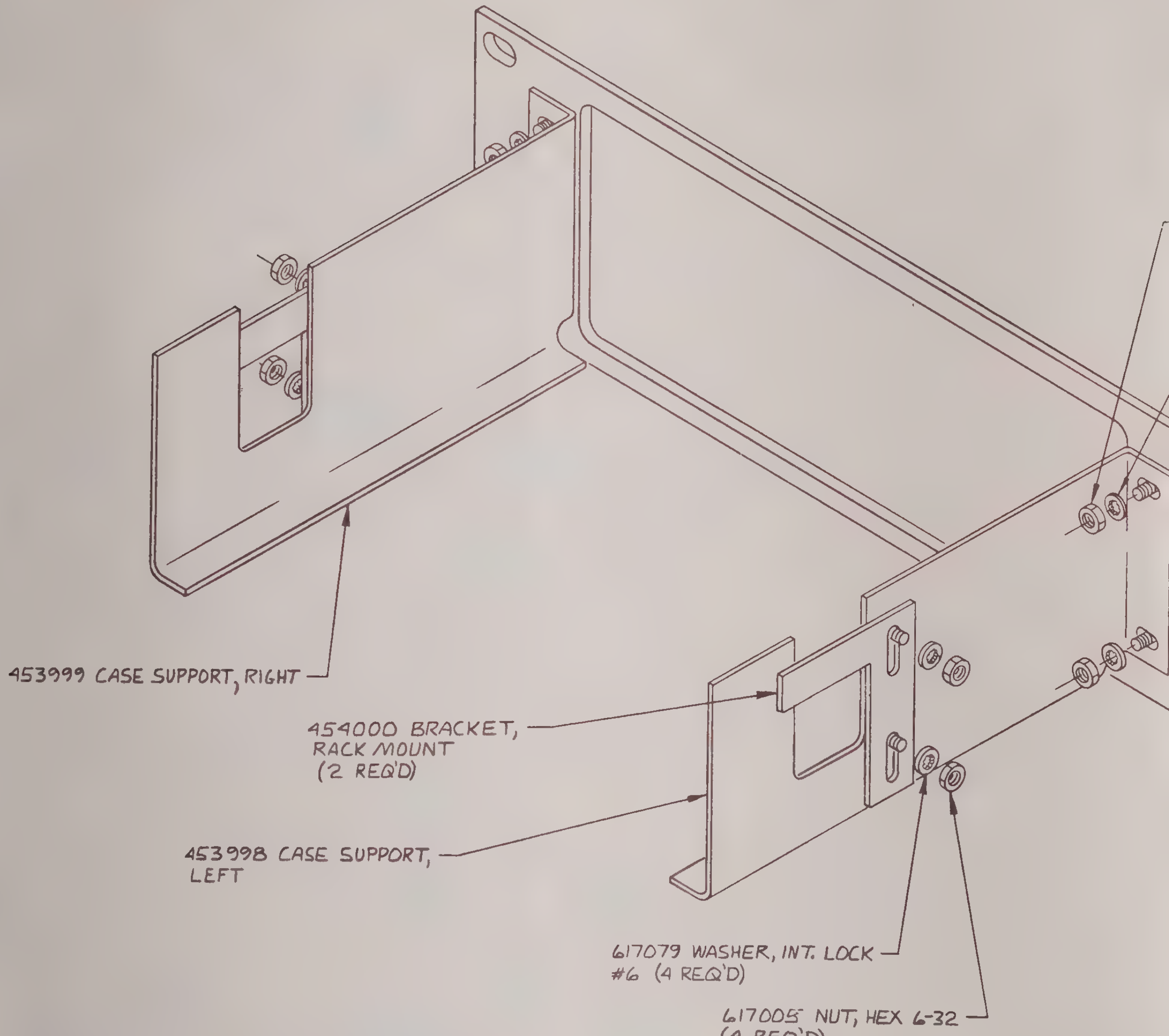
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC -
DATA OUTPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432091	F

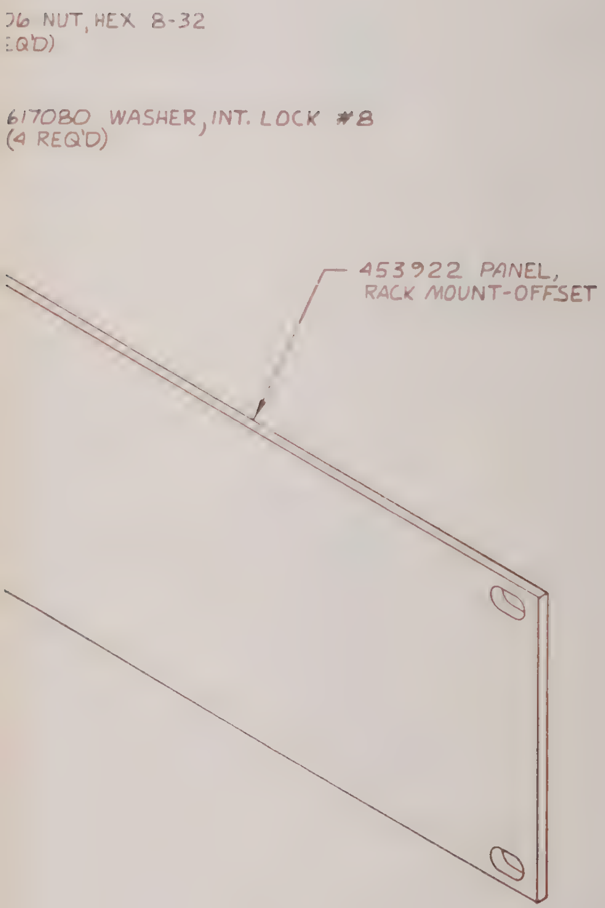
SCALE

SHEET 1 OF 1


453999 CASE SUPPORT, RIGHT
454000 BRACKET, RACK MOUNT (2 REQ'D)
453998 CASE SUPPORT, LEFT
617079 WASHER, INT. LOCK #6 (4 REQ'D)
617005 NUT, HEX 6-32 (4 REQ'D)

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1114 1/22/76			
B	REVISED PER E.O.			


6 NUT, HEX 8-32
EQ'D)
617080 WASHER, INT. LOCK #8
(4 REQ'D)
453922 PANEL,
RACK MOUNT-OFFSET

RIGHT HAND MOUNTING SHOWN

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

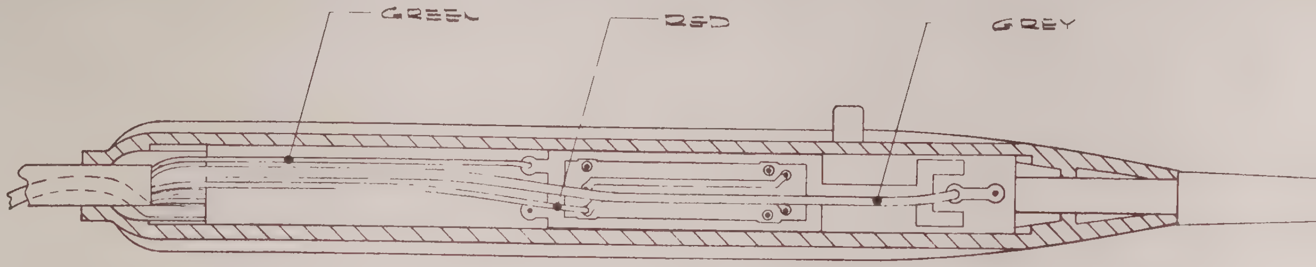
MATERIAL	FINISH

DRAWN	R. Henderson	1/15/76
CHECK		
DESIGN		
MECH ENGR	J. GUERCIO	1-16-76
PROJ ENGR		1/16/76
PROD ENGR		1-22-76

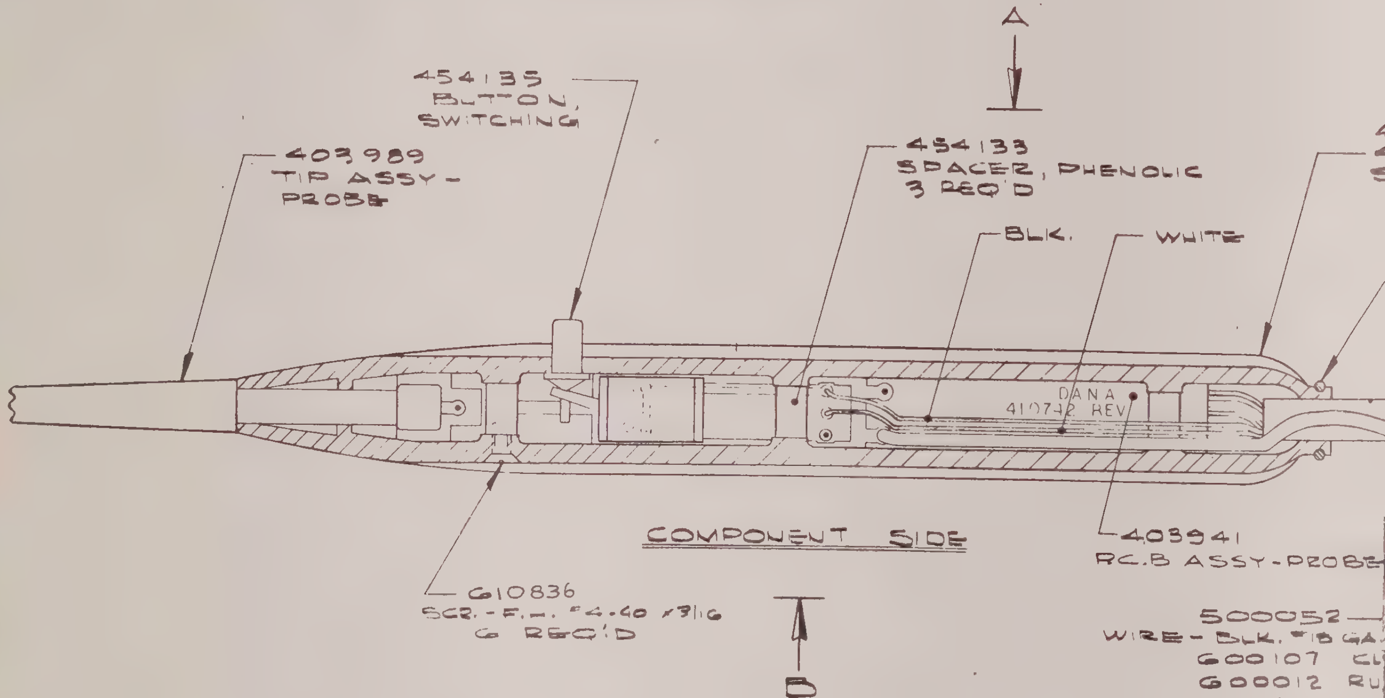
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

RACK MOUNTING OPTION

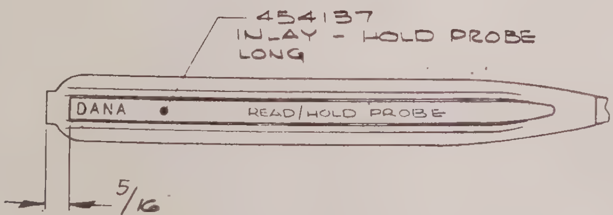
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403892	B
SCALE 1/1		SHEET 1 OF 2	


GREEN
RED
GREY

CIRCUIT SIDE


A
454135
BUTTON, SWITCHING
403989
TIP ASSY-
PROBE
454133
SPACER, PHENOLIC
3 REQ'D
BLK.
WHITE
DANA
410742 REV
403941
P.C.B ASSY-PROBE
610836
SCR.-F.H. #4-40 x 3/16
6 REQ'D
B
500052
WIRE-BLK. #18 GA
600107 CL
600012 RU

COMPONENT SIDE


454137
INLAY - HOLD PROBE
LONG
DANA
READ/HOLD PROBE
5/16

VIEW B
ROTATED 180° C.W.
SCALE 1/1

3. PLACE RETAINER RING OVER COIL CORD AND GROUND LEAD PRIOR TO SOLDERING TO P.C.B.

2. SEE DWG. 432107 FOR SCHEMATIC.

1. SOLDER LEADS AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

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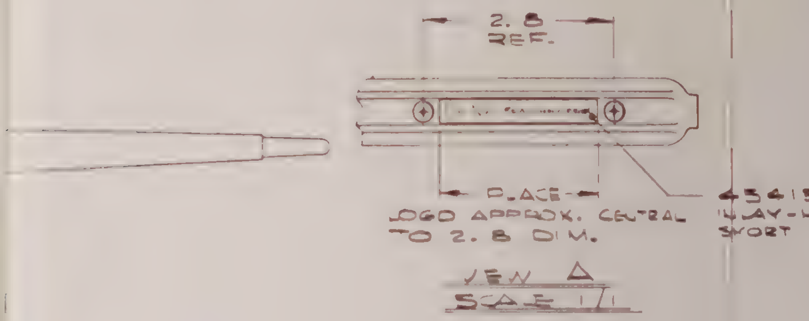
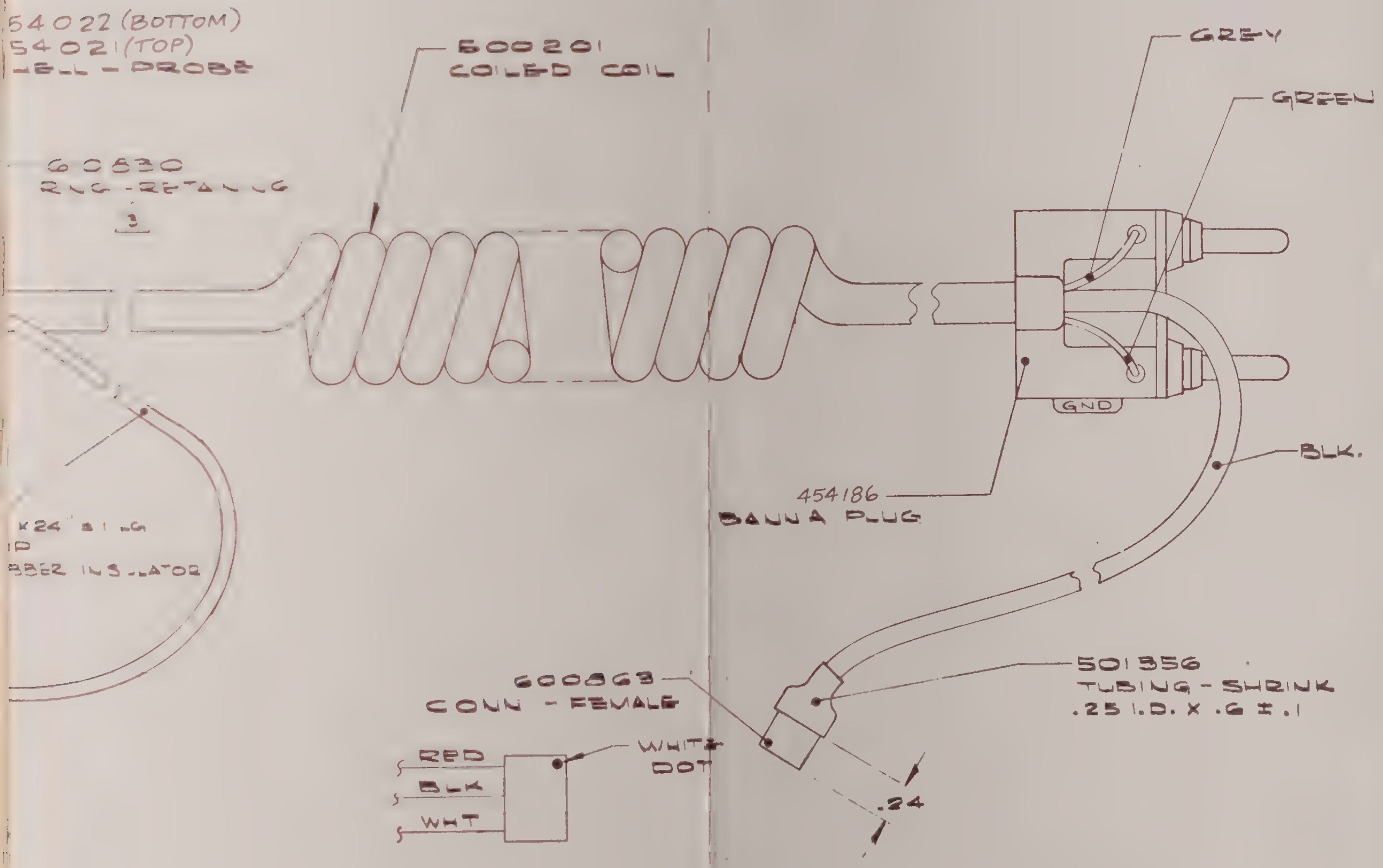
MENTS WHICH SPECIFY P
FROM DANA LABORATO

PCB REV	LTR	DESCRIPTION	DR	CHK	APPD
		RELEASED PER DRN # 1121			
C	B	REVISED + REDRAWN PER EO. 10889	2-22-77	2-25-77	
	C	EO 11032			
	D	EO 11170			
	E	EO 11192			
	F	EO 11249			


2.8
REF.
PLACE
LOGO APPROX. CENTRAL
TO 2.8 DIM.
454156
INLAY-HOLD PROBE,
SHORT
VIEW A
SCALE 1/1


54022 (BOTTOM)
54021 (TOP)
ELL - PROBE
600201
COILED COIL
600830
RING-RETAINING
3
K24 #1 LG
IP
BBER INSULATOR
GREY
GREEN
GND
BLK.
454186
BANNA PLUG
501356
TUBING - SHRINK
.25 I.D. X .6 ± .1
600863
CONN - FEMALE
RED
BLK
WHT
WHITE
DOT
.24

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AT PRIVATE EXPENSE, AND
PURPOSES OF ENGINEERING
IR INCORPORATION INTO
IONS AND OTHER DOCU-
ROCUREMENT OF PRODUCTS
IES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	4600 OPT. 81		
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES

DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN	F. QUON	2-22-77
CHECK		
DESIGN	F QUON	2-22-77
MECH ENGR	Guerrero	3-25-77
PROJ ENGR		
PROD ENGR		

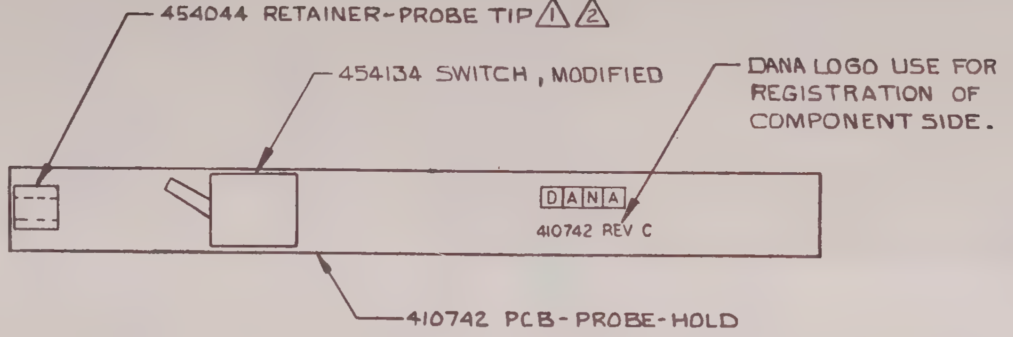
DANA
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSY - PROBE HOLD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403356	F

SCALE 2/1 SHEET 1 OF 2

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1121 4/13/76	mayo		
B	REVISED PER ED. 10881	BKING 3/25/77		5-3-77


454044 RETAINER-PROBE TIP △1 △2
454134 SWITCH, MODIFIED
DANA LOGO USE FOR REGISTRATION OF COMPONENT SIDE.
DANA
410742 REV C
410742 PCB-PROBE-HOLD

△2 SOLDER TO PAD FAR SIDE.

△1 SWAGE IN PLACE FAR SIDE.

NOTES: UNLESS OTHERWISE SPECIFIED

403896	4600 OPT 81	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

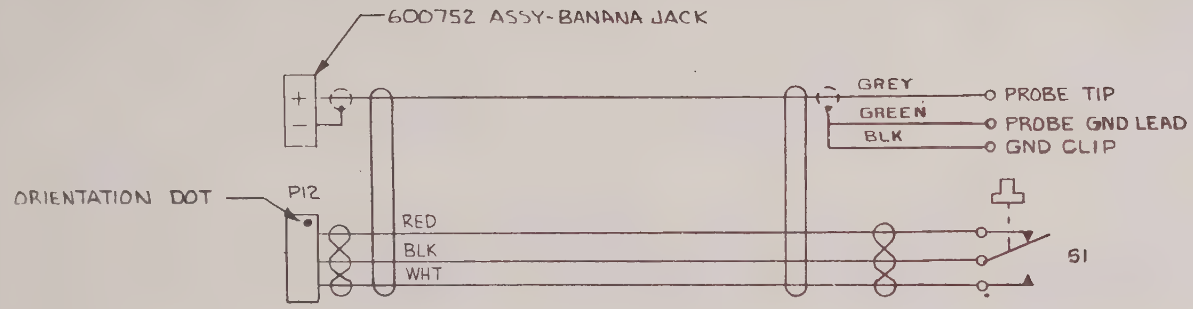
DRAWN	D. Petersen	4-4-76
CHECK	D. Petersen	4-5-76
DESIGN	D. Petersen	4-4-76
MECH ENGR	Guzzcio	4-12-76
PROJ ENGR	J. CROSBY	4/12/76
PROD ENGR		4-12-76

DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY-PROBE, HOLD

SIZE	CODE IDENT. NO	DWG NO.	REV
C	21793	403941	B

REVISIONS					
LTR	DESCRIPTION		DR	CHK	APPD
A	RELEASED PER DRN # 1121	4/13/76			
B	REVISED PER EO 10894			JG	5-4-77 Ⓜ


600752 ASSY-BANANA JACK
+
−
GREY
GREEN
BLK
PROBE TIP
PROBE GND LEAD
GND CLIP
ORIENTATION DOT
P12
RED
BLK
WHT
S1

NOTES: UNLESS OTHERWISE SPECIFIED

403896	4600 OPT81	REF	R+
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS	ANGLES	HOLE DIAMETERS
X.030 XX.020 XXX.010	0° 30′ FORMED 1° 0′	+ .004 − .001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

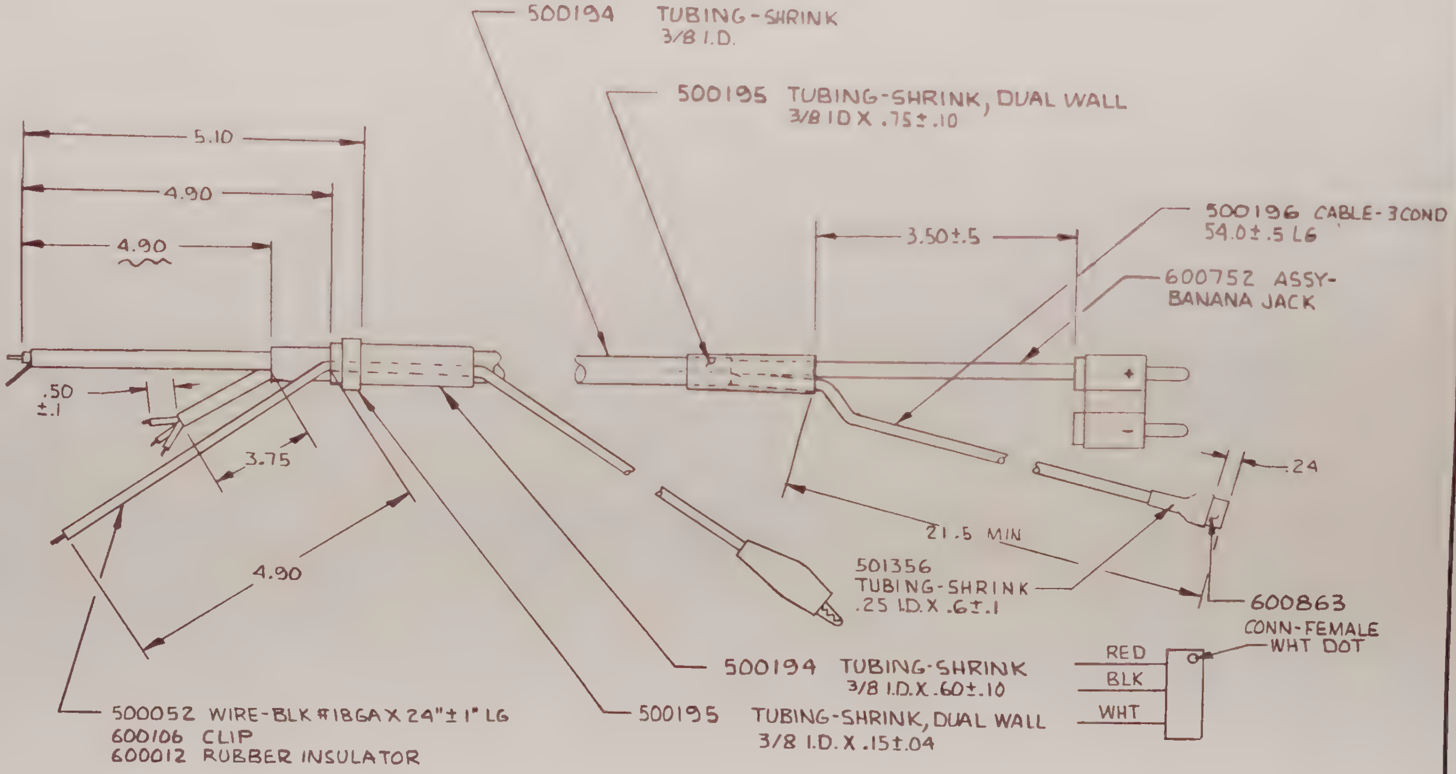
DRAWN	D. Petersen	4-12-76
CHECK	D. Petersen	4-12-76
DESIGN	D. Petersen	4-12-76
MECH ENGR		4-12-76
PROJ ENGR	J. CROSBY	4/12/76
PROD ENGR		4/12/76

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC- PROBE, HOLD

SIZE	CODE IDENT NO.	DWG NO.	REV
C	21793	432107	B
SCALE NONE		SHEET 1 OF 1	

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1121 4/13/76			


500194 TUBING-SHRINK 3/8 I.D.
500195 TUBING-SHRINK, DUAL WALL 3/8 I D X .75±.10
500196 CABLE-3COND 54.0±.5 LG
600752 ASSY-BANANA JACK
5.10
4.90
4.90
3.50±.5
+
-
.24
.50 ±.1
3.75
4.90
21.5 MIN
501356 TUBING-SHRINK .25 I.D. X .6±.1
600863 CONN-FEMALE WHT DOT
RED
BLK
WHT
500194 TUBING-SHRINK 3/8 I.D. X .60±.10
500195 TUBING-SHRINK, DUAL WALL 3/8 I.D. X .15±.04
500052 WIRE-BLK #18GA X 24"±1" LG
600106 CLIP
600012 RUBBER INSULATOR

403896	4600 OPT81	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X 030 XX 020 XXX 010	ANGLES 0 30' FORMED 1° 0'	HOLE DIAMETERS + 004 - 001

DIMENSIONS AND TOLERANCES PER USAS Y14 15

MATERIAL	FINISH

DRAWN	D. Petersen	4-7-76
CHECK	D. Petersen	4-7-76
DESIGN	D. Petersen	4-7-76
MECH ENGR	Guercio	4-12-76
PROJ ENGR	J. CROSBY	4/12/76
PROD ENGR		4-12-76

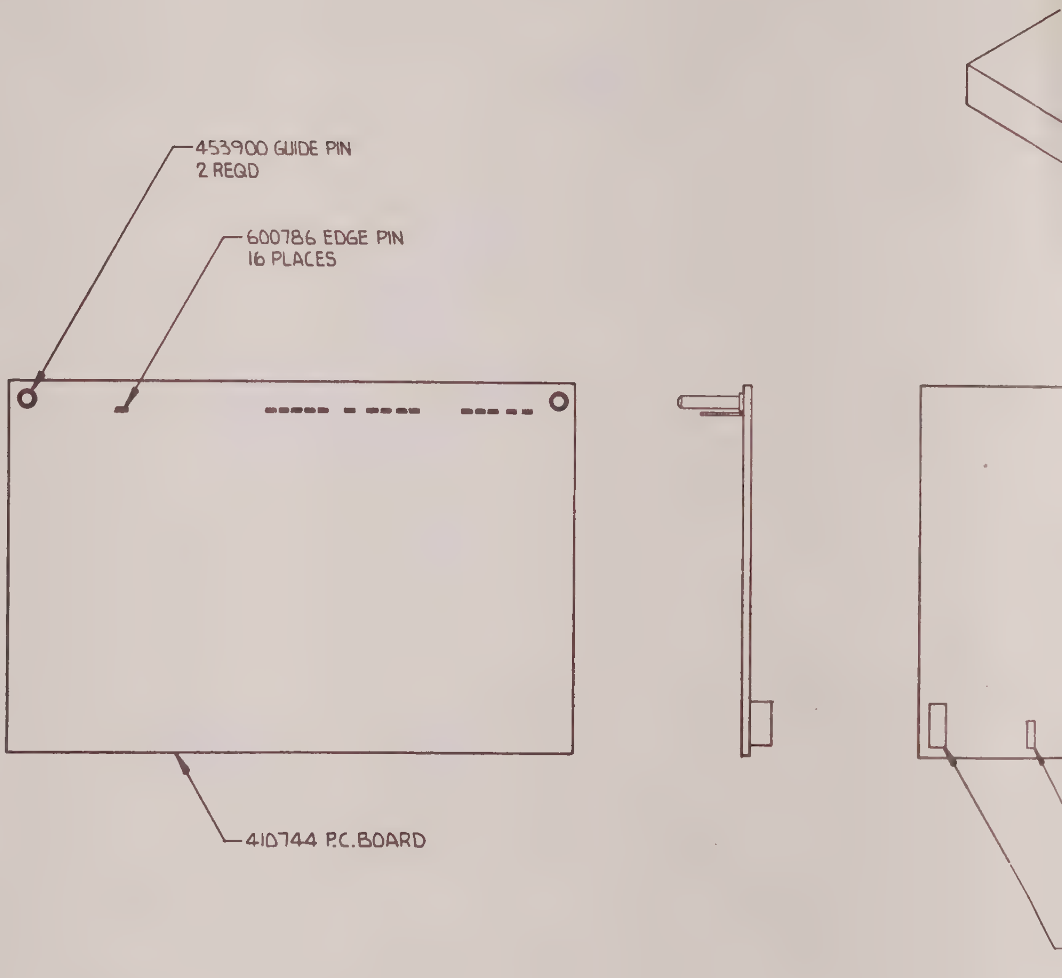
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

CABLE ASSY-PROBE, HOLD

SIZE	CODE IDENT NO	DWG NO.	REV
C	21793	403940	A
SCALE NONE		SHEET 1 OF 2	

NOTES: UNLESS OTHERWISE SPECIFIED

DANA 900237 BISHOP GRAPHICS/ACCUPRESS REORDER NO A 6526


453900 GUIDE PIN
2 REQD
600786 EDGE PIN
16 PLACES
410744 P.C. BOARD

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MENTS WHICH SPECIFY P
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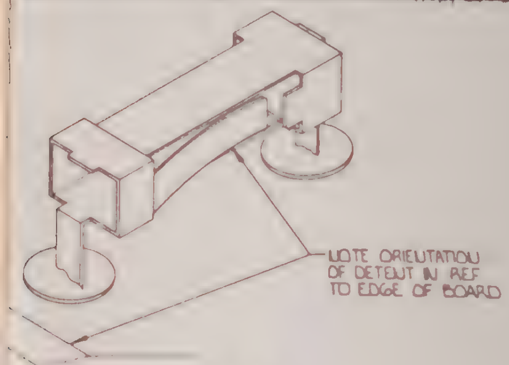
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS					
LTR	DESCRIPTION		DR	CHK	APPD
A	RELEASED PER DRN # 1129	7/8/76	meyer		



DETAIL "A"

600787 RECEPTACLE
16 PLACES
SEE DETAIL "A"

600149 JACK HORIZONTAL
2 PLACES

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PRIVATE EXPENSE, AND
RPOSES OF ENGINEERING
INCORPORATION INTO
S AND OTHER DOCU-
UREMENT OF PRODUCTS
, INC

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

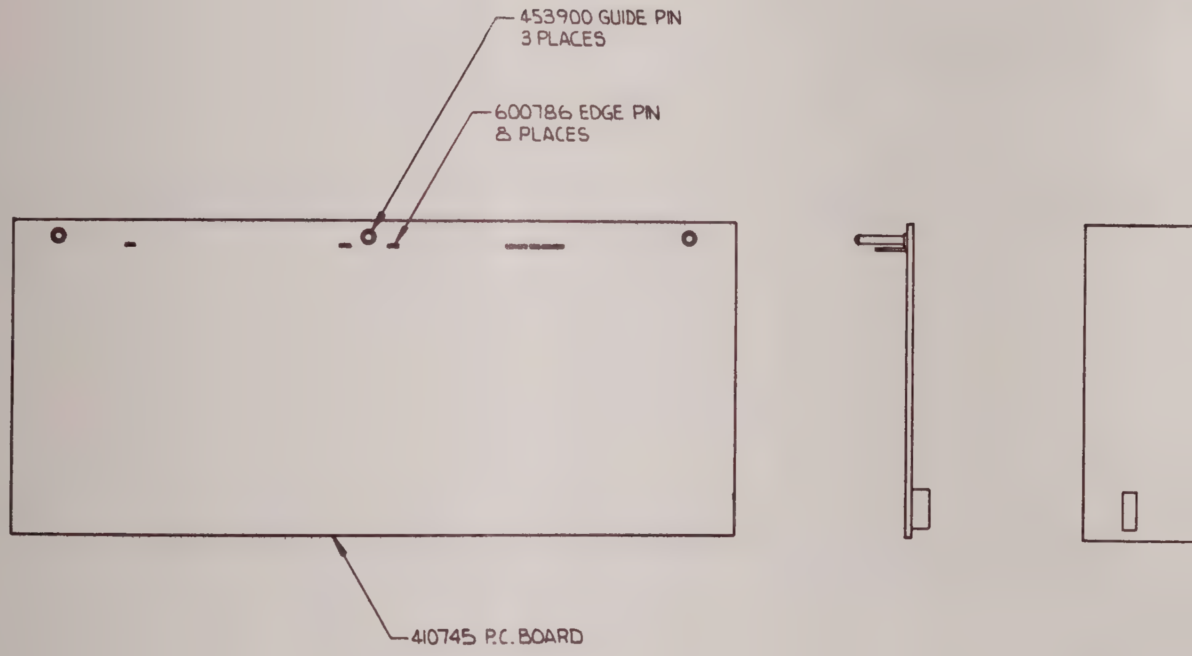
DRAWN	Z. Benson	6/21/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R. Kolemeyer	6/30/76
PROD ENGR		7-7-76

DANA®

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

EXTENDER BOARD ASSY.-ISOLATOR
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403949	A
SCALE NONE		SHEET 1 OF 2	


453900 GUIDE PIN
3 PLACES
600786 EDGE PIN
8 PLACES
410745 P.C. BOARD

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EVALUATION AND
TECHNICAL SPECIFI
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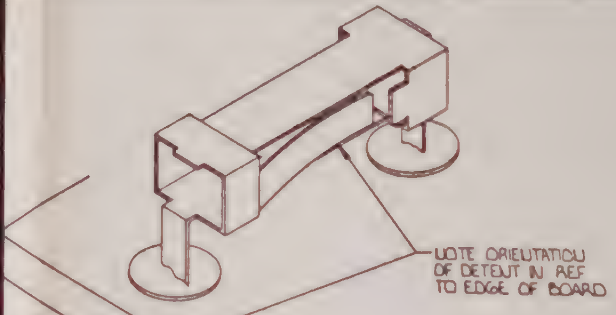
FROM DANA LABORA

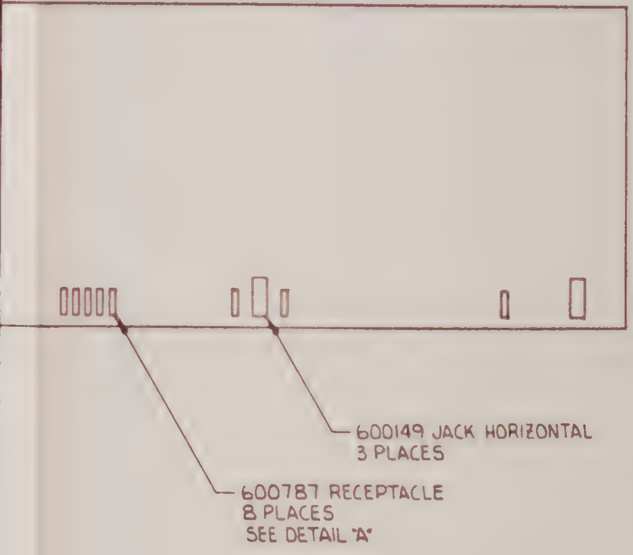
1. ASSEMBLY PROCEEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1129 7/8/76			


NOTE ORIENTATION
OF DETENT IN REF
TO EDGE OF BOARD

DETAIL "A"


600149 JACK HORIZONTAL
3 PLACES
600787 RECEPTACLE
8 PLACES
SEE DETAIL "A"

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OR PURPOSES OF ENGINEERING
FOR INCORPORATION INTO
ATIONS AND OTHER DOCU-
Y PROCUREMENT OF PRODUCTS
TORIES, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30' FORMED 1° 0'	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	Z Brown	4/21/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R Kolenz	6/30/76
PROD ENGR		7-7-76

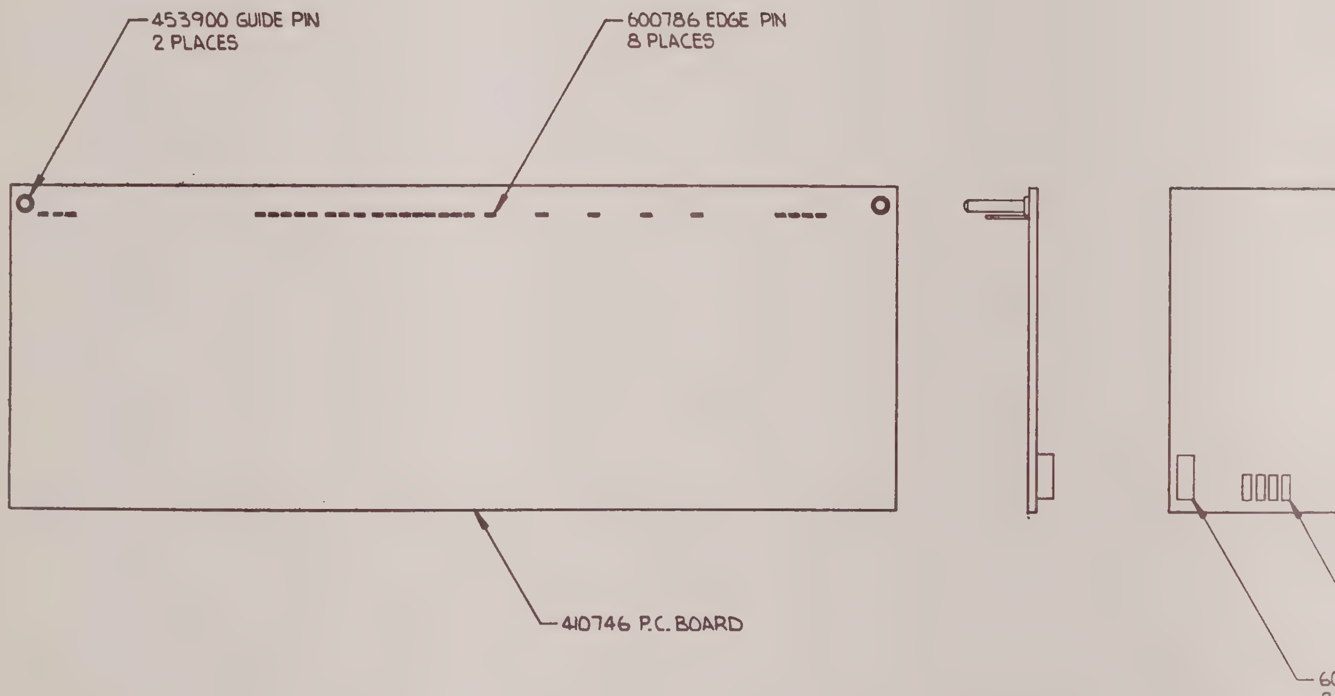
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

EXTENDER BOARD ASSY - A.C.
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403950	A

SCALE NONE

SHEET 1 OF 2


453900 GUIDE PIN
2 PLACES
600786 EDGE PIN
8 PLACES
410746 P.C. BOARD
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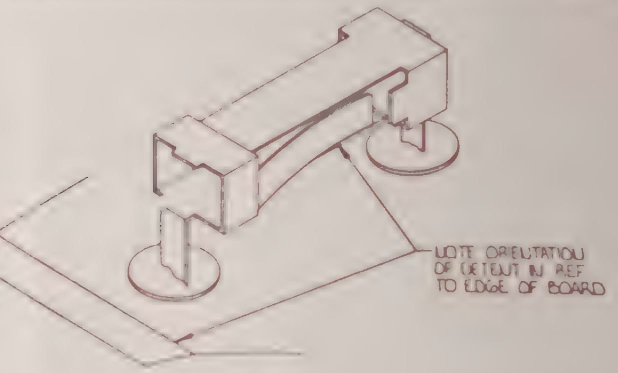
NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPD
A	RELEASED PER DRN # 1129 7/8/76 mayu			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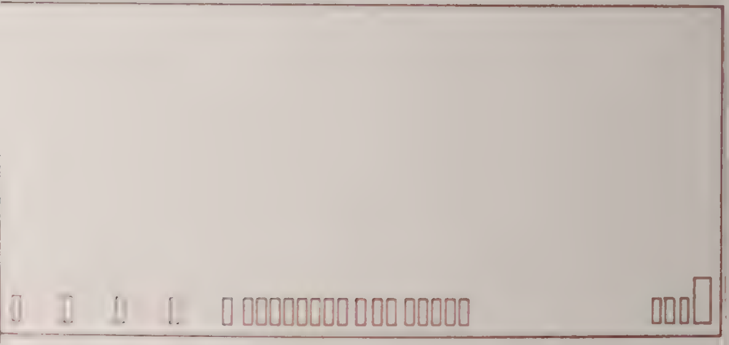
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28 PLACES
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, INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX 020 XXX 010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL

FINISH

DRAWN	J Benson	6/21/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R Kolyngk	6/30/76
PROD ENGR		7-7-76

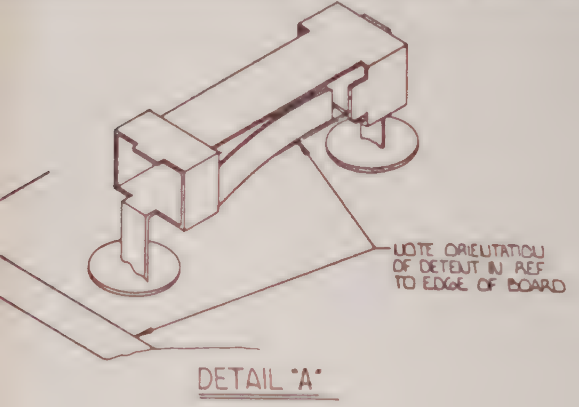
DANA® DANA LABORATORIES INC.
IRVINE, CALIFORNIA

EXTENDER BOARD ASSY.-DIGITIZER
MODEL 5100

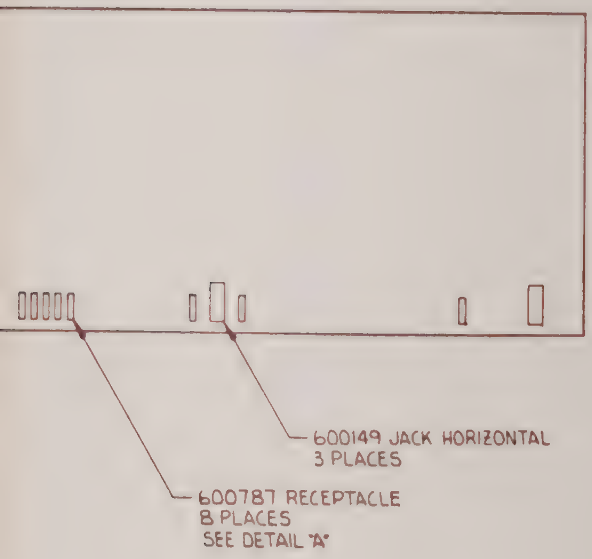
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403951	A

SCALE NONE
SHEET 1 OF 2

REVISIONS					
LTR	DESCRIPTION		DR	CHK	APPD
A	RELEASED PER DRN #1129	7/8/76			


NOTE ORIENTATION OF DETENT IN REF TO EDGE OF BOARD

DETAIL "A"


600149 JACK HORIZONTAL
3 PLACES
600787 RECEPTACLE
8 PLACES
SEE DETAIL "A"

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INCORPORATION INTO
S AND OTHER DOCU-
UREMENT OF PRODUCTS
INC.

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE THICKNESS OF PLATING

TOLERANCES		
DECIMALS X.030 XX.020 XXX.010	ANGLES 0° 30′ FORMED 1° 0′	HOLE DIAMETERS +.004 −.001

DIMENSIONS AND TOLERANCES PER USAS Y14.15

MATERIAL	FINISH

DRAWN		6/21/76
CHECK		
DESIGN		
MECH ENGR		
PROJ ENGR	R Kolyne	6/30/7
PROD ENGR		7-7-76

DANA®

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

EXTENDER BOARD ASSY- A.C.
MODEL 5100

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	403950	A

SCALE NONE

SHEET 1 OF 2

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

Page
Main Logic 7-3
Display 7-7
Digitizer 7-9
Reference Isolator 7-12
Zener Reference Kit 7-15
RMS Converter (Option 10) 7-16
AC Averaging Converter (Option 14) 7-19
Data Output (Option 51) 7-21

7.2 Manufacturers are identified by FSC numbers listed in table 7.2, "List of Suppliers." The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

7.3 Certain parts having 21793 (Dana) listed in the "FSC" column are specially-selected semiconductors. For some of these, standard commercial parts will serve as satisfactory replacements. These Dana parts are identified in table 7.1 along with the commercial equivalent.

Table 7.1

Semiconductor Type:	Equivalent:
018 Diode	Fairchild 1N916B

Table 7.2 - List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PENNSYLVANIA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
04222	AEROVOX CORP. (Hi-Q Division) MYRTLE BEACH, SOUTH CAROLINA
04713	MOTOROLA, INC. (Semi-Conductor Products Division) PHOENIX, ARIZONA
05397	UNION CARBIDE CORP. (Materials Systems Division) CLEVELAND, OHIO
07263	FAIRCHILD (Semiconductor Division) MOUNTAIN VIEW, CALIFORNIA
07388	TOROTEL, INC. GRANDVIEW, MISSOURI
07716	TRW ELECTRONIC COMPONENTS (IRC) BURLINGTON, IOWA
08257	NPC ELECTRONICS CANOGA PARK, CALIFORNIA
09023	CORNELL-DUBILIER ELECTRONICS SANFORD, NORTH CAROLINA
10400	AIRBORNE, INC. DALLAS, TEXAS
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
12406	ELPAC, INC. IRVINE, CALIFORNIA
15636	ELEC-TROL, INC. SAUGUS, CALIFORNIA
21793	DANA LABORATORIES, INC. IRVINE, CALIFORNIA
22045	JORDAN ELECTRIC CO. VAN NUYS, CALIFORNIA
26625	MIAL USA, INC. NUTLEY, NEW JERSEY
26806	AMERICAN ZETTLER, INC. COSTA MESA, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
32293	INTERSIL, INC. CUPERTINO, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (Component Division) HAUPPAUGE, NEW YORK
50434	HEWLETT-PACKARD CO. (HPA Division) PALO ALTO, CALIFORNIA
52763	STETTNER-TRUSH CAZENOVIA, NEW YORK
56289	SPRAGUE ELECTRIC CO. (Pacific Division) LOS ANGELES, CALIFORNIA
71471	AEROVOX CORP. (Cinema Plant) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
72136	ELECTRO MOTIVE MFG. CO., INC. WILLIMANTIC, CONNECTICUT
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, LONG ISLAND, NEW YORK
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
80294	BOURNS, INC. RIVERSIDE, CALIFORNIA
81349	MILITARY SPECIFICATION
86884	RCA (Electronics Components Division) HARRISON, NEW JERSEY

403907 – Assy., PCB, MAIN LOGIC & INTERCONNECTION

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR2	230301	INTEGRATED CIRCUIT	04713	MC7905CP
AR5	230103	INTEGRATED CIRCUIT	27014	LM308
C1	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C2	100101	CAP CERAM 33 PFD 1000 V 5%	56289	C030B102F330J
C3	101145	CAP CERAM 100 PFD 500 V 10%	04222	TCD-DI-1N5600-100
C4	100046	CAP CERAM .01 MFD 1000 V 20%	56289	C023B102K103M
C5	100052	CAP CERAM 22 PFD 1000 V 5%	56289	C030B102F220J
C7	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C8	100126	CAP CERAM 680 PFD 1000 V 20%	56289	C023B102E681M
C9	100071	CAP CERAM .001 MFD 1000 V 20%	56289	C023B102E102M
C10	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C11	101145	CAP CERAM 100 PFD 500 V 10%	04222	TCD-DI-1N5600-100
C12	110170	CAP ELECT 3.3 MFD 350 V 10%		350VB3.3
C13	110170	CAP ELECT 3.3 MFD 350 V 10%		350VB3.3
C14	110185	CAP ELECT 4700 MFD 16 V		16TAL4700
C15	110172	CAP ELECT 470 MFD 35 V		35VBSL470
C16	110172	CAP ELECT 470 MFD 35 V		35VBSL470
C17	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C18	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C19	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C20	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C21	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C22	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C23	100071	CAP CERAM .001 MFD 1000 V 20%	56289	C023B102E102M
C24	100124	CAP CERAM 330 PFD 1000 V 20%	56289	C023B102E331M
C25	100101	CAP CERAM 33 PFD 1000 V 5%	56289	C030B102F330J
C26	120339	CAP POLY .22 MFD 200 V 5%	12406	P2A224J
C27	120290	CAP MYLAR .22 MFD 100 V 20%	73445	C281AH/A220K
C28	120339	CAP POLY .22 MFD 200 V 5%	12406	P2A224J
C29	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C30	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C31	100062	CAP CERAM .01 MFD 100 V 10%	72982	8121-100-W5R0-103K
C32	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C33	100063	CAP CERAM .01 MFD 500 V 20%	56289	C023B501E103M
C34	100063	CAP CERAM .01 MFD 500 V 20%	56289	C023B501E103M
C35	100068	CAP CERAM .02 MFD 100 V 20%	56289	C023B101H203M
C36	100068	CAP CERAM .02 MFD 100 V 20%	56289	C023B101H203M
C37	121091	CAP MYLAR .033 MFD 100 V 10%	09023	WMF1S33
C40	100062	CAP CERAM .01 MFD 100 V 10%	72982	8121-100-W5R0-103K
CR1	211083	DIODE SILICO 018	21793	211083
CR2	211083	DIODE SILICO 018	21793	211083

403907 Assy., PCB, MAIN LOGIC & INTERCONNECTION *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR5	210004	DIODE SILICO	81349	1N4004
CR6	210004	DIODE SILICO	81349	1N4004
CR7	210004	DIODE SILICO	81349	1N4004
CR8	210004	DIODE SILICO	81349	1N4004
CR9	210004	DIODE SILICO	81349	1N4004
CR10	210004	DIODE SILICO	81349	1N4004
CR11	210004	DIODE SILICO	81349	1N4004
CR12	210004	DIODE SILICO	81349	1N4004
CR13	210004	DIODE SILICO	81349	1N4004
CR14	210004	DIODE SILICO	81349	1N4004
CR15	220004	DIODE SILICO ZENER	81349	1N961B
CR16	220015	DIODE SILICO ZENER	81349	1N967A
CR17	211083	DIODE SILICO 018	21793	211083
CR18	211083	DIODE SILICO 018	21793	211083
CR19	211083	DIODE SILICO 018	21793	211083
CR20	211083	DIODE SILICO 018	21793	211083
J1	600821	CONN 6 PIN	27264	09-03-1062
J202	600789	CONN MALE, 3 CONTACTS	10400	WT3PRD7
K1	310130	RELAY 1 KV CONTACTS, 5V COIL	26806	AZ-420-217-200
K2	310130	RELAY 1 KV CONTACTS, 5V COIL	26806	AZ-420-217-200
Q1	200230	TRANS FET N-CHAN, SIL JUNCTION		E305
Q2	200099	TRANS	81349	2N4258
Q3	200197	TRANS SILICO NPN	04713	MPS-H10
Q4	200197	TRANS SILICO NPN	04713	MPS-H10
Q5	200099	TRANS	81349	2N4258
Q6	200068	TRANS PNP	80131	2N4250
R1	000154	RES CARBON 150 K 5% 1/4W	81349	RC07GF154J
R2	000753	RES CARBON 75 K 5% 1/4W	81349	RC07GF753J
R3	000226	RES CARBON 22 M 5% 1/4W	81349	RC07GF226J
R4	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R5	001887	RES CARBON 510 K 5% 1/2W	81349	RC20GF514J
R6	000514	RES CARBON 510 K 5% 1/4W	81349	RC07GF514J
R7	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R8	000152	RES CARBON 1.5 K 5% 1/4W	81349	RC07GF152J
R9	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R10	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J

403907 – Assy., PCB, MAIN LOGIC & INTERCONNECTION *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R12	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R13	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R14	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R15	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R16	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R17	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R18	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R21	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R23	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R24	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R25	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R26	020688	RES SET, PRECISION, W/R27	21793	020688
R27	020688	RES SET, PRECISION, W/R26	21793	020688
R28	030005	RES CARBON 100 K 5% 2 W	81349	RC42GF104J
R29	030005	RES CARBON 100 K 5% 2 W	81349	RC42GF104J
R30	000204	RES CARBON 200 K 5% 1/4W	81349	RC07GF204J
R31	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R32	040233	POT CERMET 20 K 10%	73138	89PR20K
R33	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R34	040196	POT CERMET 1 K 20%	11237	360T102B
R35	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R36	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R37	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R38	000122	RES CARBON 1.2 K 5% 1/4W	81349	RC07GF122J
R39	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R40	000241	RES CARBON 240 OHM 5% 1/4W	81349	RC07GF241J
R41	000122	RES CARBON 1.2 K 5% 1/4W	81349	RC07GF122J
R42	000161	RES CARBON 160 OHM 5% 1/4W	81349	RC07GF161J
R43	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
S11	600778	SWITCH, PUSHBUTTON	71590	PBI Series
T1	300083	TRANSFORMER, POWER	21793	300083
U1	230195	INTEGRATED CIRCUIT	27014	CMOS74C04N
U2	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U3	230217	INTEGRATED CIRCUIT	01295	SN74490N
U4	230196	INTEGRATED CIRCUIT	01295	SN74LS51N
U5	230234	INTEGRATED CIRCUIT	01295	SN74LS04N
U6	230108	INTEGRATED CIRCUIT	01295	SN7416N
U7	230314	INTEGRATED CIRCUIT	01295	SN74LS75
U8	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U9	230194	INTEGRATED CIRCUIT	01295	SN74LS74N

403907 – Assy., PCB, MAIN LOGIC & INTERCONNECTION *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U10	230120	INTEGRATED CIRCUIT	07263	3814
U11	230237	INTEGRATED CIRCUIT	01295	SN74LS123N
U12	230305	INTEGRATED CIRCUIT	01295	SN74LS08
U13	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U14	230248	INTEGRATED CIRCUIT	01295	SN74LS10N
U15	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U16	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U17	230306	INTEGRATED CIRCUIT	01295	SN74LS02
U18	230152	INTEGRATED CIRCUIT	07263	7416
U19	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U20	230312	INTEGRATED CIRCUIT	01295	SN74193N
U21	230300	INTEGRATED CIRCUIT ROM	32293	IM5600C-PE
U22	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U23	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
Y1	920761	CRYSTAL 1 MHz	07388	X01677-2
Z1	080005	RES CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z2	080005	RES CERMET 10 K NETWORK 2%	11237	750-61-R10K
Z3	080005	RES CERMET 10 K NETWORK 2%	11237	750-61-R10K

403855 – Assy., PCB, DISPLAY

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR1	210004	DIODE SILICO	81349	1N4004
CR2	210004	DIODE SILICO	81349	1N4004
LED 1	210082	DIODE LED DISPLAY	50434	HP5082-7662
LED 2	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
LED 3	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
LED 4	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
LED 5	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
LED 6	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
LED 7	210074	DIODE LED DISPLAY 7 SEG - YELLOW	50434	HP5082-7660
Q1	200184	TRANS PNP	04713	MPSA55
Q2	200184	TRANS PNP	04713	MPSA55
Q3	200184	TRANS PNP	04713	MPSA55
Q4	200184	TRANS PNP	04713	MPSA55
Q5	200184	TRANS PNP	04713	MPSA55
Q6	200184	TRANS PNP	04713	MPSA55
R1	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R2	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R3	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R4	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R5	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
R6	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R7	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R8	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R9	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R10	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R11	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R12	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R13	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R14	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R15	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R16	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R17	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R18	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R19	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R20	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R21	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R22	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R23	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R24	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J

403855 – Assy., PCB, DISPLAY *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R25	000470	RES CARBON 47 OHM 5% 1/4W	81349	RC07GF470J
R26	000151	RES CARBON 150 OHM 5% 1/4W	81349	RC07GF151J
R27	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R28	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R29	000821	RES CARBON 820 OHM 5% 1/4W	81349	RC07GF821J
U1	230192	INTEGRATED CIRCUIT	01295	SN74LS05N
U2	230071	INTEGRATED CIRCUIT	07263	7445
U3	230132	INTEGRATED CIRCUIT	07263	7447
U4	230132	INTEGRATED CIRCUIT	07263	7447

403906 – Assy., PCB, DIGITIZER

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230103	INTEGRATED CIRCUIT	27014	LM308
AR2	230324	INTEGRATED CIRCUIT OP AMP FET	27014	LF356H
AR3	230331	INTEGRATED CIRCUIT	27014	LF355H
AR4	230110	INTEGRATED CIRCUIT OP AMP	27014	LM301A
AR5	230307	INTEGRATED CIRCUIT VOLTAGE COMPARATOR	27014	LM311H
AR6	230118	INTEGRATED CIRCUIT NPN	86884	CA3086
C1	110190	CAP TANTA 10 MFD 50 V	21793	110190
C2	110159	CAP TANTA 33 MFD 10 V 10%	05397	T368B336K010AS
C3	120184	CAP POLY 1000 PFD 1000 V 5%	26625	611
C4	120321	CAP MYLAR .047 MFD 250 V 10%	73445	C281AB/A47K
C5	100071	CAP CERAM .001 MFD 1000 V 20%	56289	C023B102E102M
C6	100088	CAP CERAM 220 PFD 100 V 5%	72982	8121-M100-C0G221J
C7	120335	CAP POLY 4.7 MFD 63 V 10%	52763	MKC1860-547/06
C8	120341	CAP MET MYLAR 33 MFD 200 V 10%	07716	X363
C10	120286	CAP MYLAR .1 MFD 100 V 20%	73445	C281AH/A100K
C11	100125	CAP CERAM 10 PFD 1000 V 20%	56289	C023B102E100M
C12	100120	CAP CERAM 270 PFD 1000 V 20%	56289	C023B102E271M
CR1	211083	DIODE SILICO 018	21793	211083
CR2	211083	DIODE SILICO 018	21793	211083
CR3	211083	DIODE SILICO 018	21793	211083
CR4	210058	DIODE SILICO	81349	1N458
CR5	210058	DIODE SILICO	81349	1N458
CR8	211083	DIODE SILICO 018	21793	211083
CR9	211083	DIODE SILICO 018	21793	211083
CR10	220004	DIODE SILICO ZENER	81349	1N961B
CR11	211083	DIODE SILICO 018	21793	211083
CR12	211083	DIODE SILICO 018	21793	211083
CR13	211083	DIODE SILICO 018	21793	211083
CR14	211083	DIODE SILICO 018	21793	211083
CR15	211083	DIODE SILICO 018	21793	211083
CR16	211083	DIODE SILICO 018	21793	211083
CR17	211083	DIODE SILICO 018	21793	211083
CR18	211083	DIODE SILICO 018	21793	211083
CR19	220004	DIODE SILICO ZENER	81349	1N961B
K1	310125	RELAY REED 1 FORM A 5 V	21793	310125
K2	310125	RELAY REED 1 FORM A 5 V	21793	310125
K3	310125	RELAY REED 1 FORM A 5 V.	21793	310125

403906 – Assy., PCB, DIGITIZER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q1	200129	TRANS SILICO NPN	07263	SE4020
Q2	200129	TRANS SILICO NPN	07263	SE4020
Q3	200199	TRANS FET	27014	FM1302
Q4	200199	TRANS FET	27014	FM1302
Q5	200159	TRANS SILICO NPN	21793	200159
Q6	200159	TRANS SILICO NPN	21793	200159
Q7	200200	TRANS NPN	21793	200200
Q8	200068	TRANS PNP	80131	2N4250
Q9	200198	TRANS PNP	04713	MPS-A92
Q10	200198	TRANS PNP	04713	MPS-A92
Q11	200248	TRANS	21793	200248
Q12	200248	TRANS	21793	200248
Q13	200129	TRANS SILICO NPN	07263	SE4020
R1	040238	POT CERMET 500 K 10%	73138	89PR500K
R2	040266	POT CERMET 500 K 20% 1/2W	73138	72XW500K
R3	000205	RES CARBON 2 M 5% 1/4W	81349	RC07GF205J
R4	000515	RES CARBON 5.1 M 5% 1/4W	81349	RC07GF515J
R5	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R6	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R7	001887	RES CARBON 510 K 5% 1/2W	81349	RC20GF514J
R8	001887	RES CARBON 510 K 5% 1/2W	81349	RC20GF514J
R9	010013	RES METAL 60.4 K T-2 1% 1/8W	81349	RN60C6042F
R10	010392	RES METAL 20 K .1% 1/10W	81349	RN55C2002B
R11	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R12	001737	RES CARBON FSV 5% 1/4W	21793	001737
R13	001737	RES CARBON FSV 5% 1/4W	21793	001737
R14	010639	RES METAL 20 K .1% 1/10W	81349	RN55E2002B
R15	010639	RES METAL 20 K .1% 1/10W	81349	RN55E2002B
R16	040257	POT CERMET 50 OHM 20% 1/2W	80294	3389S-500
R17	000471	RES CARBON 470 OHM 5% 1/4W	81349	RC07GF471J
R18	001737	RES CARBON FSV 5% 1/4W	21793	001737
R19	001737	RES CARBON FSV 5% 1/4W	21793	001737
R20	012025	RES METAL 301 K 1% 1/8W	81349	RN60C3013F
R21	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R22	010257	RES METAL 365 K 1% 1/8W	81349	RN60C3653F
R23	040182	POT CERMET 250 K 20% 1/2W	11237	360S254B
R24	040182	POT CERMET 250 K 20% 1/2W	11237	360S254B
R25	010467	RES METAL FSV 1%	21793	010467
R26	010467	RES METAL FSV 1%	21793	010467
R27	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R28	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R29	000244	RES CARBON 240 K 5% 1/4W	81349	RC07GF244J
R30	000244	RES CARBON 240 K 5% 1/4W	81349	RC07GF244J
R31	000244	RES CARBON 240 K 5% 1/4W	81349	RC07GF244J

403906 – Assy., PCB, DIGITIZER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R32	000244	RES CARBON 240 K 5% 1/4W	81349	RC07GF244J
R33	040238	POT CERMET 500 K 10%	73138	89PR500K
R34	000107	RES CARBON 100 M 5% 1/4W	81349	RC07GF107J
R35	010818	RES METAL 43.2 K 1% 1/10W	81349	RN55C4322F
R36	000106	RES CARBON 10 M 5% 1/4W	81349	RC07GF106J
R37	020676	RES WW 99.9 K .02%	21793	020676
R38	000514	RES CARBON 510 K 5% 1/4W	81349	RC07GF514J
R39	040227	POT CERMET 200 OHM 10%	73138	89PR200
R40	010918	RES METAL 499 OHM 1% 1/10W	81349	RN55C4990F
R41	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R42	040210	POT CERMET 100 K 20% 1 W	11237	360S104B
R43	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R44	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R45	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R46	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R47	000203	RES CARBON 20 K 5% 1/4W	81349	RC07GF203J
R48	000184	RES CARBON 180 K 5% 1/4W	81349	RC07GF184J
R49	020677	RES WW, SET W/R53, R58	21793	020677
R50	040229	POT CERMET 1 K 10%	73138	89PR1K
R51	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R52	000394	RES CARBON 390 K 5% 1/4W	81349	RC07GF394J
R53	020677	RES WW, SET W/R49, R58	21793	020677
R54	000201	RES CARBON 200 OHM 5% 1/4W	81349	RC07GF201J
R55	040226	POT CERMET 100 OHM 10%	73138	89PR100
R56	040240	POT CERMET 10 OHM 20%	73138	89PR10
R57	040240	POT CERMET 10 OHM 20%	73138	89PR10
R58	020677	RES WW, SET W/R53, R49	21793	020677
R59	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R60	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R61	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R62	010541	RES METAL 40.2 K 1% 1/10W	81349	RN55C4022F
R63	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R64	010541	RES METAL 40.2 K 1% 1/10W	81349	RN55C4022F
R71	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R72	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R73	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R74	010918	RES METAL 499 OHM 1% 1/10W	81349	RN55C4990F
R75	000208	RES CARBON 2000 M 20% 1/4W	01121	CB2082
U1	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U2	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U3	230313	INTEGRATED CIRCUIT	86884	CD4016AE
U4	230108	INTEGRATED CIRCUIT	01295	SN7416N
Z1	080012	RES MODULE 15 K 8 PIN 2%	21793	080012

403847 – Assy., PCB, REFERENCE ISOLATOR

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
AR1	230085	INTEGRATED CIRCUIT					27014	LM308AH
AR2	230103	INTEGRATED CIRCUIT					27014	LM308
AR3	230331	INTEGRATED CIRCUIT					27014	LF355H
AR4	230085	INTEGRATED CIRCUIT					27014	LM308AH
AR5	230119	INTEGRATED CIRCUIT μA741					07263	741HC
C1	120004	CAP	POLY	.001 MFD	500 V	5%	08257	KSO Series
C2	120344	CAP	POLY	.1 MFD	400 V	20%	12406	ZD4A104M
C3	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C4	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C5	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C7	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C8	100068	CAP	CERAM	.02 MFD	100 V	20%	56289	C023B101H203M
C9	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C10	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C11	100101	CAP	CERAM	33 PFD	1000 V	5%	56289	C030B102F330J
C12	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C13	100071	CAP	CERAM	.001 MFD	1000 V	20%	56289	C023B102E102M
C14	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
CR1	211083	DIODE	SILICO		018		21793	211083
CR2	211083	DIODE	SILICO		018		21793	211083
CR3	210004	DIODE	SILICO				81349	1N4004
CR4	220078	DIODE	ZENER	SELECTED	5 V	5%	81349	1N5231
CR5	220078	DIODE	ZENER	SELECTED	5 V	5%	81349	1N5231
CR7	220078	DIODE	ZENER	SELECTED	5 V	5%	81349	1N5231
CR8	220078	DIODE	ZENER	SELECTED	5 V	5%	81349	1N5231
CR10	403942	ZENER REFERENCE KIT					21793	403942
CR11	211083	DIODE	SILICO		018		21793	211083
Q1	200129	TRANS	SILICO	NPN			07263	SE4020
Q2	200068	TRANS		PNP			80131	2N4250
Q3	201084	TRANS	GERMAN	PNP			81349	2N1304
Q4	200246	TRANS					21793	200246
Q5	200201	TRANS	DUAL	NPN			21793	200201
Q6	200200	TRANS		NPN			21793	200200
Q7	200129	TRANS	SILICO	NPN			07263	SE4020
Q8	200230	TRANS	FET					E305
Q9	200230	TRANS	FET					E305

403847 – Assy., PCB, REFERENCE ISOLATOR *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q10	200200	TRANS NPN	21793	200200
Q11	200200	TRANS NPN	21793	200200
R1	001889	RES CARBON 39 K 5% 1/2W	81349	RC20GF393J
R2	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R3	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R5	000107	RES CARBON 100 M 5% 1/4W	81349	RC07GF107J
R6	000107	RES CARBON 100 M 5% 1/4W	81349	RC07GF107J
R7	000513	RES CARBON 51 K 5% 1/4W	81349	RC07GF513J
R8	040235	POT CERMET 100 K 10%	73138	89PR100K
R9	012008	RES METAL 442 OHM 1% 1/10W	81349	RN55C4420F
R10	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R11	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R12	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R13	001766	RES CARBON 220 K 5% 1/2W	81349	RC20GF224J
R14	001737	RES CARBON FSV 5% 1/4W	21793	001737
R15	012013	RES CMF 3.32 M 1% 1/4W	01121	CC3324F
R16	600245	JUMPER, INSULATED	21793	L-2007-1LP
R17	012009	RES CMF 2.21 M 1% 1/4W	01121	CC2214F
R18	001737	RES CARBON FSV 5% 1/4W	21793	001737
R19	012013	RES CMF 3.32 M 1% 1/4W	01121	CC3324F
R20	600245	JUMPER, INSULATED	21793	L-2007-1LP
R21	000683	RES CARBON 68 K 5% 1/4W	81349	RC07GF683J
R22	000364	RES CARBON 360 K 5% 1/4W	81349	RC07GF364J
R23	000186	RES CARBON 18 M 5% 1/4W	81349	RC07GF186J
R24	000513	RES CARBON 51 K 5% 1/4W	81349	RC07GF513J
R25	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R27	000224	RES CARBON 220 K 5% 1/4W	81349	RC07GF224J
R28	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R29	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R30	000332	RES CARBON 3.3 K 5% 1/4W	81349	RC07GF332J
R31	040226	POT CERMET 100 OHM 10%	73138	89PR100
R32	040227	POT CERMET 200 OHM 10%	73138	89PR200
R33	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R34	020678	RES WW, SET Matched W/R35 & R37	21793	020678
R35	020678	RES WW, SET Matched W/R34 & R37	21793	020678
R36	001759	RES CARBON 5.1 OHM 5% 1/4W	81349	RC07GF5R1J
R37	020678	RES WW, SET Matched W/R34 & R35	21793	020678
R39	001737	RES CARBON FSV 5% 1/4W	21793	001737

403847 – Assy., PCB, REFERENCE ISOLATOR *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R40	001737	RES CARBON FSV 5% 1/4W	21793	001737
R41	403942	ZENER REFERENCE KIT	21793	403942
R42	020693	RES WW 1 K .1%	22045	J90
R43	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R44	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R45	001737	RES CARBON FSV 5% 1/4W	21793	001737
R46	001737	RES CARBON FSV 5% 1/4W	21793	001737
R47	020675	RES WW, SET Matched W/R49	21793	020675
R48	040238	POT CERMET 500 K 10%	73138	89PR500K
R49	020675	RES WW, SET Matched W/R47	21793	020675
R50	001737	RES CARBON FSV 5% 1/4W	21793	001737
R51	001737	RES CARBON FSV 5% 1/4W	21793	001737
R52	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R54	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R55	010529	RES METAL 10 K 1% 1/10W	81349	RN55C1002F
R56	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R57	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R58	403942	ZENER REFERENCE KIT	21793	403942

403942 – Assy., ZENER REFERENCE KIT

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR1	220082	DIODE ZENER REF	04713	Z483
R1	020689	RES WW FSV	21793	020689
R2	001737	RES CARBON FSV 5% 1/4W	21793	001737

403904 – Assy., PCB, RMS CONVERTER, OPTION 10

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230324	INTEGRATED CIRCUIT FET	27014	LF356H
AR2	230324	INTEGRATED CIRCUIT FET	27014	LF356H
AR3	230054	INTEGRATED CIRCUIT	27014	LM301A
C1	120280	CAP MYLAR .22 MFD 1000 V 10%	27556	ZA2J224K
C2	100100	CAP CERAM FSV	21793	100100
C3	100100	CAP CERAM FSV	21793	100100
C4	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C5	100095	CAP CERAM 2.7±.5 PFD 1000 V	56289	C030B102S2R7D
C6	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C7	100100	CAP CERAM FSV	21793	100100
C8	100054	CAP CERAM 27 PFD 1000 V 5%	56289	C030B102G270J
C9	130123	CAP TRIMMER 1-3 PFD 250 V	52763	R-TR1K0-122-09SD
C10	100100	CAP CERAM FSV	21793	100100
C11	130160	CAP MICA 330 PFD	72136	DM-15 Series
C12	130124	CAP TRIMMER 1.7-10 PFD 250 V	52763	R-TR1K0-122-09SD
C13	130116	CAP MICA 3900 PFD 500 V 2%	72136	DM19F392G0
C14	100100	CAP CERAM FSV	21793	100100
C15	110140	CAP TANTA 47 MFD 6 V 20%	05397	T368B476M006AS
C16	100117	CAP CERAM 470 PFD 1000 V 20%	56289	C023B102E471M
C17	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C18	100102	CAP CERAM 47 PFD 1000 V 5%	56289	C030B102H470J
C19	100117	CAP CERAM 470 PFD 1000 V 20%	56289	C023B102E471M
C20	130160	CAP MICA 330 PFD	72136	DM-15 Series
C21	101642	CAP CERAM 150 PFD 500 V 10%	71471	SCD1X5F
C22	100040	CAP CERAM 200 PFD 1000 V 20%	56289	C023B102E201M
C23	120026	CAP MYLAR .47 MFD 100 V 10%	27556	SA2B474K
C24	120026	CAP MYLAR .47 MFD 100 V 10%	27556	SA2B474K
C25	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C26	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
CR1	211083	DIODE SILICO 018	21793	211083
CR2	211083	DIODE SILICO 018	21793	211083
CR3	220022	DIODE SILICO ZENER	81349	1N965B
CR4	220022	DIODE SILICO ZENER	81349	1N965B
CR5	211083	DIODE SILICO 018	21793	211083
CR6	211083	DIODE SILICO 018	21793	211083
CR7	211083	DIODE SILICO 018	21793	211083
CR8	210015	DIODE	50434	HP5082-2800
CR9	210015	DIODE	50434	HP5082-2800
CR10	211083	DIODE SILICO 018	21793	211083
CR11	220004	DIODE SILICO ZENER	81349	1N961B
CR12	220078	DIODE SILICO SELECTED 5 V 5%	81349	1N5231

403904 – Assy., PCB, RMS CONVERTER, OPTION 10 *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
K1	310127	RELAY REED	15636	RA3032-1051
K2	310125	RELAY REED 1 FORM A 5 V	21793	310125
K3	310125	RELAY REED 1 FORM A 5 V	21793	310125
Q1	200068	TRANS PNP	80131	2N4250
Q2	200197	TRANS SILICO NPN	04713	MPS-H10
Q3	200197	TRANS SILICO NPN	04713	MPS-H10
Q4	403865	TRANS SET MATCHED LOG	21793	403865
Q5	403865	TRANS SET MATCHED LOG	21793	403865
Q6	200068	TRANS PNP	80131	2N4250
Q7	200201	TRANS DUAL NPN	21793	200201
Q8	200068	TRANS PNP	80131	2N4250
Q9	200200	TRANS NPN	21793	200200
Q10	200200	TRANS NPN	21793	200200
Q11	200068	TRANS PNP	80131	2N4250
R1	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R2	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R3	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R4	001737	RES CARBON FSV 5% 1/4W	21793	001737
R5	012015	RES SET, W/R6, R8, R9, R11, R12	21793	012015
R6	012015	RES SET, W/R5, R8, R9, R11, R12	21793	012015
R7	000107	RES CARBON 100 M 5% 1/4W	81349	RC07GF107J
R8	012015	RES SET, W/R5, R6, R9, R11, R12	21793	012015
R9	012015	RES SET, W/R5, R6, R8, R11, R12	21793	012015
R10	010720	RES METAL 9.09 K 1/4% 1/10W	81349	RN55C9091C
R11	012015	RES SET, W/R5, R6, R8, R9, R12	21793	012015
R12	012015	RES SET, W/R5, R6, R8, R9, R11	21793	012015
R13	040211	POT CERMET 500 OHM 20%	11237	360S Series
R14	040257	POT CERMET 50 OHM 20% 1/2W	80294	3389S-500
R15	040211	POT CERMET 500 OHM 20%	11237	360S Series
R16	000204	RES CARBON 200 K 5% 1/4W	81349	RC07GF204J
R17	403865	TRANS SET MATCHED LOG	21793	403865
R18	012017	RES SET, W/R23, R46	21793	012017
R19	012018	RES SET, W/R26	21793	012018
R20	040257	POT CERMET 50 OHM 20% 1/2W	80294	3389S-500
R21	000336	RES CARBON 33 M 5% 1/4W	81349	RC07GF336J
R22	040210	POT CERMET 100 K 20% 1 W	11237	360S104B
R23	012017	RES SET, W/R18, R46	21793	012017
R24	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R25	010818	RES METAL 43.2 K 1% 1/10W	81349	RN55C4322F
R26	012018	RES SET, W/R19	21793	012018

403904 – Assy., PCB, RMS CONVERTER, OPTION 10 *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R27	000242	RES	CARBON	2.4 K	5%	1/4W	81349	RC07GF242J
R28	040264	POT	CERMET	25 K	20%	1/2W	73138	72XW25K
R29	000182	RES	CARBON	1.8 K	5%	1/4W	81349	RC07GF182J
R30	010600	RES	METAL	249 OHM	1%	1/10W	81349	RN55C2490F
R31	000512	RES	CARBON	5.1 K	5%	1/4W	81349	RC07GF512J
R32	040257	POT	CERMET	50 OHM	20%	1/2W	80294	3389S-500
R33	010533	RES	METAL	28.7 K	1%	1/10W	81349	RN55C2872F
R34	010818	RES	METAL	43.2 K	1%	1/10W	81349	RN55C4322F
R35	000392	RES	CARBON	3.9 K	5%	1/4W	81349	RC07GF392J
R36	000103	RES	CARBON	10 K	5%	1/4W	81349	RC07GF103J
R37	000470	RES	CARBON	47 OHM	5%	1/4W	81349	RC07GF470J
R38	040210	POT	CERMET	100 K	20%	1 W	11237	360S104B
R39	000756	RES	CARBON	75 M	5%	1/4W	81349	RC07GF756J
R40	010918	RES	METAL	499 OHM	1%	1/10W	81349	RN55C4990F
R41	000102	RES	CARBON	1 K	5%	1/4W	81349	RC07GF102J
R42	000102	RES	CARBON	1 K	5%	1/4W	81349	RC07GF102J
R43	001759	RES	CARBON	5.1 OHM	5%	1/4W	81349	RC07GF5R1J
R44	040257	POT	CERMET	50 OHM	20%	1/2W	80294	3389S-500
R45	000104	RES	CARBON	100 K	5%	1/4W	81349	RC07GF104J
R46	012017	RES	SET, W/R18, R23				21793	012017
R47	403865	TRANS	SET	MATCHED LOG			21793	403865
R48	000105	RES	CARBON	1 M	5%	1/4W	81349	RC07GF105J
R49	001737	RES	CARBON	FSV	5%	1/4W	21793	001737
R50	012016	RES	SET, W/R52				21793	012016
R51	040258	POT	CERMET	100 OHM	20%	1/2W	73138	72XW100
R52	012016	RES	SET, W/R50				21793	012016
R53	001737	RES	CARBON	FSV	5%	1/4W	21793	001737
TP1	600786	POST, MACHINE APPLIED STRIP					00779	1-87022-0
TP2	600786	POST, MACHINE APPLIED STRIP					00779	1-87022-0
TP3	600786	POST, MACHINE APPLIED STRIP					00779	1-87022-0
TP4	600786	POST, MACHINE APPLIED STRIP					00779	1-87022-0
TP5	600786	POST, MACHINE APPLIED STRIP					00779	1-87022-0

403905 – Assy., PCB, AC AVERAGING CONVERTER, OPTION 14

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230180	INTEGRATED CIRCUIT	27014	LM318H
C1	120280	CAP MYLAR .22 MFD 1000 V 10%	27556	ZA2J224K
C2	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C3	120101	CAP POLY FSV	21793	120101
C4	120101	CAP POLY FSV	21793	120101
C5	130146	CAP TRIMMER .25-1.5 PFD	74970	273-0001-002
C6	100101	CAP CERAM 33 PFD 1000 V 5%	56289	C030B102F330J
C7	130123	CAP TRIMMER 1-3 PFD 250 V	52763	R-TR1K0-122-09SD
C8	120158	CAP POLY 390 PFD 63 V 5%	26625	611
C9	130148	CAP TRIMMER 5-20 PFD 250 V	52763	R-TR1K0-122-09MG
C10	120246	CAP POLY 0.01 MFD 33 V 5%	08257	KSC Series
C11	120294	CAP MYLAR .47 MFD 100 V 20%	73445	C281AH/A470K
C12	120101	CAP POLY FSV	21793	120101
C13	110186	CAP TANTA 330 MFD 6 V	05397	T362D337K006AS
C14	100076	CAP CERAM 20 PFD 1000 V 5%	56289	C030B102F200J
C15	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C16	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C17	110186	CAP TANTA 330 MFD 6 V	05397	T362D337K006AS
C18	120101	CAP POLY FSV	21793	120101
C19	120101	CAP POLY FSV	21793	120101
C20	111148	CAP ELECT 100 MFD 25 V	34553	ET101X025A5
C21	120101	CAP POLY FSV	21793	120101
CR1	220004	DIODE SILICO ZENER	81349	1N961B
CR2	211083	DIODE SILICO 018	21793	211083
CR3	211083	DIODE SILICO 018	21793	211083
CR4	211083	DIODE SILICO 018	21793	211083
CR5	211083	DIODE SILICO 018	21793	211083
CR6	220007	DIODE SILICO ZENER	81349	1N751A
CR7	220007	DIODE SILICO ZENER	81349	1N751A
CR8	210015	DIODE	50434	HP5082-2800
CR9	210015	DIODE	50434	HP5082-2800
K1	310125	RELAY REED 1 FORM A 5 V	21793	310125
K2	310125	RELAY REED 1 FORM A 5 V	21793	310125
K3	310125	RELAY REED 1 FORM A 5 V	21793	310125
Q1	200199	TRANS FET	27014	FM1302
Q2	200088	TRANS SILICO PNP	80131	2N4248
Q3	200200	TRANS NPN	21793	200200
Q4	200200	TRANS NPN	21793	200200

403905 – Assy., PCB, AC AVERAGING CONVERTER, OPTION 14 *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
Q5	200197	TRANS SILICO NPN	04713	MPS-H10
Q6	200197	TRANS SILICO NPN	04713	MPS-H10
R1	012012	RES SET	21793	012012
R3	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R4	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R5	000511	RES CARBON 510 OHM 5% 1/4W	81349	RC07GF511J
R6	000822	RES CARBON 8.2 K 5% 1/4W	81349	RC07GF822J
R7	000561	RES CARBON 560 OHM 5% 1/4W	81349	RC07GF561J
R8	000331	RES CARBON 330 OHM 5% 1/4W	81349	RC07GF331J
R9	010929	RES METAL 2.10 K 1% 1/10W	81349	RN55C2101F
R10	040255	POT CERMET 10 OHM 20% 1/2W	73138	72XW10
R11	012012	RES SET	21793	012012
R12	012012	RES SET	21793	012012
R13	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R14	010536	RES METAL 100 K 1% 1/10W	81349	RN55C1003F
R15	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R16	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R17	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R18	012012	RES SET	21793	012012
R19	040261	POT CERMET 2 K 20% 1/2W	73138	72XW2K
R20	012012	RES SET	21793	012012
R21	040259	POT CERMET 200 OHM 20% 1/2W	73138	72XW200
R22	012012	RES SET	21793	012012
R23	040256	POT CERMET 20 OHM 20% 1/2W	73138	72XW20
R24	012012	RES SET	21793	012012
R25	010802	RES METAL FSV 1%	21793	010802
R26	010802	RES METAL FSV 1%	21793	010802
R27	010802	RES METAL FSV 1%	21793	010802
R28	010802	RES METAL FSV 1%	21793	010802
R29	010802	RES METAL FSV 1%	21793	010802
W1	600245	JUMPER INSULATED		L-2007-1LP

403902 – Assy., PCB, DATA OUTPUT, OPTION 51

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230275	INTEGRATED CIRCUIT 5.0 V	04713	MC7805CT
C1	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C2	110183	CAP ELECT 220 MFD 16 V	34553	ET221X106A6
C3	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C4	110151	CAP TANTA 10 MFD 35 V 20%	05397	T362C106M035A
C5	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
CR1	210004	DIODE SILICO	81349	1N4004
CR2	210004	DIODE SILICO	81349	1N4004
CR3	210004	DIODE SILICO	81349	1N4004
CR4	210004	DIODE SILICO	81349	1N4004
OCI-1	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
OCI-2	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
OCI-3	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
OCI-4	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
OCI-5	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
OCI-6	250005	OPTO ISOLATOR, LOGIC DRIVER	21793	250005
P2	600859	CONN 20 POS	00779	87133-6
P6	600860	CONN 2 POS	00779	87176-1
R1	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R2	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R3	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R4	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R5	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R6	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R7	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R8	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R9	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R10	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R11	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R12	000621	RES CARBON 620 OHM 5% 1/4W	81349	RC07GF621J
R13	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
U1	230192	INTEGRATED CIRCUIT	01295	SN74LS05N
U2	230306	INTEGRATED CIRCUIT	01295	SN74LS02
U3	230194	INTEGRATED CIRCUIT	01295	SN74LS74N
U4	230317	INTEGRATED CIRCUIT	01295	74LS90
U5	230315	INTEGRATED CIRCUIT	01295	SN74LS153N
U6	230315	INTEGRATED CIRCUIT	01295	SN74LS153N

403902 – Assy., PCB, DATA OUTPUT, OPTION 51 *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
U7	230236	INTEGRATED CIRCUIT	01295	SN74LS47N
U8	230193	INTEGRATED CIRCUIT	01295	SN74LS00N
U9	230238	INTEGRATED CIRCUIT	27014	74LS164
U10	230238	INTEGRATED CIRCUIT	27014	74LS164
U11	230238	INTEGRATED CIRCUIT	27014	74LS164
U12	230238	INTEGRATED CIRCUIT	27014	74LS164

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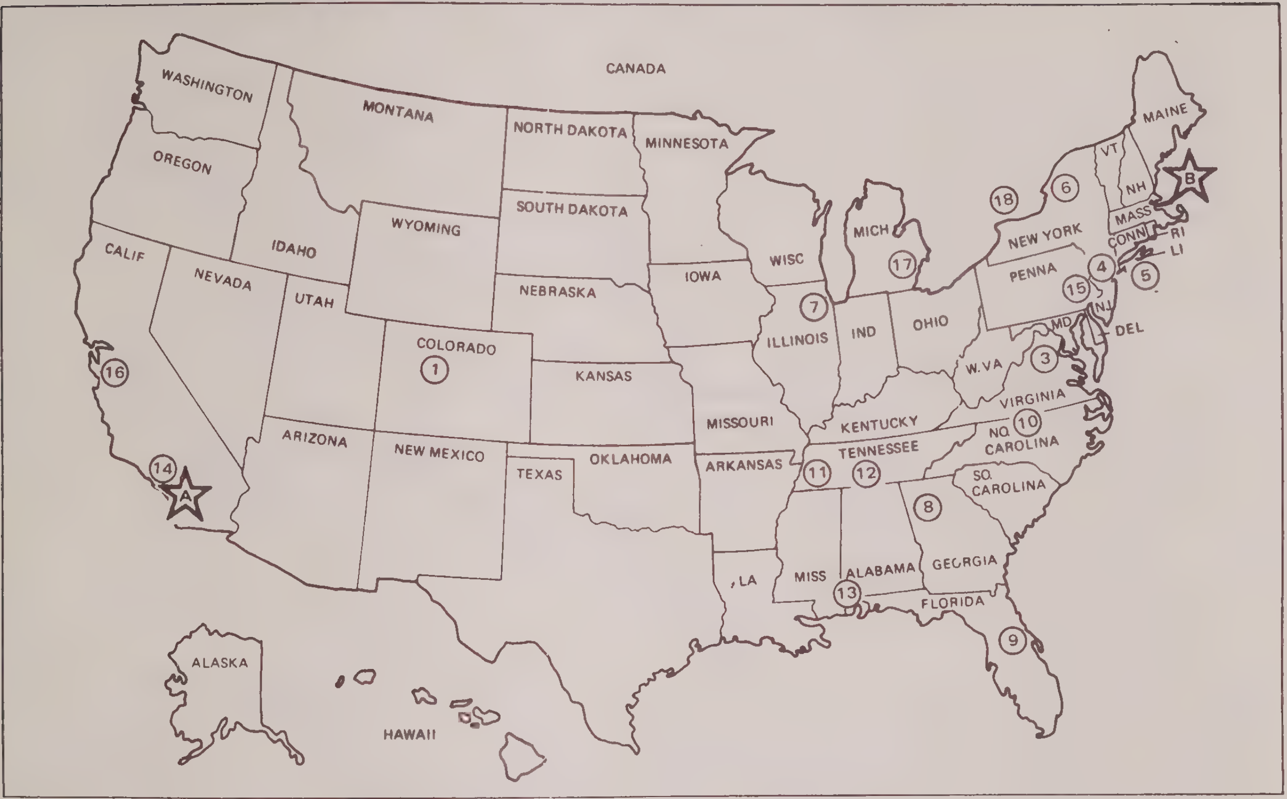
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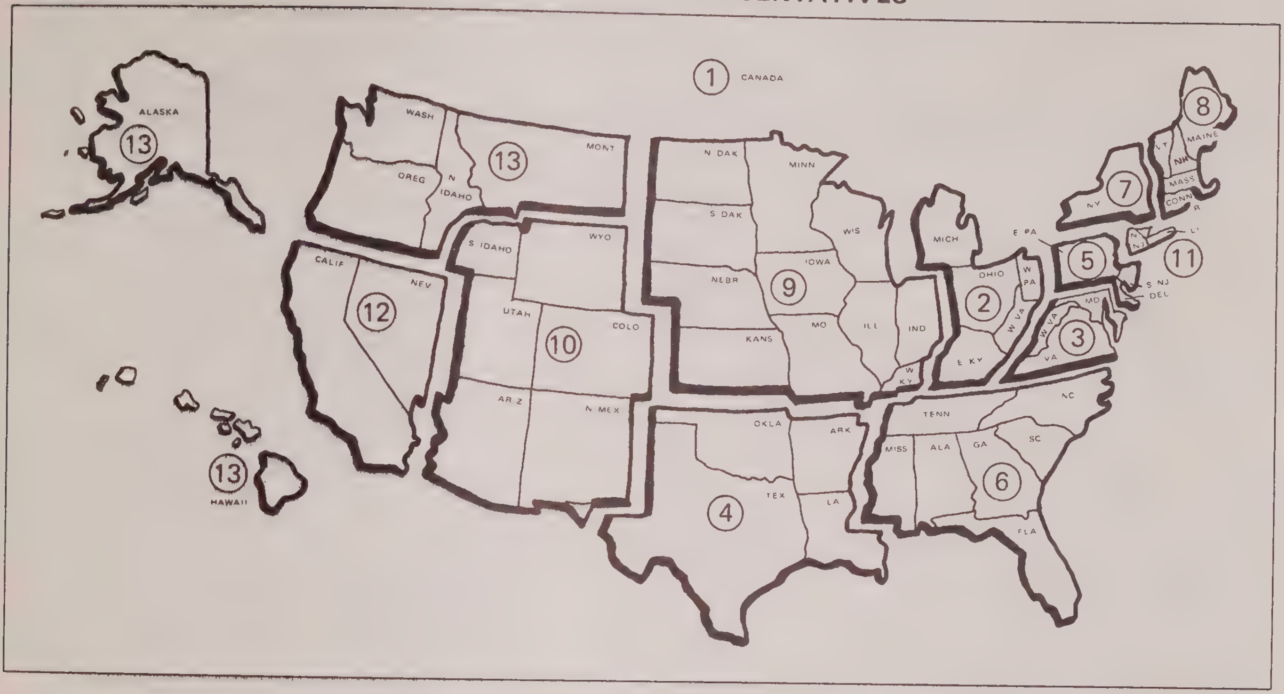

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